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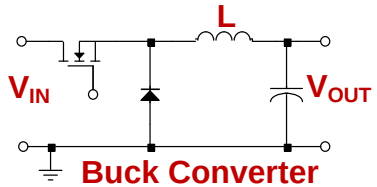
Switch-Mode Power Supplies (SMPS) Topologies and Fundamentals

Agenda

- Power terminology you need to know (Conduction modes and Control methods)
- Non-Synchronous/Synchronous Buck converter operation
- Boost converter operation
- Inverting Buck operation
- 4 switch Buck/Boost operation
- Fly-buck, SEPIC, Flyback, and Forward converter operation
- Brief overview of other converters you may encounter
- What questions to ask
- Efficiency, size, and cost – how do they effect the design

Buck, boost and buck-boost derived topologies

Buck, forward, push-pull, bridge



$$V_{OUT} = V_{IN} \cdot D$$

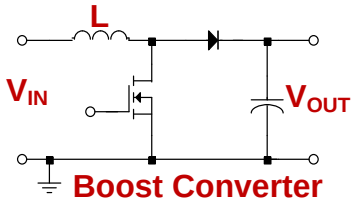
- Forward
- Two switch forward
- Active clamp forward
- Half bridge

$$V_{OUT} = V_{IN} \cdot D \cdot \frac{N_S}{N_P}$$

- Push-pull
- Full bridge
- Phase-shifted full bridge

$$V_{OUT} = V_{IN} \cdot 2 \cdot D \cdot \frac{N_S}{N_P}$$

Boost

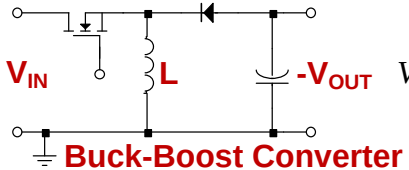


$$V_{OUT} = V_{IN} \cdot \frac{1}{D'}$$

- Boost topology

On-time duty cycle: D
Off-time duty cycle: D′ = 1 - D

Buck-boost, SEPIC, flyback



$$V_{OUT} = V_{IN} \cdot \frac{D}{D'}$$

- Buck-boost derived topologies
- SEPIC
- Cuk
- Flyback

$$V_{OUT} = V_{IN} \cdot \frac{D}{D'} \cdot \frac{N_S}{N_P}$$

Continuous Vs. Discontinuous conduction mode

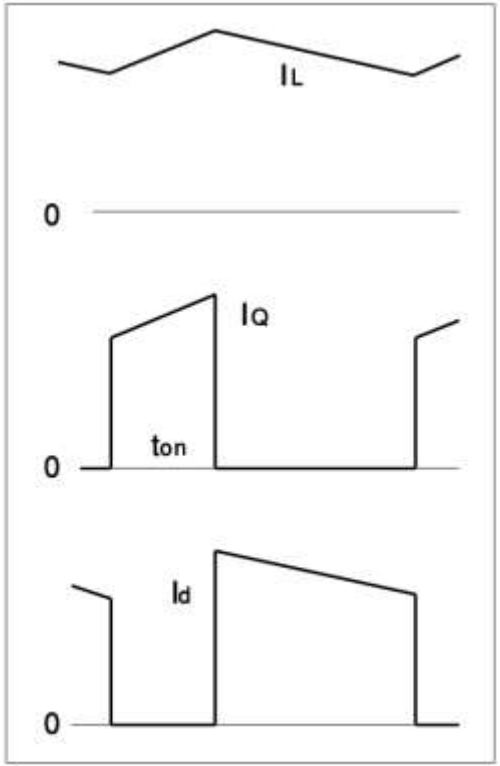


Fig. 8. - Continuous Mode Waveforms

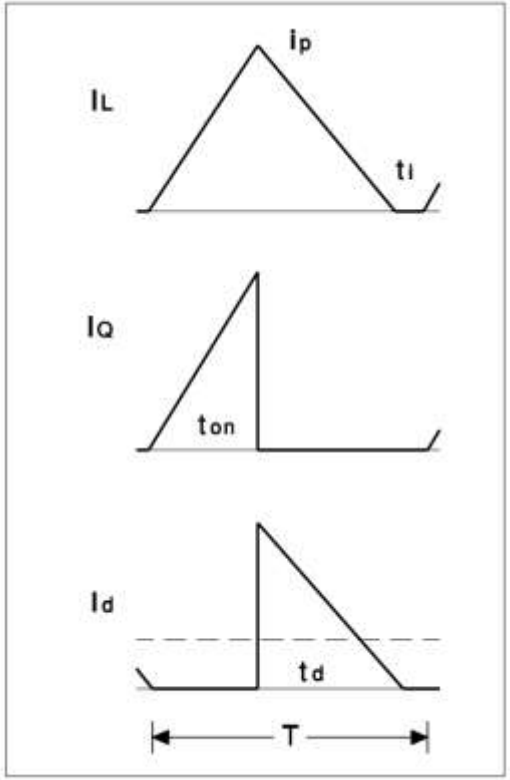


Fig. 9. - Discontinuous Mode

Loop Control Methods (Voltage Mode)

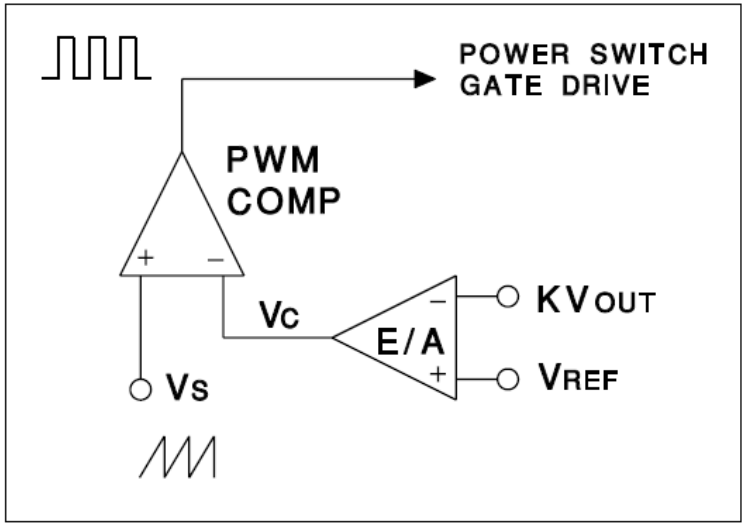


Figure 10. - PWM Comparator

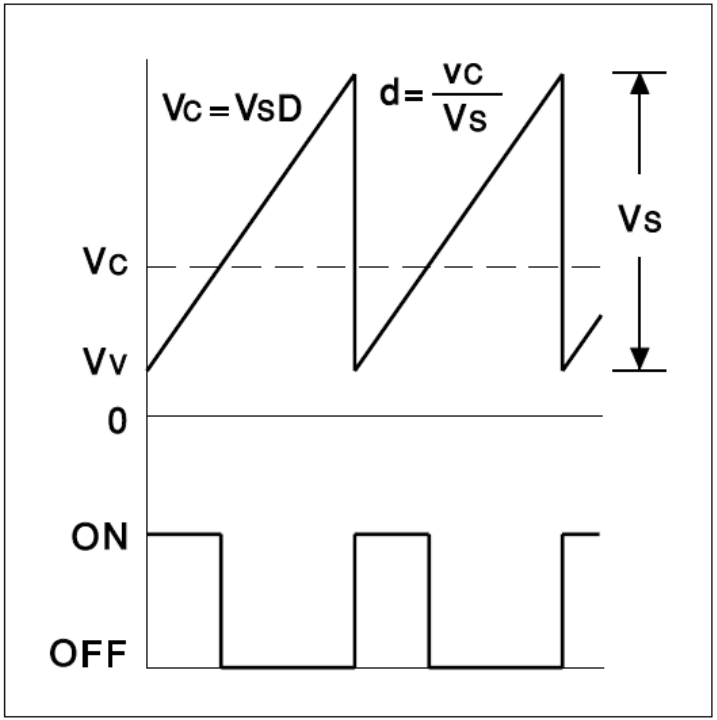


Figure 11. - PWM Waveforms

Loop Control Methods (Peak current mode)

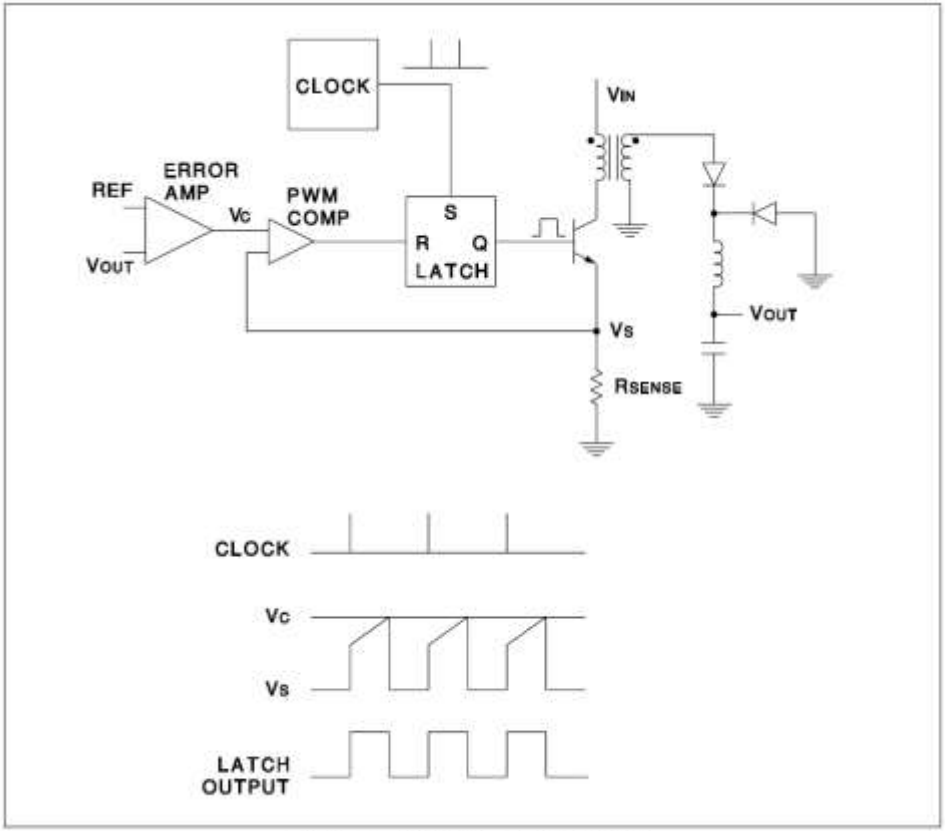


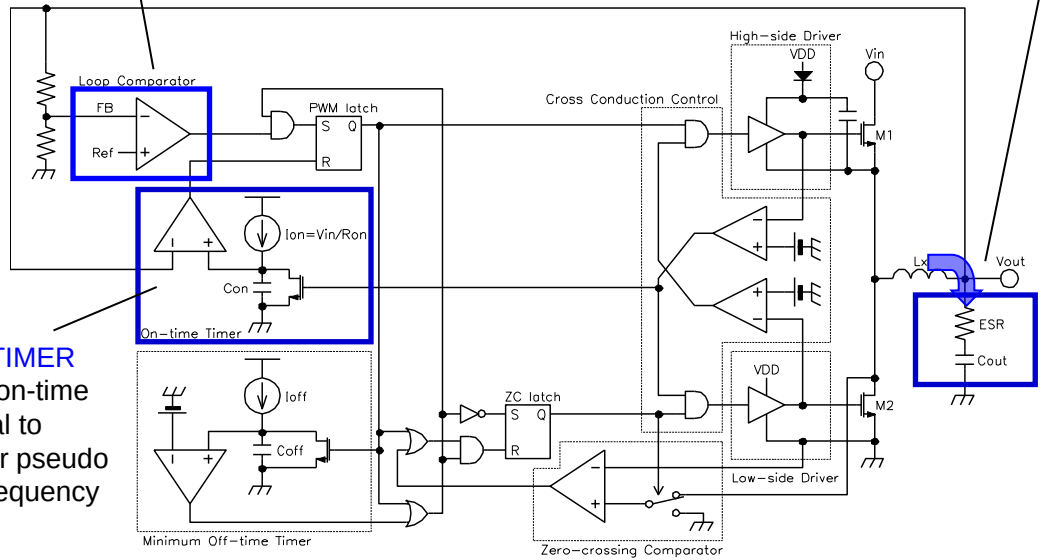
Figure 13. - Peak Current Mode Control

Loop Control Methods DCAP with Constant On-Time Modulator

3 Fundamental Components

2. PWM COMPARATOR compares VFB DIRECTLY with V_{REF}

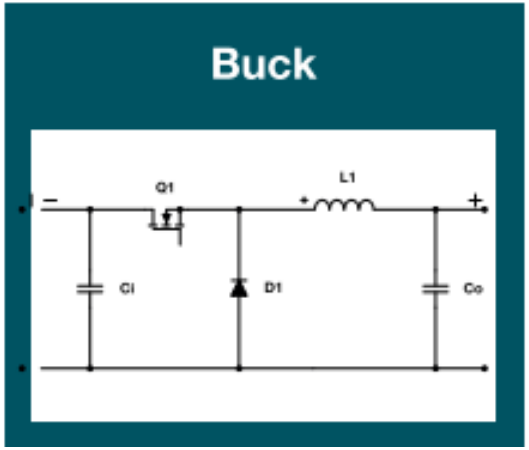
1. ESR combines current information on top of the average output voltage



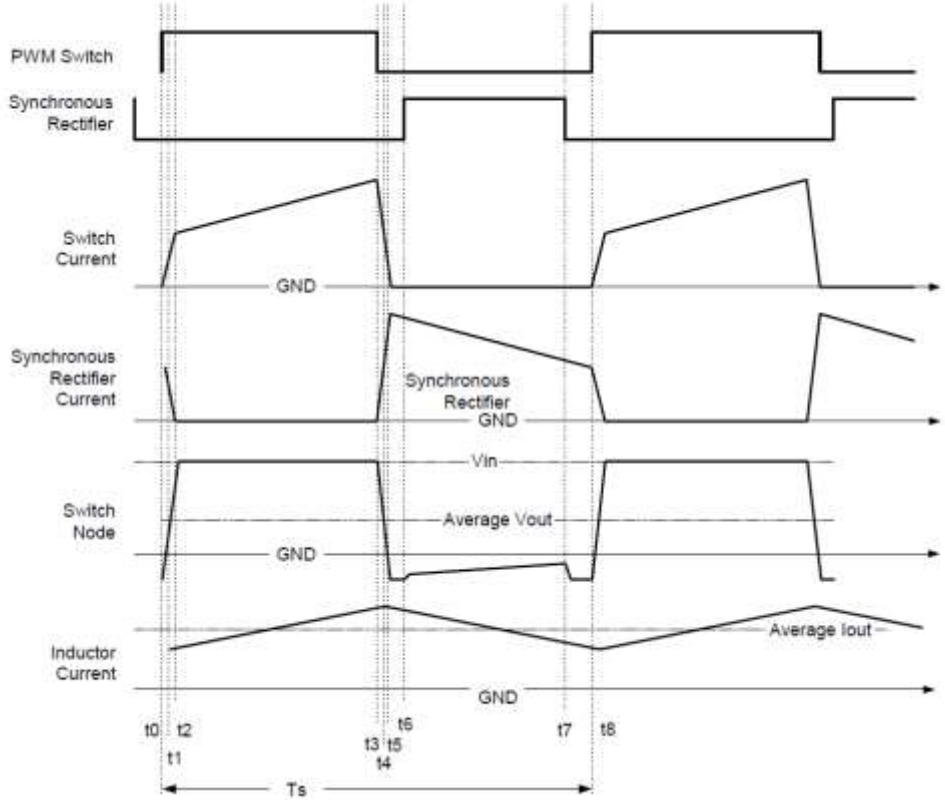
3. ON-TIME TIMER generates on-time proportional to Vin/Vout for pseudo constant frequency operation

Non-Synchronous Buck Converter overview

Buck converter makes a lower output voltage than the input voltage

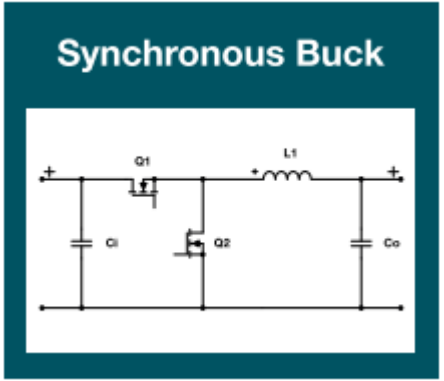


Duty Cycle	$D = \frac{V_{out} + V_f}{V_{in} + V_f}$
Q1 FET Voltage	$V_{Q1} = V_{in} + V_f$
D1 Diode Voltage	$V_{D1} = V_{in}$

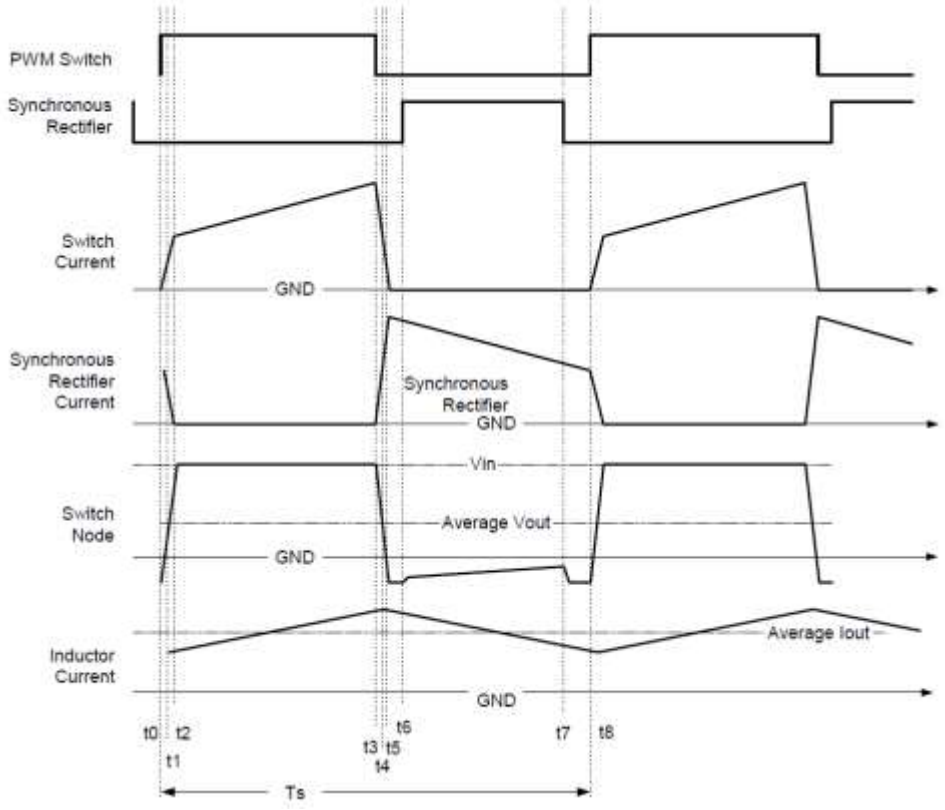


Synchronous Buck converter overview

Buck converter makes a lower output voltage than the input voltage

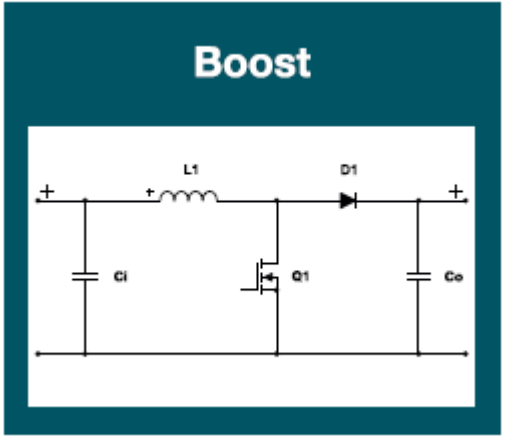


Duty Cycle	$D = \frac{V_{out}}{V_{in}}$
Q1 FET Voltage	$V_{Q1} = V_{in}$
D1 Diode Voltage	$V_{Q2} = V_{in}$

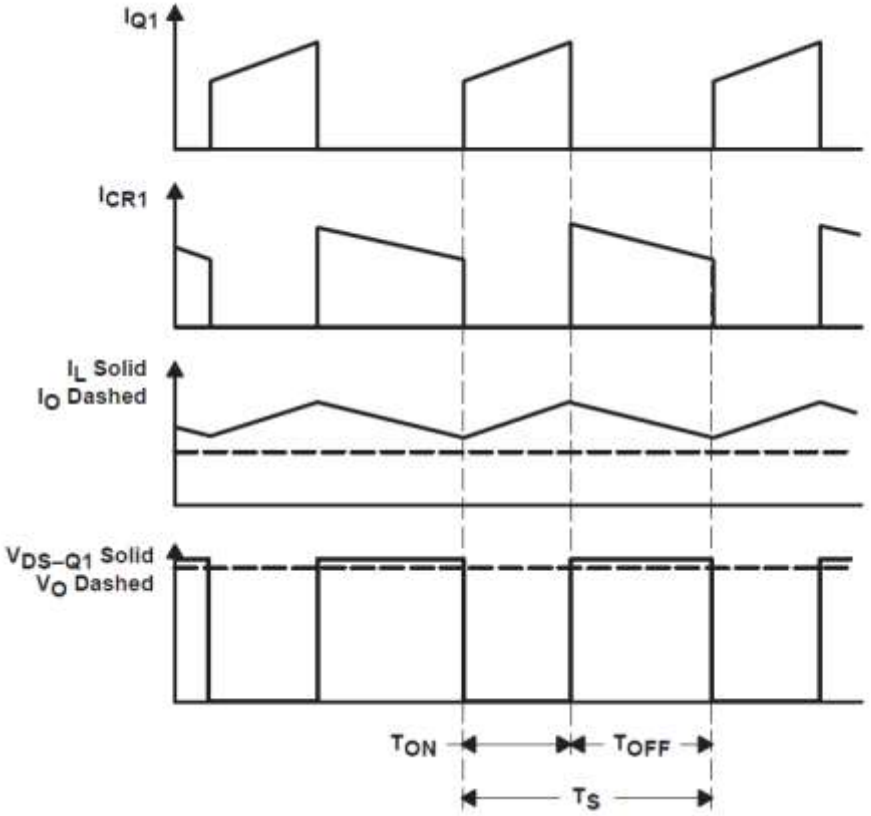


Boost converter Overview

Boost converter makes a higher output voltage than the input voltage

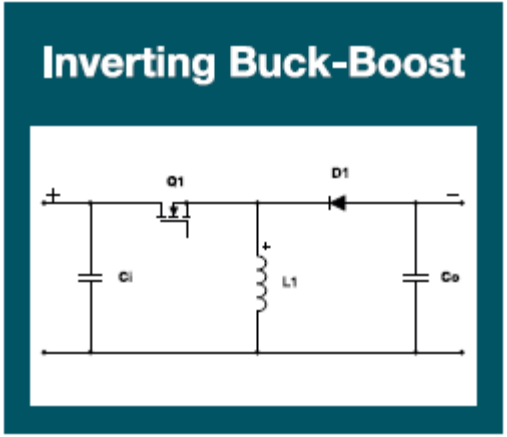


Duty Cycle	$D = \frac{V_{out} + V_f - V_{in}}{V_{out} + V_f}$
Q1 FET Voltage	$V_{Q1} = V_{out} + V_f$
D1 Diode Voltage	$V_{D1} = V_{out}$

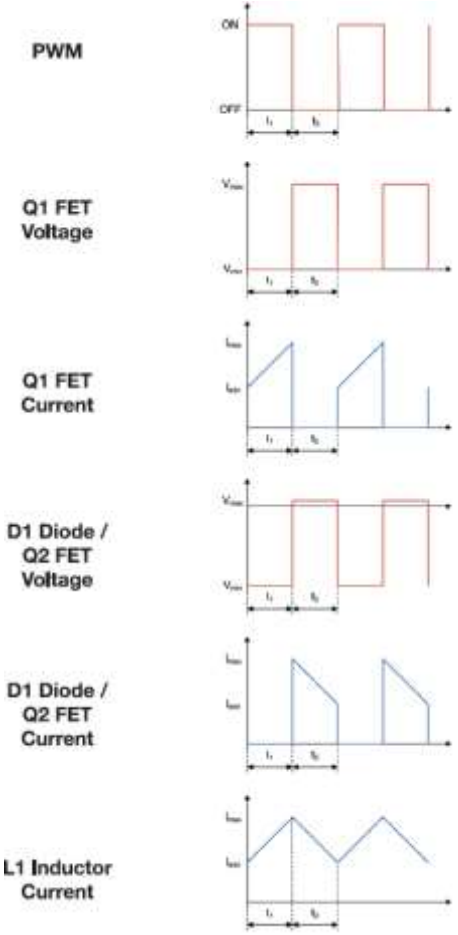


Inverting Buck-Boost

Inverting Buck-Boost converter makes a negative output voltage from a positive input voltage



Duty Cycle	$D = \frac{-V_{out} + V_f}{-V_{out} + V_f + V_{in}}$
Q1 FET Voltage	$V_{Q1} = V_{in} + V_f - V_{out}$
D1 Diode Voltage	$V_{D1} = V_{in} - V_{out}$



Inverting Buck-Boost

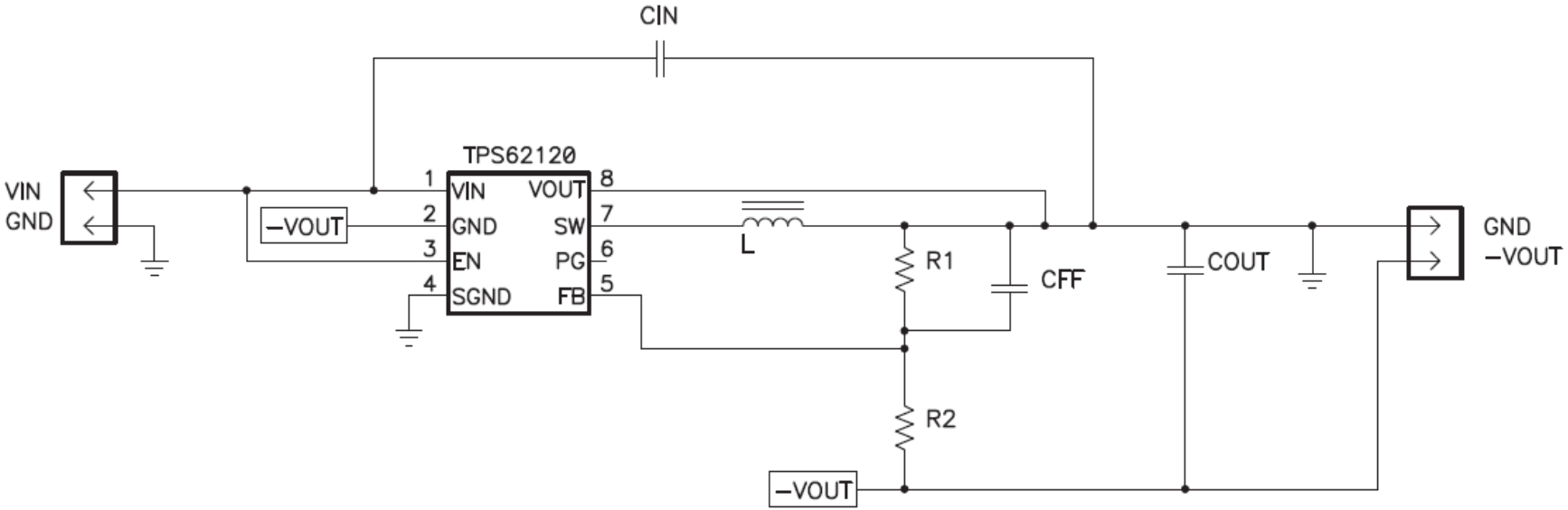


Figure 2. TPS62120 Inverting Buck-Boost Topology

4 Switch Buck/Boost

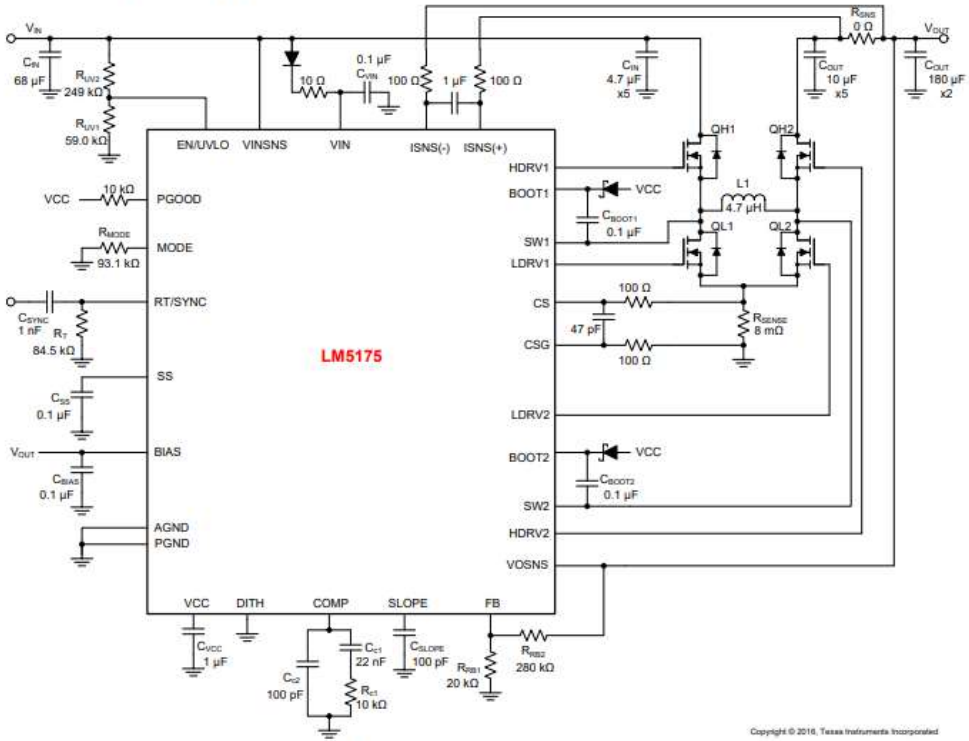


Figure 24. LM5175 Four-Switch Buck Boost Application Schematic

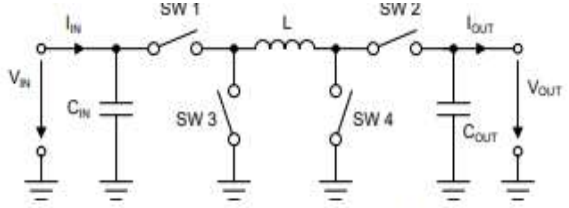
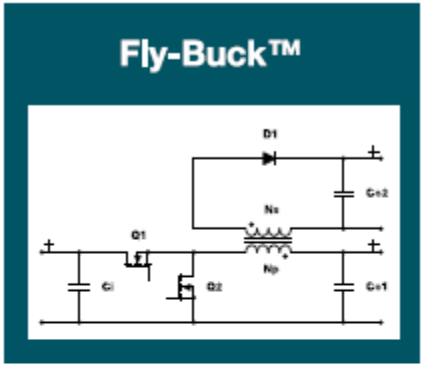


Figure 1. Buck-Boost Converter Schematic

Fly-Buck Converter



Duty Cycle

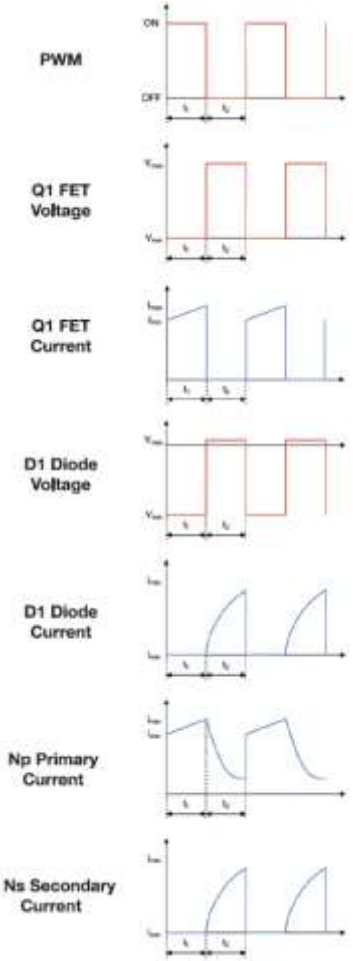
$$D = \frac{V_{out\_pri}}{V_{in}}$$

Q1 FET Voltage

$$V_{Q1} = V_{in}$$

D1 Diode Voltage

$$V_{D1} = V_{out\_sec} + (V_{in} - V_{out\_pri}) \cdot \frac{N_s}{N_p}$$



Fly-Buck Converter

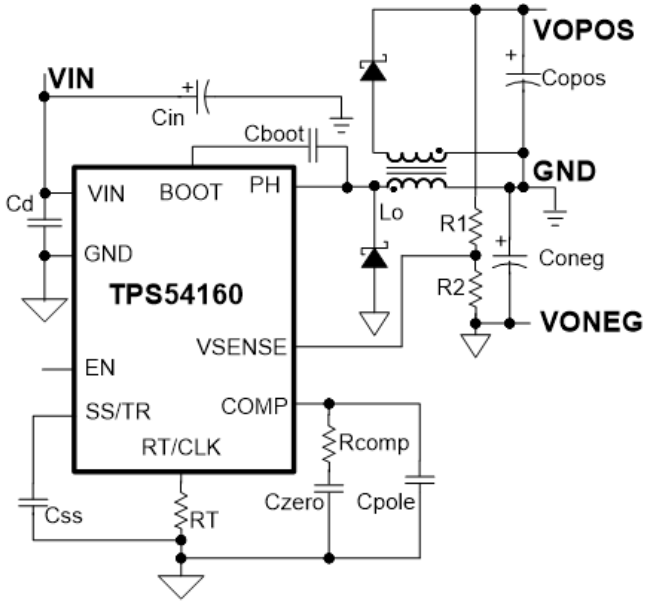
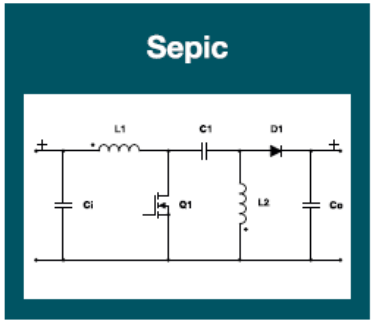


Figure 1 Split Rail Power Supply Schematic using the Inverting Method.

Sepic Converter

Can buck or boost



Duty Cycle

$$D = \frac{V_{out} + V_f}{V_{out} + V_f + V_{in}}$$

Q1 FET Voltage

$$V_{Q1} = V_{in} + V_{out} + V_f + \frac{V_{C1,ripple}}{2}$$

D1 Diode Voltage

$$V_{D1} = V_{in} + V_{out} + \frac{V_{C1,ripple}}{2}$$

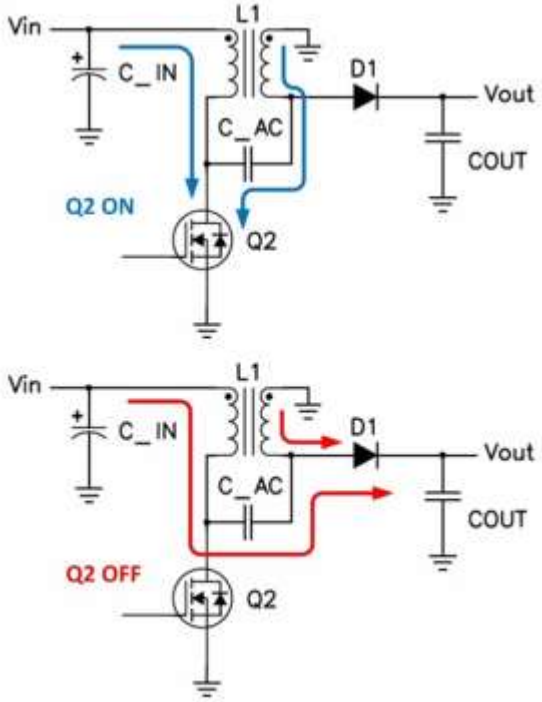


Figure 1: A coupled-inductor SEPIC converter has two current paths

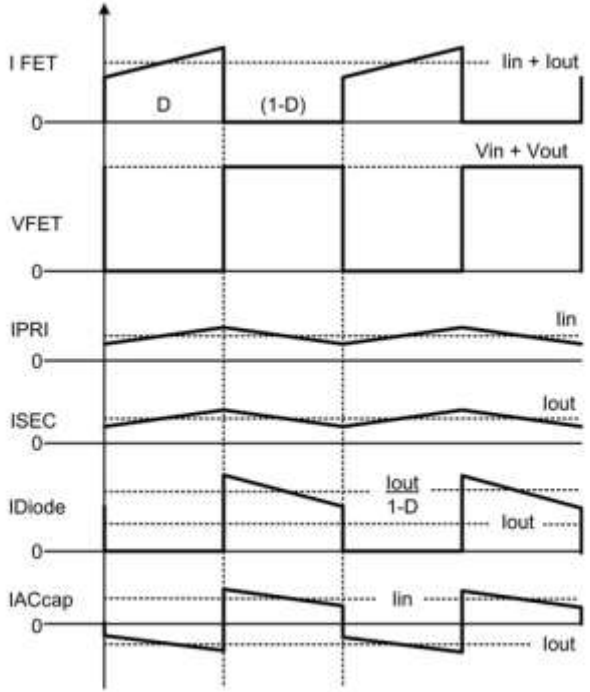
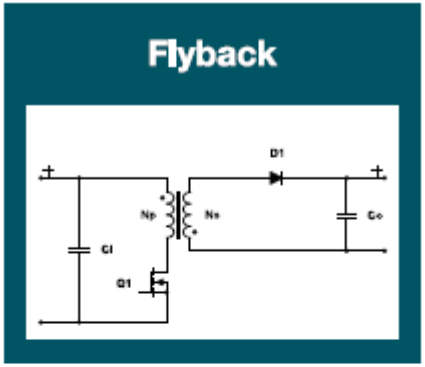


Figure 2: Key waveforms for a continuous-conduction-mode (CCM) SEPIC

Flyback Converter



Duty Cycle

$$D = \frac{(V_{out} + V_f) \cdot \frac{N_p}{N_s}}{V_{in} + (V_{out} + V_f) \cdot \frac{N_p}{N_s}}$$

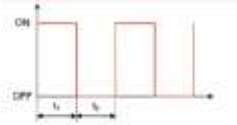
Q1 FET Voltage

$$V_{Q1} = V_{in} + (V_{out} + V_f) \cdot \frac{N_p}{N_s}$$

D1 Diode Voltage

$$V_{D1} = V_{out} + V_{in} \cdot \frac{N_s}{N_p}$$

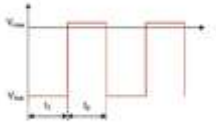
PWM



Q1 FET Voltage

Q1 FET Current

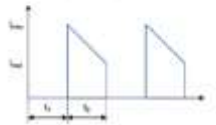
D1 Diode Voltage



D1 Diode Current

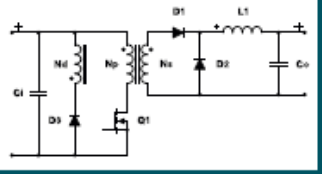
Np Primary Current

Ns Secondary Current

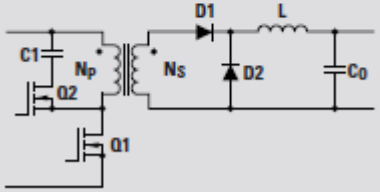


Forward Converter

Single Switch Forward



ACTIVE CLAMP FORWARD



Duty Cycle

$$D = \frac{(V_{out} + V_f)}{V_{in} \cdot \frac{N_s}{N_p}}$$

Q1 FET Voltage

$$V_{Q1} = 2 \cdot V_{in} + V_f$$

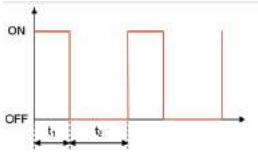
D1 Diode Voltage

$$V_{D1} = (V_{in} + V_f) \cdot \frac{N_s}{N_d} - V_f$$

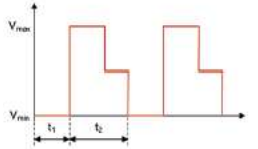
D2 Diode Voltage

$$V_{D2} = V_{in} \cdot \frac{N_s}{N_p} - V_f$$

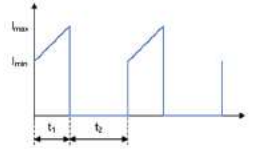
PWM



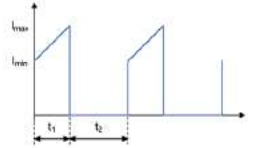
Q1 FET Voltage



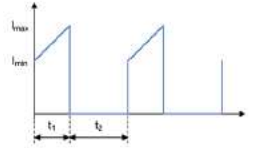
Q1 FET Current



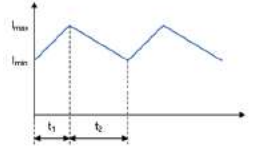
Np Primary Current



Ns Secondary Current

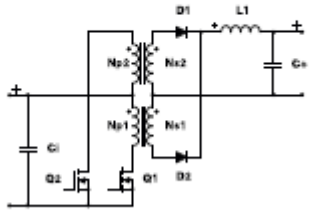


L1 Inductor Current

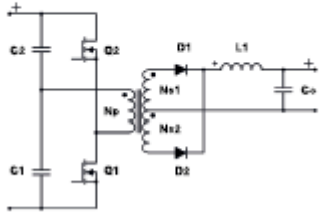


Various other converters

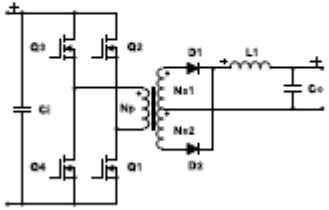
Push-Pull



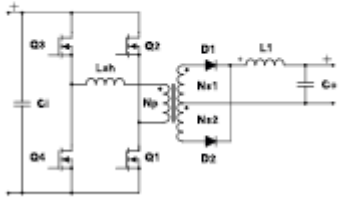
Half-Bridge



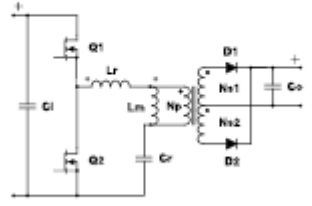
Full-Bridge



Phase Shifted Full-Bridge



LLC Half-Bridge



Questions to ask when working on a PS

Design specifications

- Vinmax = 30V
- Vinmin = 26V
- Vout = 15V
- Iomax = 2.8A
- Switching Frequency = 300khz
- Vout ripple = 50mV
- Vin ripple = 500mV
- Efficiency > 90%

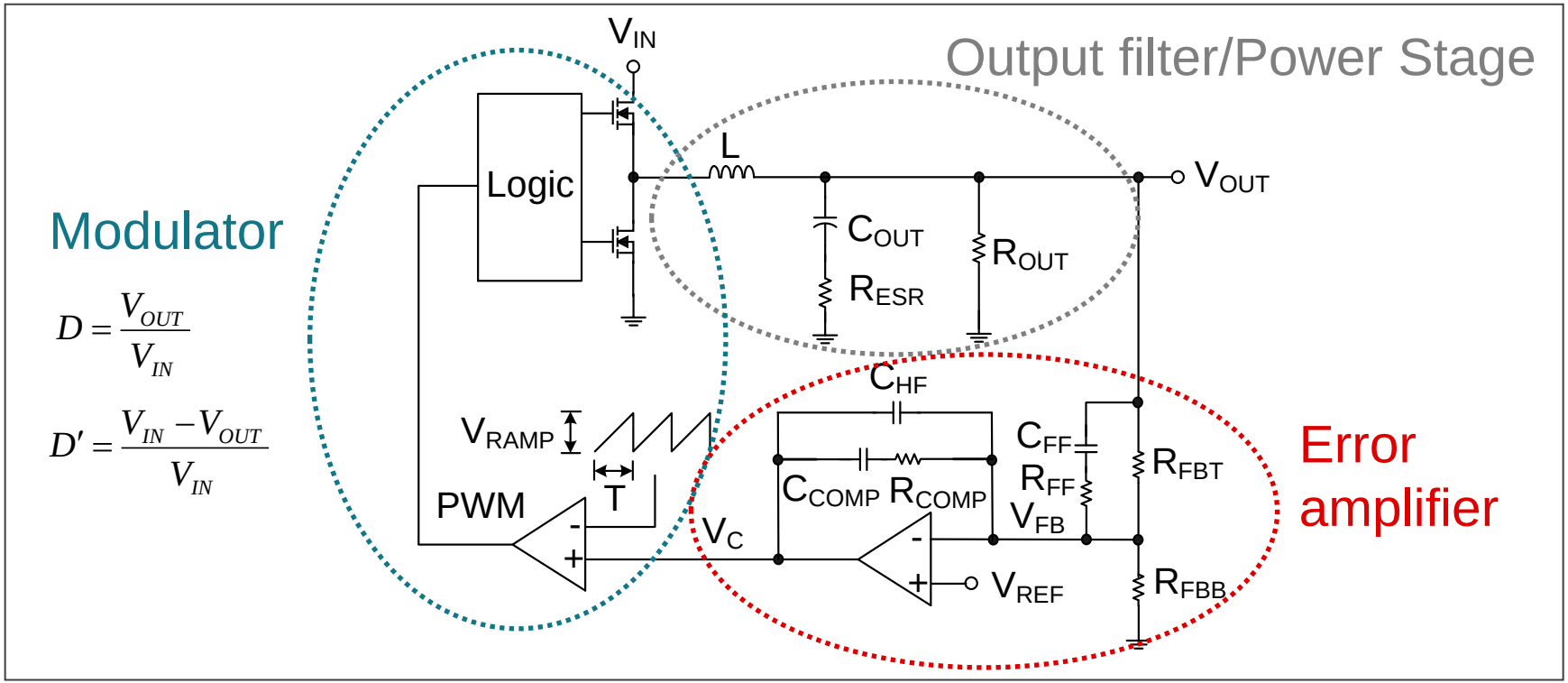
Power Supply Trades

- Size
- Cost
- Efficiency
- Can you have all 3?

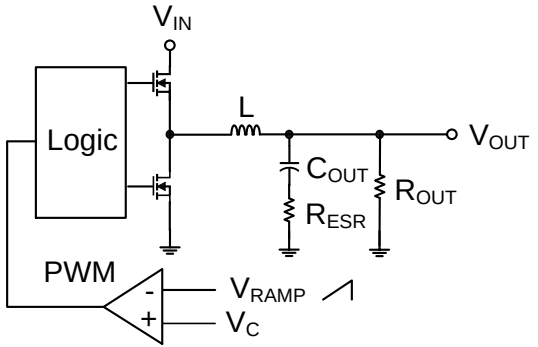
DC/DC Switch-Mode Power Supplies(SMPS)

- The end unless you want to get into the real stuff

Buck design example/discussion terms

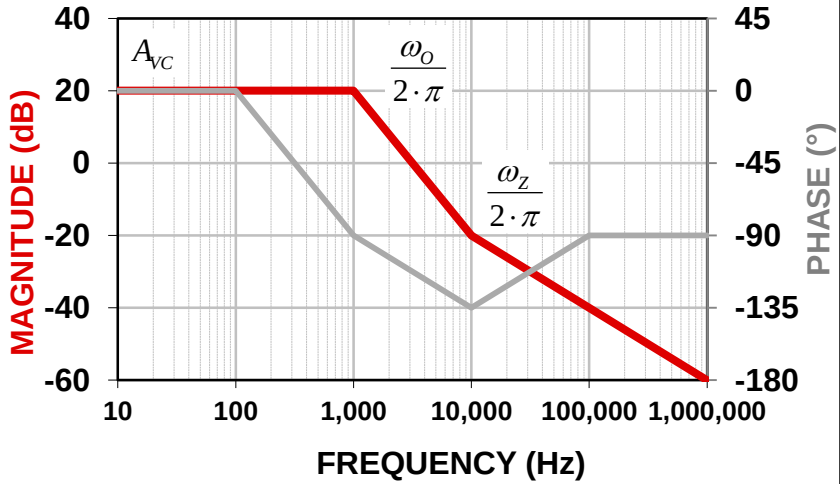


Voltage-mode buck power stage



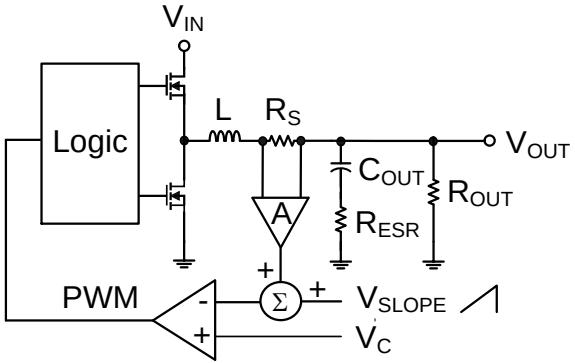
$$A_{VC} = \frac{V_{IN}}{V_{RAMP}} \qquad \omega_O = \frac{1}{\sqrt{L \cdot C_{OUT}}}$$

$$Q_O = \frac{R_{OUT}}{\sqrt{L/C_{OUT}}} \qquad \omega_Z = \frac{1}{R_{ESR} \cdot C_{OUT}}$$



$$\frac{\hat{v}_{OUT}}{\hat{v}_C} = A_{VC} \cdot \frac{1 + \frac{s}{\omega_Z}}{1 + \frac{s}{Q_O \cdot \omega_O} + \frac{s^2}{\omega_O^2}}$$

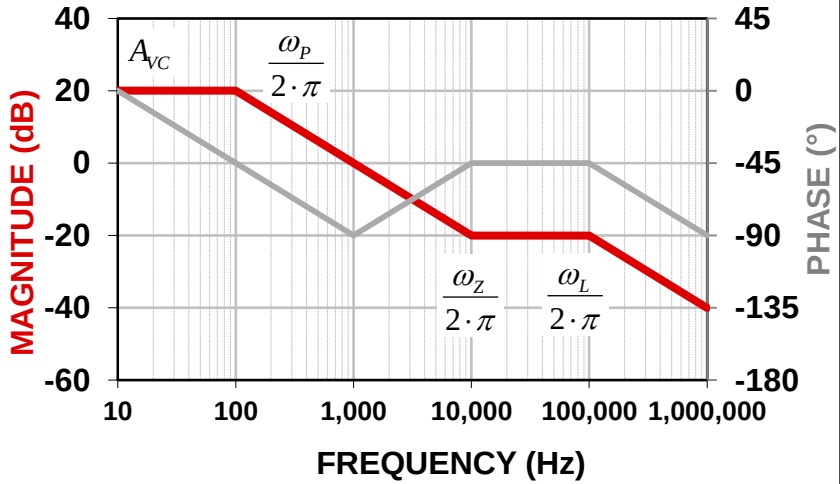
Current-mode buck power stage



$$R_i = A \cdot R_S \qquad \omega_Z = \frac{1}{R_{ESR} \cdot C_{OUT}}$$

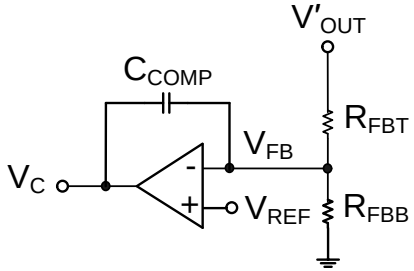
$$A_{VC} \approx \frac{R_{OUT}}{R_i} \qquad K_m \approx \frac{V_{IN}}{V_{SLOPE}} \quad \text{at D = 0.5}$$

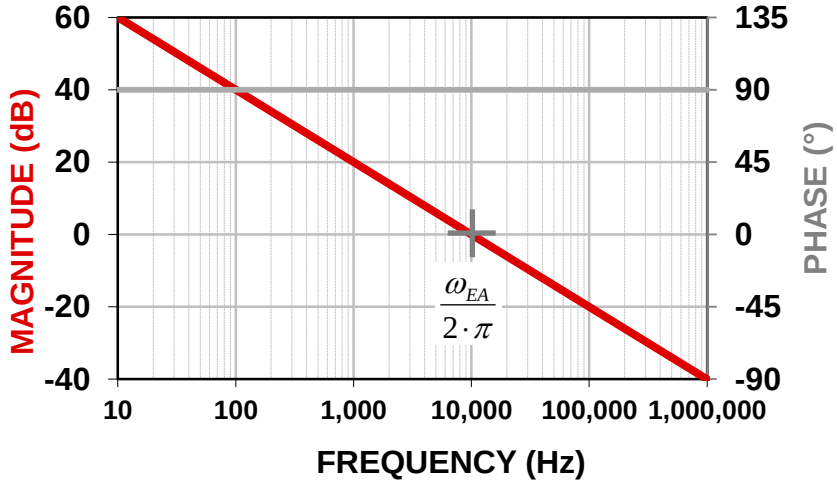
$$\omega_P \approx \frac{1}{C_{OUT} \cdot R_{OUT}} \qquad \omega_L = \frac{K_m \cdot R_i}{L}$$



$$\frac{\hat{v}_{OUT}}{\hat{v}_C} \approx A_{VC} \cdot \frac{1 + \frac{s}{\omega_Z}}{\left(1 + \frac{s}{\omega_P}\right) \cdot \left(1 + \frac{s}{\omega_L}\right)}$$

Type I error amplifier

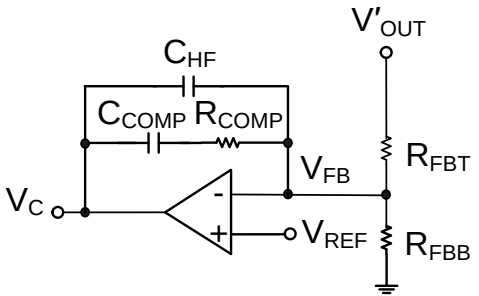




$$\omega_{EA} = \frac{1}{R_{FBT} \cdot C_{COMP}}$$

$$\frac{\hat{v}_C}{\hat{v}'_{OUT}} \approx -\frac{\omega_{EA}}{s}$$

Type II error amplifier

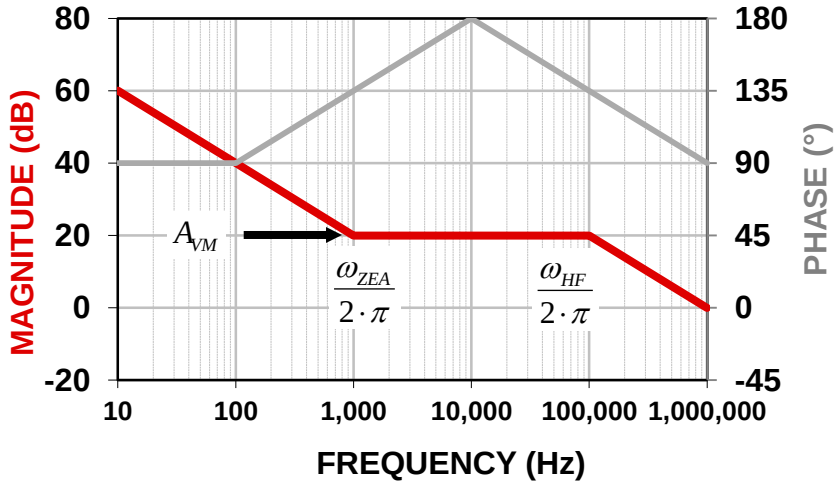


$$A_{VM} \approx \frac{R_{COMP}}{R_{FBT}}$$

$$\omega_{ZEA} = \frac{1}{R_{COMP} \cdot C_{COMP}}$$

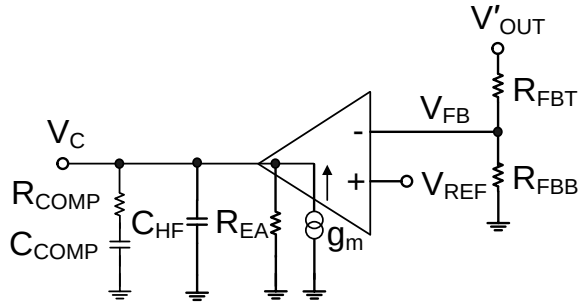
$$\omega_{HF} \approx \frac{1}{R_{COMP} \cdot C_{HF}}$$

Assumption: $C_{COMP} >> C_{HF}$



$$\frac{\hat{v}_C}{\hat{v}'_{OUT}} \approx -A_{VM} \cdot \frac{1+\frac{\omega_{ZEA}}{s}}{1+\frac{s}{\omega_{HF}}} \approx -\frac{A_{VM} \cdot \omega_{ZEA}}{s} \cdot \frac{1+\frac{s}{\omega_{ZEA}}}{1+\frac{s}{\omega_{HF}}}$$

Type II transconductance amplifier

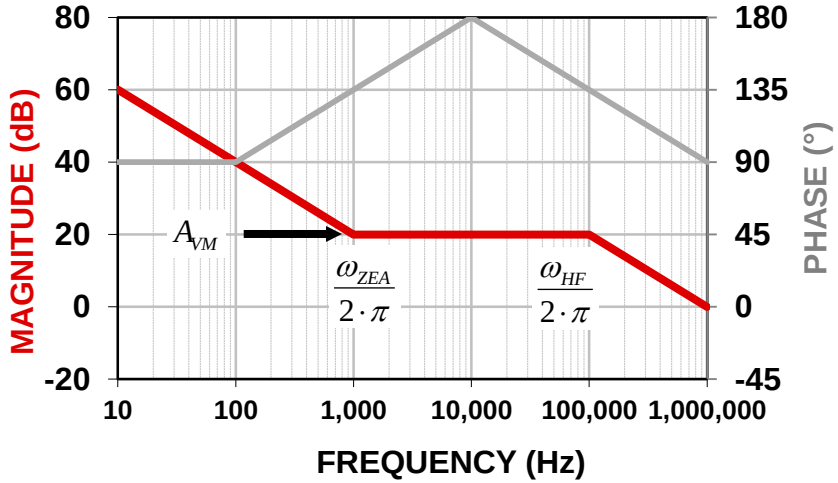


$$A_{VM} = K_{FB} \cdot g_m \cdot R_{COMP}$$

$$\omega_{ZEA} = \frac{1}{R_{COMP} \cdot C_{COMP}} \qquad K_{FB} = \frac{R_{FBB}}{R_{FBB} + R_{FBT}}$$

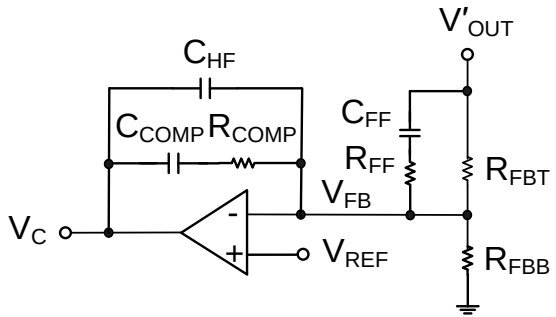
$$\omega_{HF} \approx \frac{1}{R_{COMP} \cdot C_{HF}} \qquad A_{OL} = g_m \cdot R_{EA}$$

Assumptions: $C_{COMP} >> C_{HF}$ & $R_{EA} >> R_{COMP}$



$$\frac{\hat{v}_C}{\hat{v}'_{OUT}} \approx -A_{VM} \cdot \frac{1 + \frac{\omega_{ZEA}}{s}}{1 + \frac{s}{\omega_{HF}}} \approx -\frac{A_{VM} \cdot \omega_{ZEA}}{s} \cdot \frac{1 + \frac{s}{\omega_{ZEA}}}{1 + \frac{s}{\omega_{HF}}}$$

Type III error amplifier

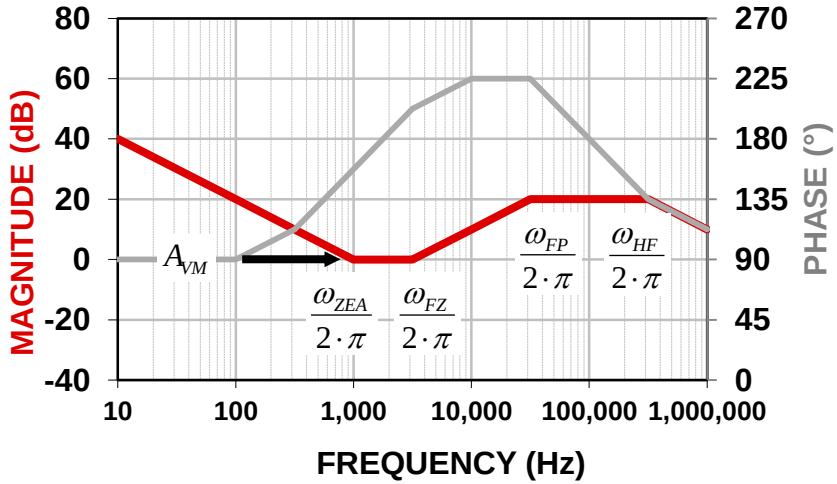


$$A_{VM} \approx \frac{R_{COMP}}{R_{FBT}}$$

$$\omega_{ZEA} = \frac{1}{R_{COMP} \cdot C_{COMP}} \qquad \omega_{FZ} \approx \frac{1}{R_{FBT} \cdot C_{FF}}$$

$$\omega_{FP} = \frac{1}{R_{FF} \cdot C_{FF}} \qquad \omega_{HF} \approx \frac{1}{R_{COMP} \cdot C_{HF}}$$

Assumptions: $C_{COMP} >> C_{HF}$ & $R_{FBT} >> R_{FF}$

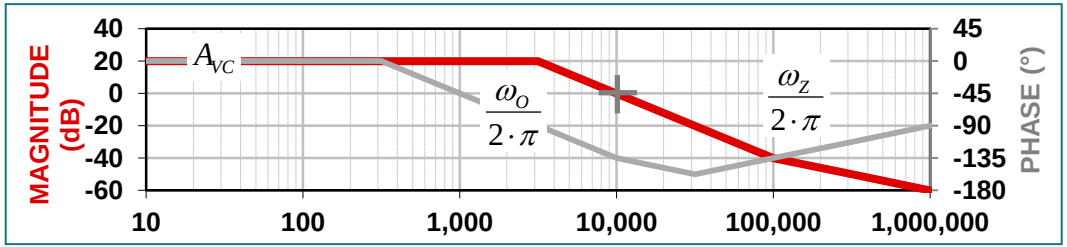


$$\frac{\hat{v}_C}{\hat{v}'_{OUT}} = -A_{VM} \cdot \frac{\left(1+\frac{\omega_{ZEA}}{s}\right)\cdot\left(1+\frac{s}{\omega_{FZ}}\right)}{\left(1+\frac{s}{\omega_{FP}}\right)\cdot\left(1+\frac{s}{\omega_{HF}}\right)} = -\frac{A_{VM}\cdot\omega_{ZEA}}{s} \cdot \frac{\left(1+\frac{s}{\omega_{ZEA}}\right)\cdot\left(1+\frac{s}{\omega_{FZ}}\right)}{\left(1+\frac{s}{\omega_{FP}}\right)\cdot\left(1+\frac{s}{\omega_{HF}}\right)}$$

Buck design example

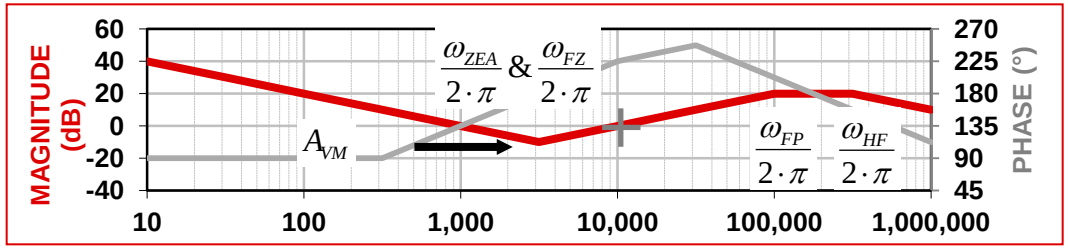
Power stage

$$\frac{\hat{v}_{OUT}}{\hat{v}_C} \approx A_{VC} \cdot \frac{1+\frac{s}{\omega_Z}}{1+\frac{s}{Q_O \cdot \omega_O}+\frac{s^2}{\omega_O^{\ 2}}}$$



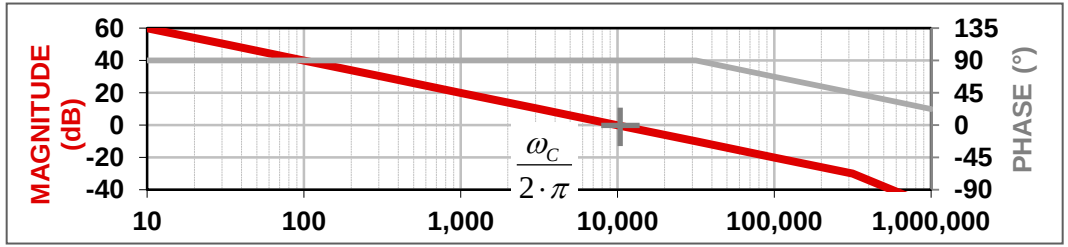
Error amplifier

$$\frac{\hat{v}_C}{\hat{v}'_{OUT}} \approx -A_{VM} \cdot \frac{\left(1+\frac{\omega_{ZEA}}{s}\right)\cdot\left(1+\frac{s}{\omega_{FZ}}\right)}{\left(1+\frac{s}{\omega_{FP}}\right)\cdot\left(1+\frac{s}{\omega_{HF}}\right)}$$



Control loop

$$\frac{\hat{v}_{OUT}}{\hat{v}'_{OUT}} = \frac{\hat{v}_{OUT}}{\hat{v}_C} \cdot \frac{\hat{v}_C}{\hat{v}'_{OUT}}$$



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3) Feedback in the Fast Lane Modeling Extending Current-Mode Control in High Frequency Converters by Brian Lynch, Texas Instruments
4) Switch-mode power converter compensation made easy – by Robert Sheehan and Louis Diana
5) How to avoid design problems by using worst case analysis calculations by Louis Diana \\corpserv\public\FAESummit\Analog\ID3.MP4