“Signal Integrity and Routing Considerations for High Speed Systems"

Graham Smith
Electrical/Signal Integrity Manager, TE Connectivity

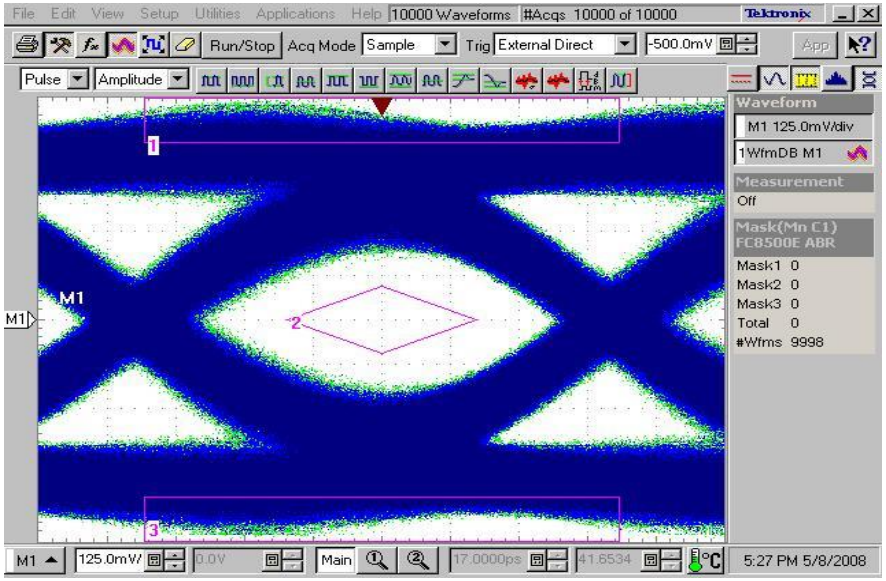
Presentation Overview

- Printed Circuit Board (PCB) Footprint Region Overview including definitions and terminology.
- Via Topics
  - Via types, sizes, market trends
  - Via stub and effects mitigation techniques
  - Via Designs for Balance and Via designs for noise improvement
- Antipad Topics
  - Traditional Antipad Designs
  - Nub-in Implementations
  - Non symmetric Antipad Considerations
- Trace Routing Topics
  - Routing Considerations
  - Layer Specific Routing
  - Deviations from “Straight Path Routing”
  - Routing and Antipad trade-offs

High Speed Systems Overview

- Pushing the envelope for faster data rates is a continuous process with evolving technologies, strategies, and techniques.

- For example, In 2005, 3.125 GBPS was a typical high speed data rate, today, 10GBPS is a norm in the industry, and migration to 25 GBPS is already being used in various industry segments.

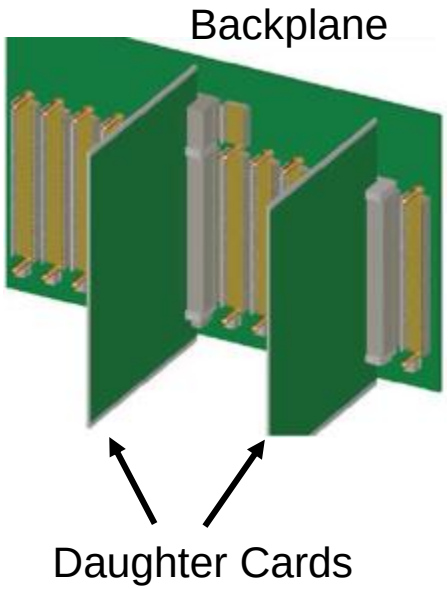


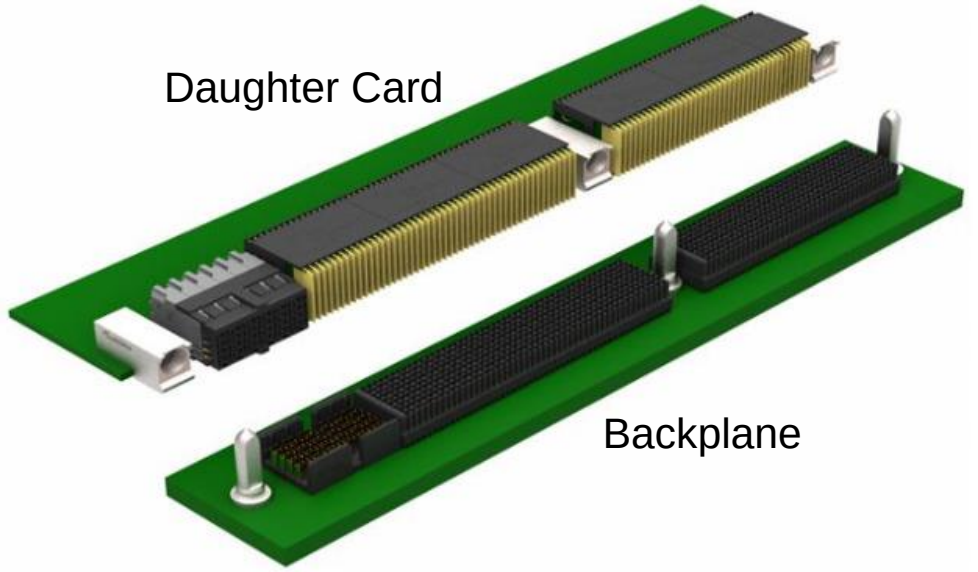
Typical High-Speed Eye Pattern

High Speed Systems Overview (cont)

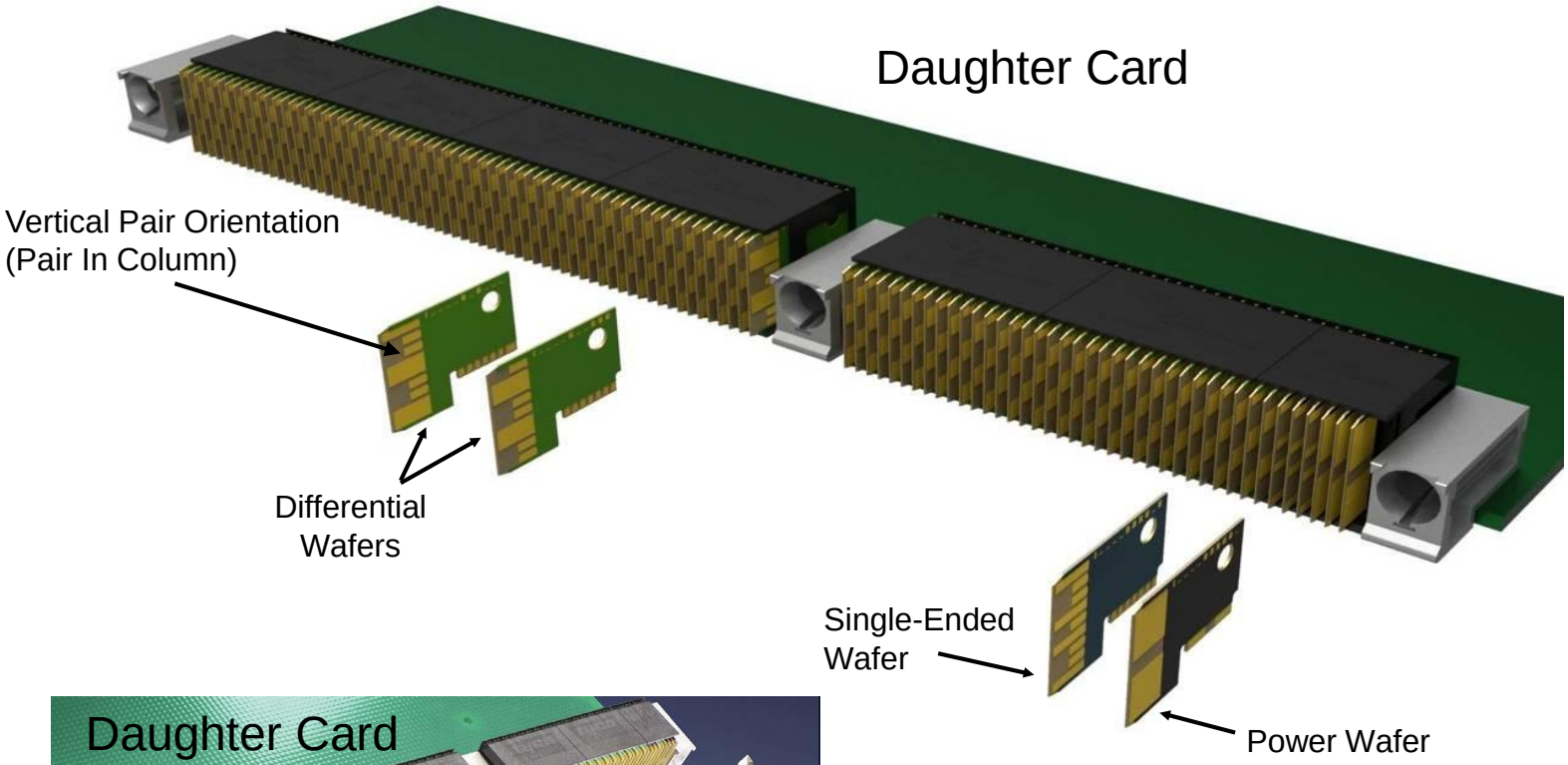
- There are various components to a channel including silicon, the board routes on both the backplane and daughter cards, as well as the interconnects (mated connector) and corresponding footprints.

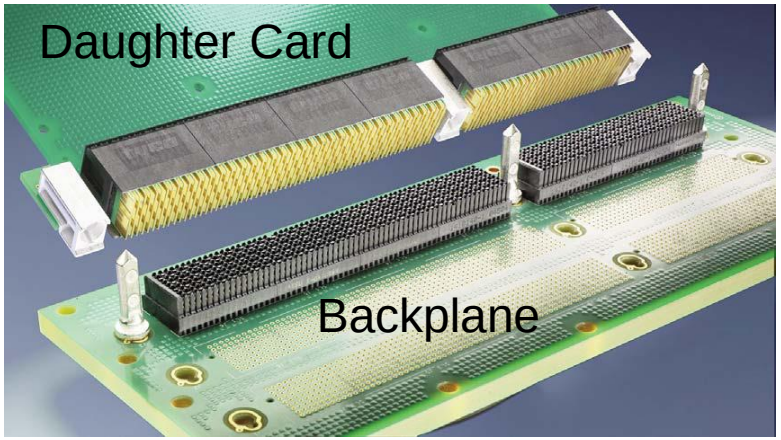
- At high data rates, the connector “board footprint” region can be just as critical as the mated connector itself.

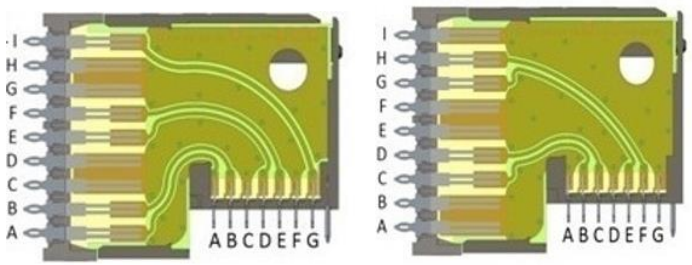




Sample Backplane Connector Construction



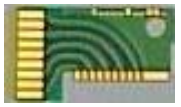




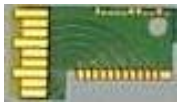
Wafer Chicklets

Example Wafer Options Include:

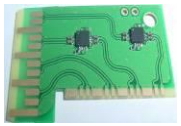
Differential Wafer



Open Pinfield (OPF) Wafer

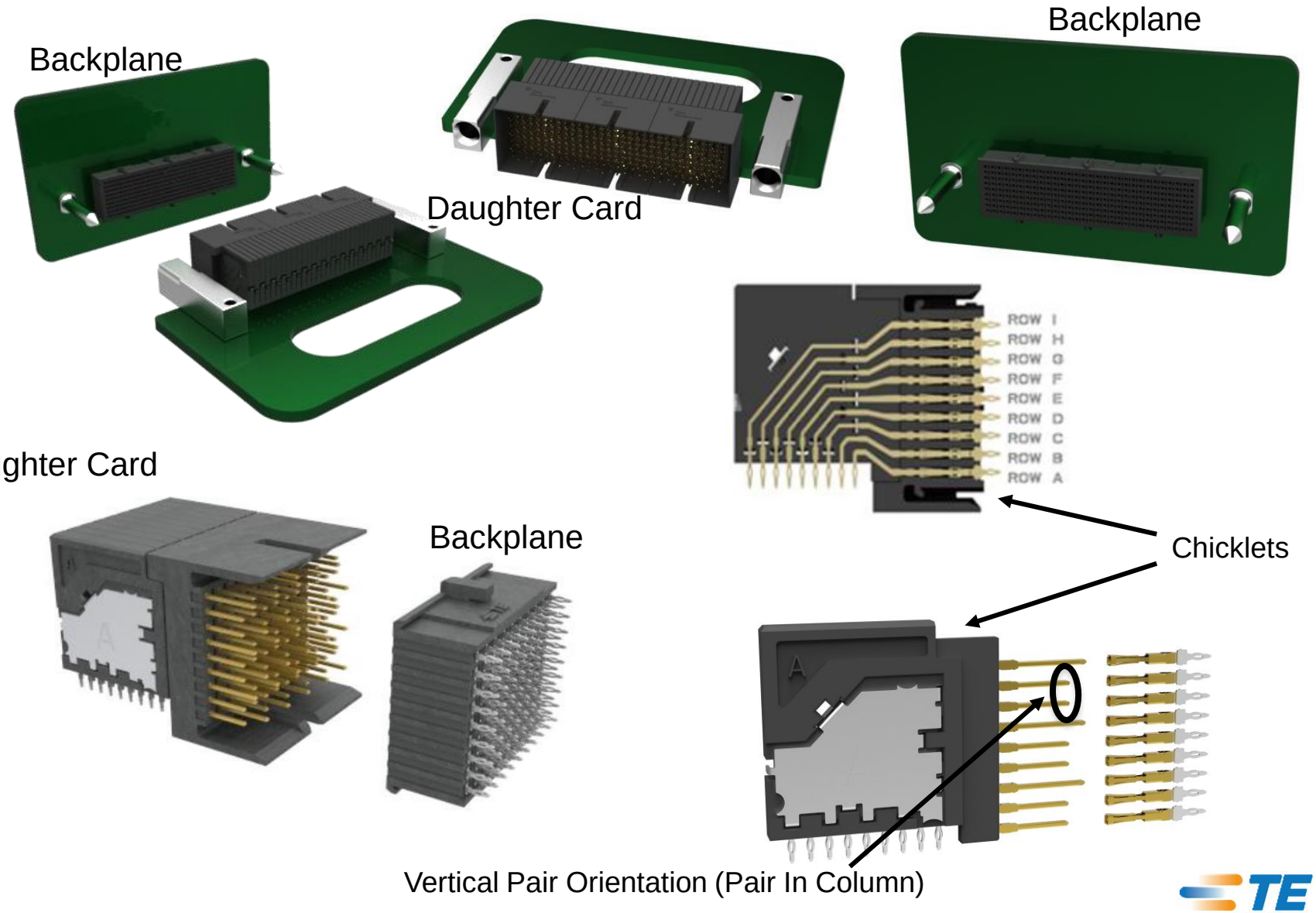


Single-Ended Wafer



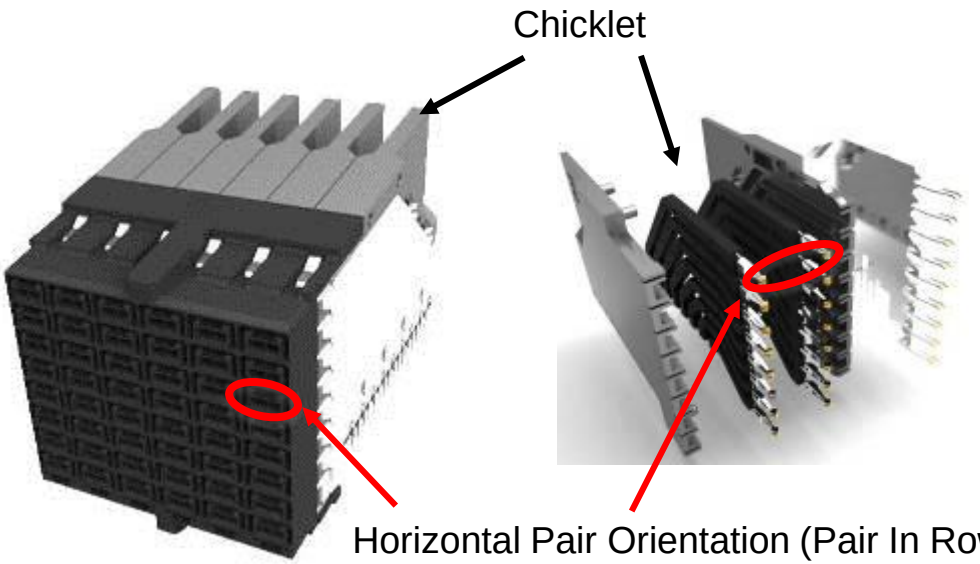
Custom Wafer

Sample Backplane Connector Construction (cont)

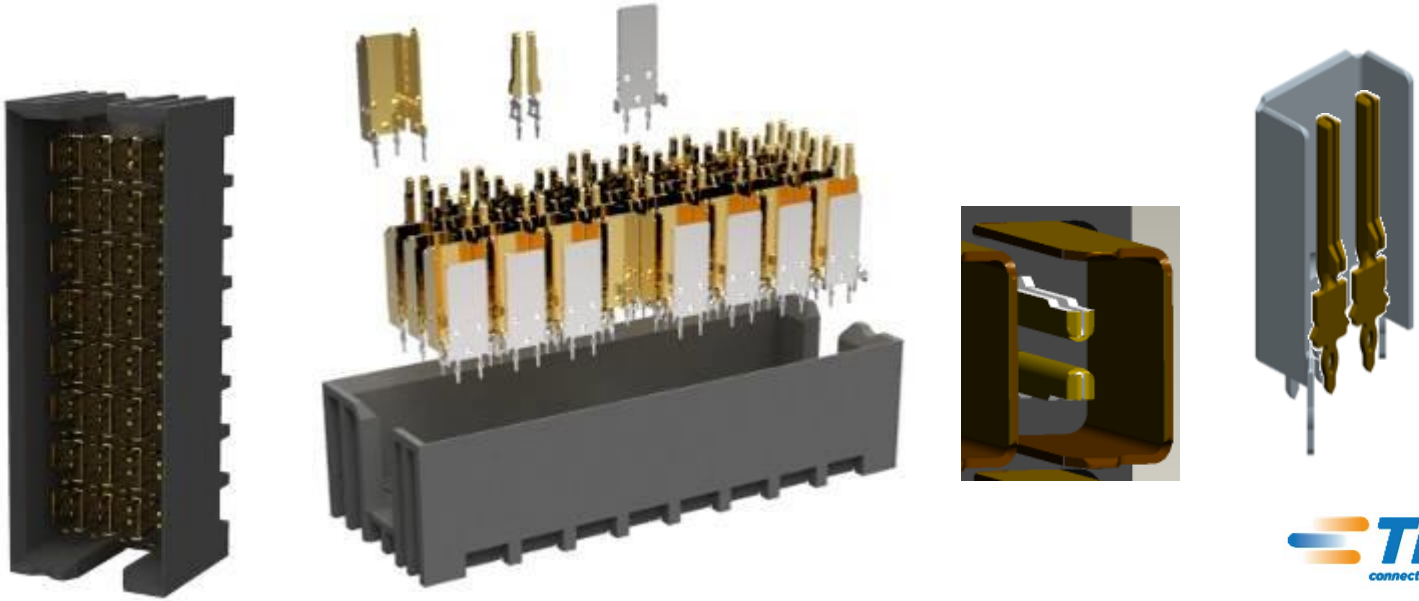


Sample Backplane Connector Construction (cont)

Daughter Card



Backplane



PCB Terminology, Definitions and Overview (cont)

- PCB material properties are also a critical part of the system with two main PCB parameters.
  - Dielectric Constant (Dk)
  - Loss Tangent or Dissipation Factor (Df)

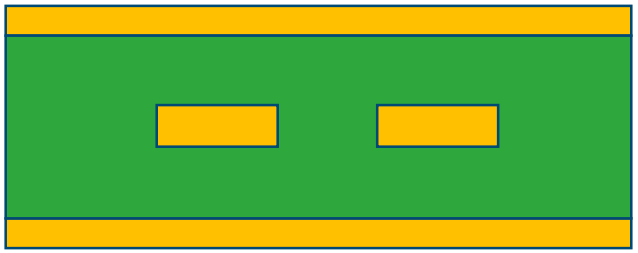
- Most PCB companies offer both low and high speed materials.
  - Typical “Low Speed” materials are of the FR-4 variety.
    - <5GBPS
  - Typical “High Speed” materials would include Nelco 4000-13EP® or –SI or Megtron6.
    - 5GBPS-25GBPS
  - Typical “Very High Speed” materials would include Rogers composite materials.
    - 56GBPS+

PCB Terminology, Definitions and Overview (cont)

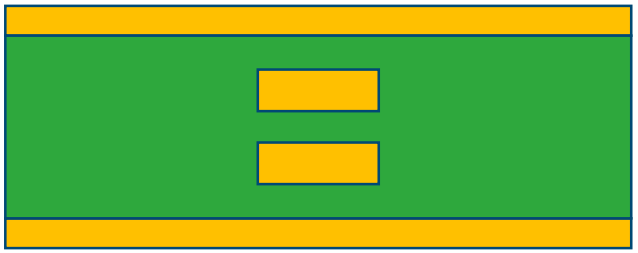
- The Dielectric Constant (Dk) of a material is a key driver in the capacitive coupling between conductors and consequently contributes to the impedance calculations of a system board.
  - Low speed Dk values can be in the 3.9-4.4 range. High speed are typically 3.3-3.6 and very high speed materials can be in the sub 3.0 range and even down in the mid 2's.
- The Loss Tangent contributes primarily to the loss of a system board.
  - Df values can vary greatly from .04 for basic FR4 materials down to .002 or lower for "High Speed" and "Very High Speed" products.

PCB Terminology, Definitions and Overview Summary

- Multilayer routing is required in most high speed backplane designs and with tight footprint densities the only viable options are edge coupled stripline and broad side coupled stripline with differential routing.



Edge Coupled Stripline



Broadside Coupled Stripline

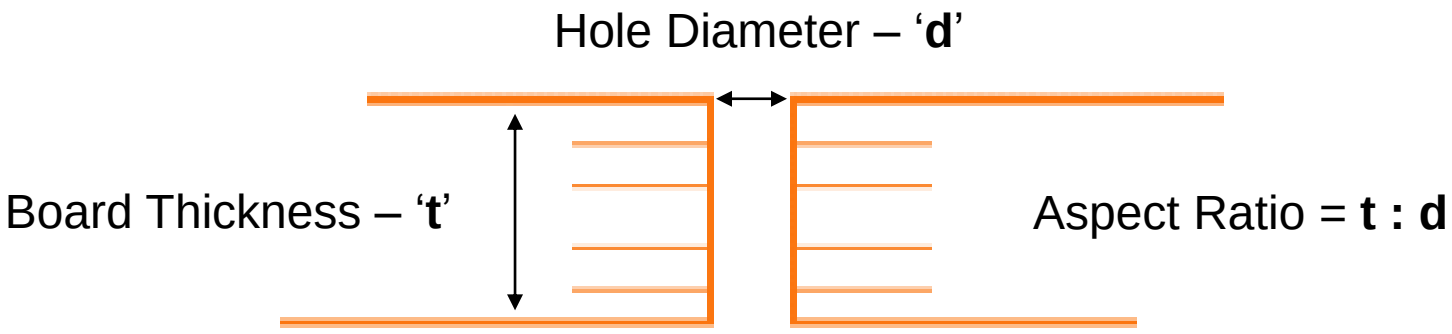
- Broadside coupled stripline requires additional layers since the signal routing is on two layers versus one.
- Broadside coupling is prone to issues with layer registration and is not a viable option for the higher speeds. Mis-registration severely impacts impedance.

PCB Terminology, Definitions and Overview Summary

- Balancing cost and performance is a challenge for our customers.
  - Performance requirement for high speed systems do not permit the use of standard FR4 due to the higher Dk and Df.
    - Higher Dk yields undesired coupling and lower impedances; High Df is lossy
  - High performance Rogers material, although it has superior performance, can be cost prohibitive.
  - Balancing cost and performance, many customers are using Megtron6 or Nelco4000-13EP® for production boards in current high speed system designs.

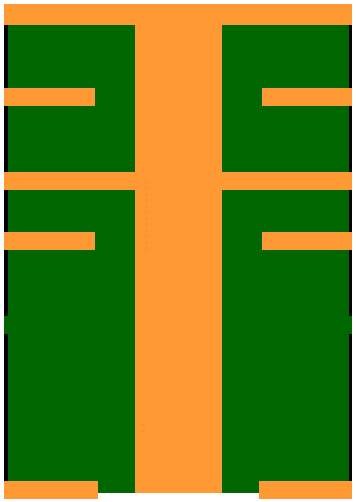
Via Types and Overview

- A key concern in via drilling capability is aspect ratio. The aspect ratio is the ratio of the board thickness to drill diameter. Practically speaking, aspect ratios are limited to approximately 12:1. Connector Footprint drilled holes must follow these constraints.

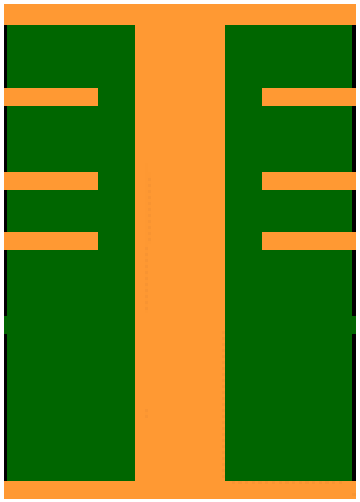


Via Types and Overview (cont)

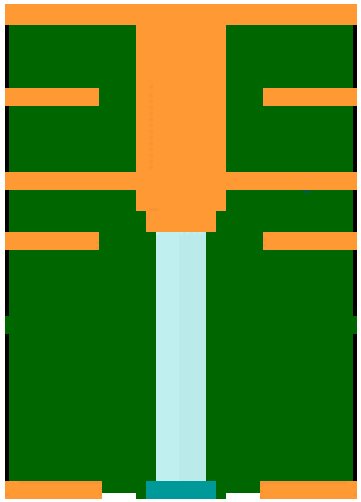
- PCB technologies allow for a variety of via types in board designs. Each via type is used for a variety of effects in a design. Several via types are illustrated below along with their pros and cons on the next page.



Drilled Thru Via



Drilled Thru Via (bottom route)



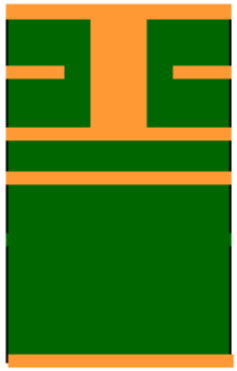
Back-drilled Thru Via

Via Types and Overview (cont)

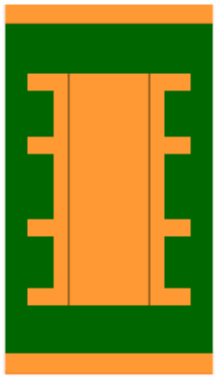
- All three via types on the previous slide involve a straight “drill through” technology.
  - Drill thru via is the simplest and although the least costly; can leave a significant stub below the trace layer which has unwanted stray capacitance and will degrade the signal.
  - Drilled thru bottom route is also simple, but is used less often; stripline designs frequently use the top and bottom layers as ground references.
  - Back-drilled thru via, commonly used via in high speed system cards, adds cost, but limits the back-drilled stub to 8-20 mils.

Via Types and Overview (cont)

- More Complex Via types:



Blind Via



Buried Via

Laser Drilled Micro Via

- Each of the illustrated complex via types has pros and cons. These are noted on the next slide.

Via Types and Overview (cont)

- Blind Via
  - Blind Vias have no drill continuation for area below the drill, consequently extra real estate is available below the drill.
  - Blind Vias have added cost due to multiple process operations.
- Buried Via
  - Buried Vias have no drill continuation for area above or below the drill, consequently extra real estate is available above and below the drill.
  - Buried Vias also have added cost due to multiple process operations and external via access does not exist.
- Laser Drilled Micro Via
  - Laser Drilled Micro Vias can be very small in high density designs, and also have no drill continuation for area below the drill.
  - Laser drilled Micro Vias also have added cost due to multiple process operations, and have a limited aspect ratio and limited overall depth.

Via Types and Overview (cont)

- Dual Diameter Via:

Dual Diameter Via

Dual Diameter Via Pros and Cons

- Dual Diameter Vias have a large upper area to accommodate a connector Eye of Needle (EON).
- Dual Diameter Vias have a reduced diameter lower section-- reduced noise coupling and potentially better impedance matching in footprint region.
- Dual Diameter Vias have added cost due to the secondary drilling operation.

Via Types and Overview (cont)

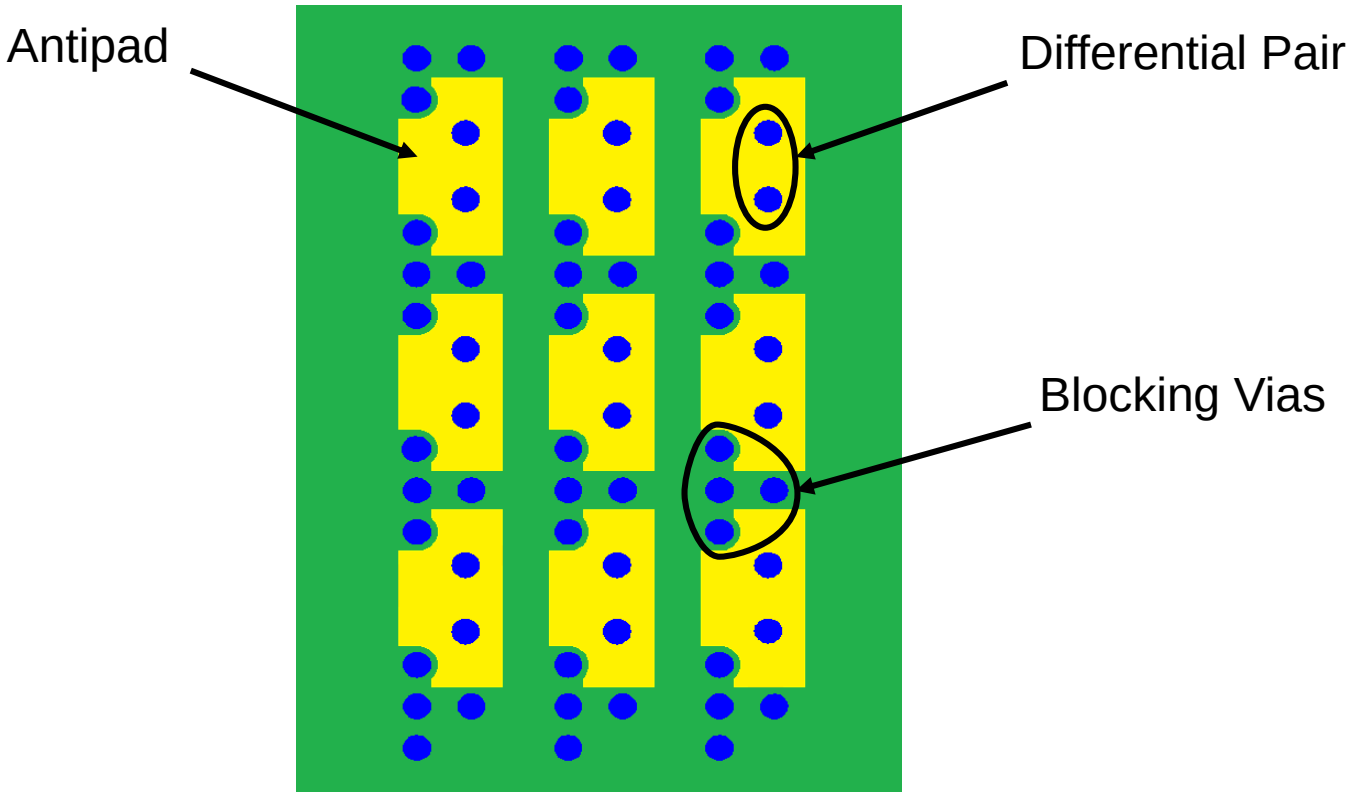
- Drill sizes for connector footprints have both electrical routing considerations as well as mechanical retention considerations-- Trade offs exist between larger size for mechanical benefit versus smaller for improved signal density while maintaining impedance matching.

- Trade offs in the cost and performance arena are considered by customers when choosing via types--Each via can be selected for different purposes/reasons as noted, but choices are also driven by the process capability.

- For the sake of this presentation, the primary vias to be considered are thru via, backdrilled via, and dual diameter vias. The majority of customers designing high speed backplanes are using the drilled thru technology with back-drilling.

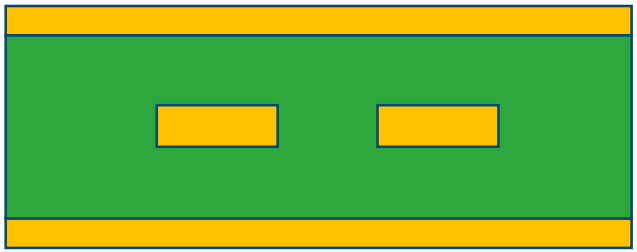
Via Types and Overview (cont)

- Although a vias primary purpose is to provide multi-layer interconnect capability and connector interface, they can also be used to alleviate cross talk. The illustration below shows how ground layer blocking vias help remediate cross talk between signal vias.



Antipad Considerations

- As illustrated before and shown below, trace layer routes in a stripline configuration dictate that the ground planes above and below the trace layer are part of the overall transmission line.



- When signals arrive at the signal pads at the vias, the ground layers must maintain clearance from the signal barrel. This clearance is called the anti-pad region. The next few slides will discuss anti-pads.

Antipad Considerations

- Anti-pad designs consist of trade-offs between capability and performance parameters. Illustrations follow on the next few slides.

  - Smaller anti-pad is close to the drill barrel and pads-- advantage is large route-out channel and smaller route-out trace to pad inside the anti-pad region.

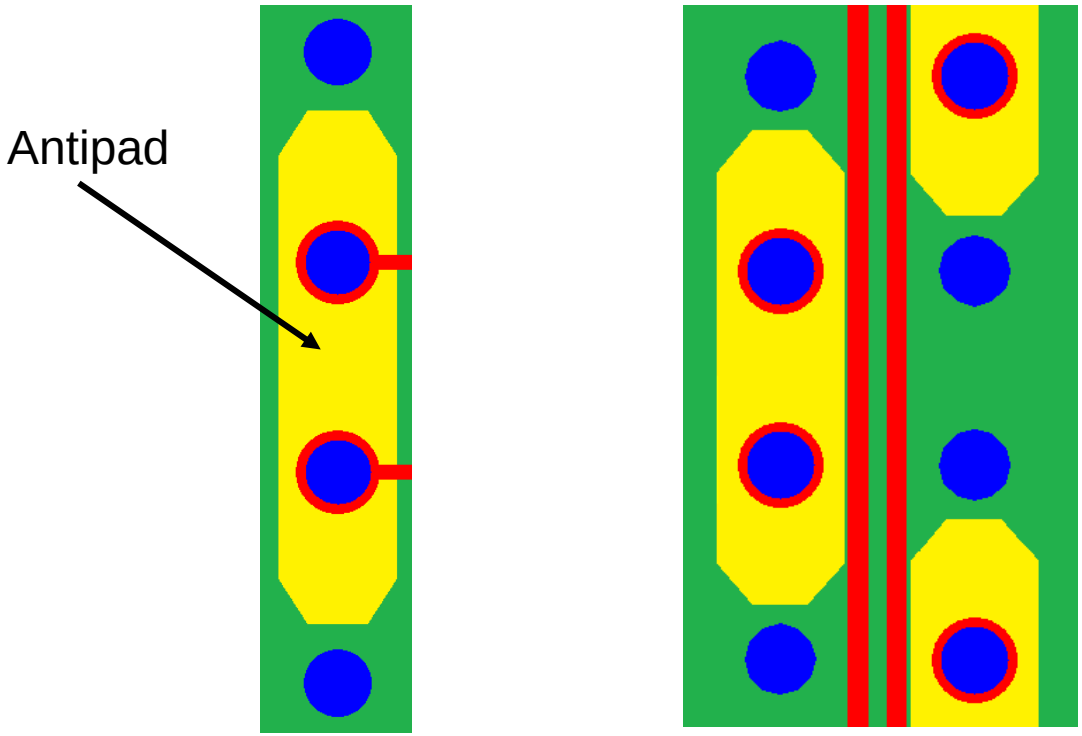
  - Disadvantage of smaller anti-pad is more coupling of via barrel and pads to ground layers—consequently, lower impedance.

  - Larger anti-pad is further from the drill barrel and pads-- advantage is reduced coupling between via barrel and pads to ground layers.

  - Disadvantages of larger anti-pad are reduced channel routing width and longer route-out traces to pad in antipad region.

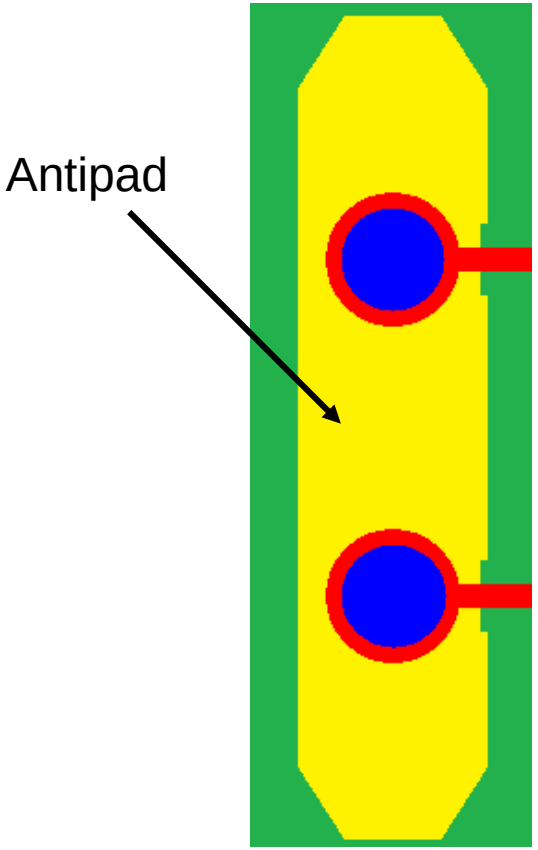
Antipad Considerations (cont)

- Typical antipad construct is shown below. The anti-pad is large enough to maintain clearance from the signal pad above and below and to prevent a low impedance from proximity of ground to barrel, but not so large as to limit channel routing or have a large route-out distance.



Antipad Considerations (cont)

- In cases when the antipad width is unconstrained by channel width and is therefore large enough that the trace route-out region is long, another anti-pad option exists called a “nub-in” design. A “nub-in” simple antipad construct is shown below.



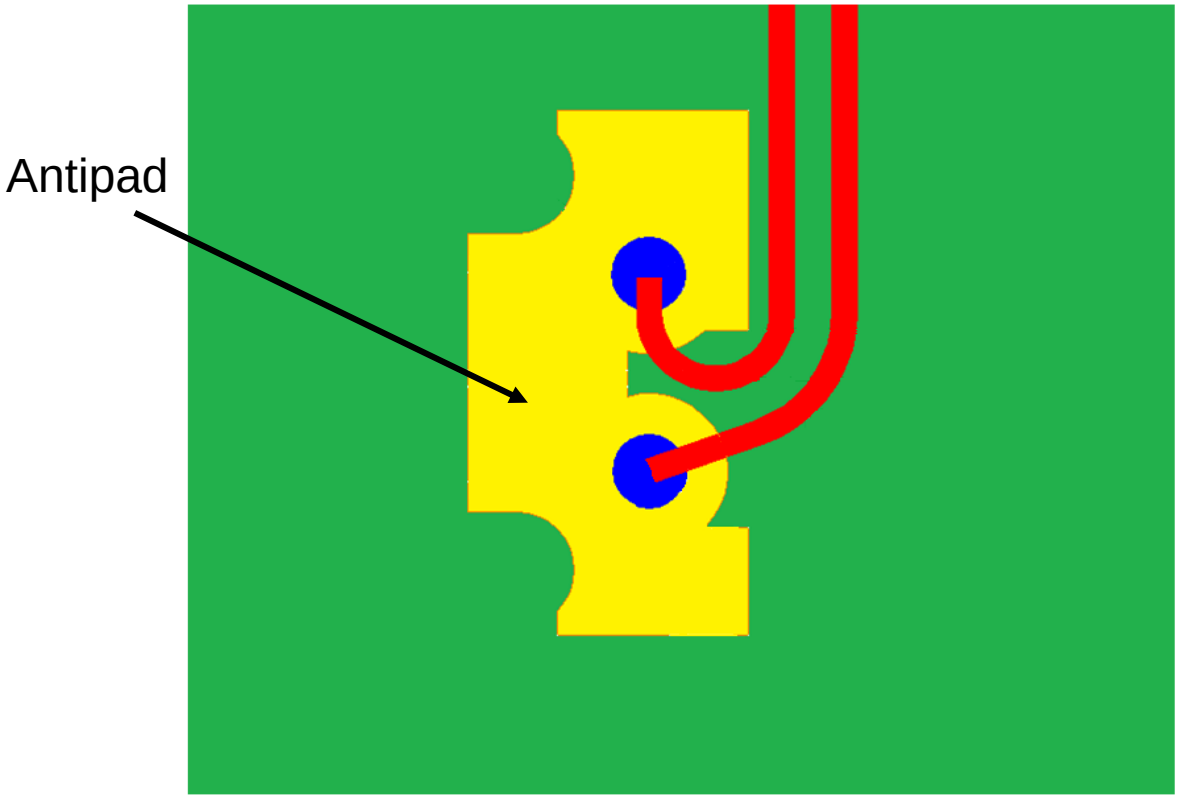
Antipad Considerations (cont)

- Note that in the simple “nub-in” design shown, the “nub-in” portion is only on the ground layers above and below the target trace layer. The ground layers beyond (above or below) the strip line ground layers have the full antipad sizing.

- The “nub-in” design limits the trace route-out “uncovered region” to 4-5 mils. It’s also good the note that the “nub-in” in-cut region is also 4-5 mils beyond the trace sides as well. These distances are good design rules to follow for high speed implementations.

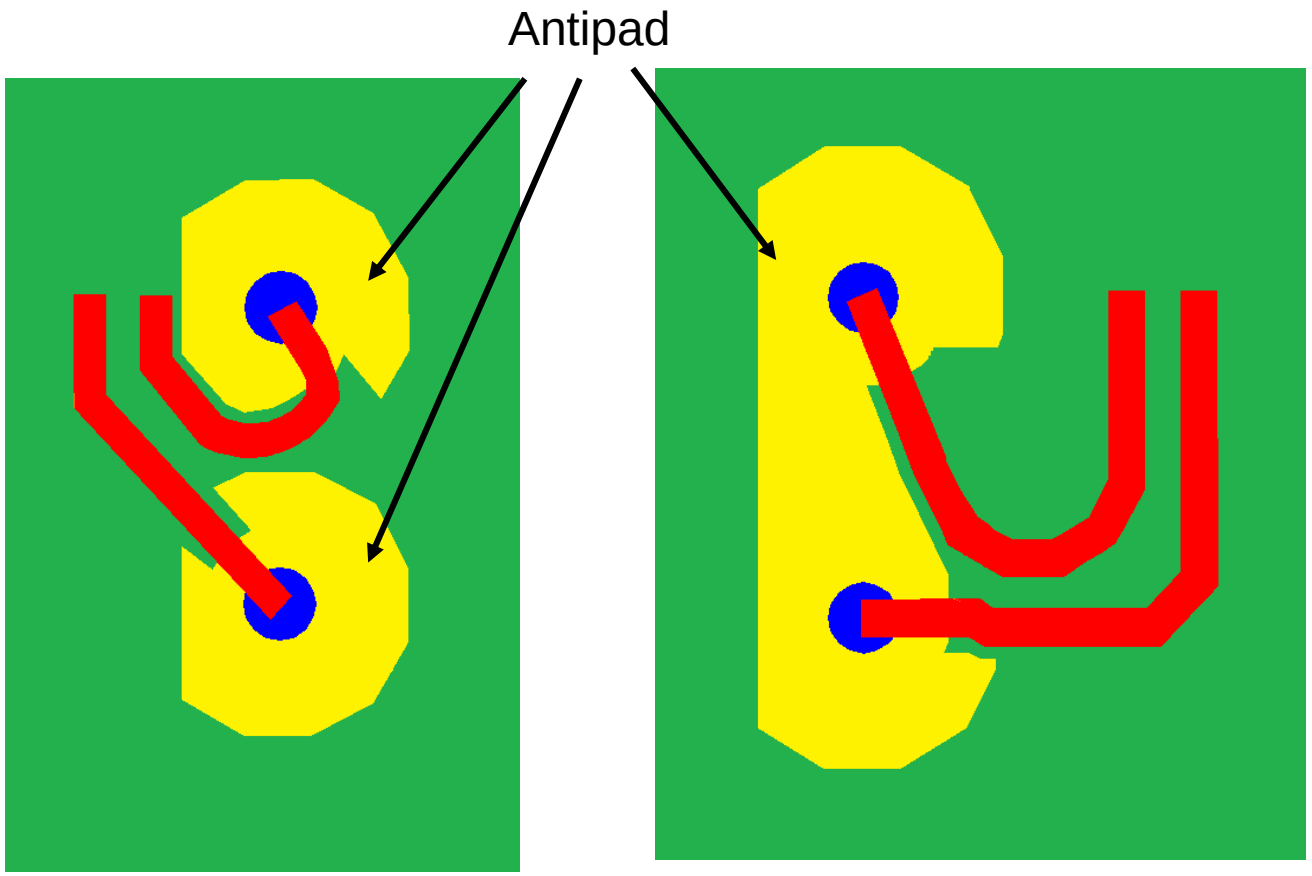
Antipad Considerations (cont)

- In cases where differential routing also requires length compensations for skew matching, alternate “nub-in” antipad designs can be considered that are non-symmetric and separated as needed. Examples of these style anti-pads are shown below:



Antipad Considerations (cont)

- More non-symmetric “nub-in” designs



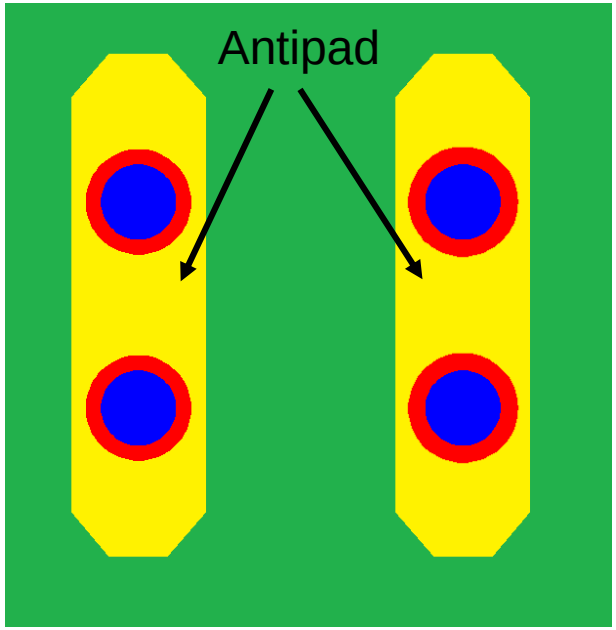
Trace Routing Considerations

- Connector footprints usually involve thru hole vias for press fit (with or without back-drilling).
  - Trace routing must work around the pin field per se and the corresponding antipads.
  - Keep-out regions must also be maintained for PCB manufacturing capability.

- The signal trace arrives at the drilled via with an “arrival pad” as noted above. The size of this pad is important to performance.
  - Pad sizes at drill plus 10-12 mils diameter are optimum while drill plus 10 mils is the smallest while ensuring a minimum annular ring.
  - Clearance from this pad to antipad was briefly discussed in the antipad section.
  - Larger pads have a detrimental effect on the signal integrity performance forcing larger antipads, increased coupling, and impedance discontinuities.

Trace Routing Considerations (cont)

- The image below shows a drill plus 10 mils in comparison to a drill plus 12 mils. The antipad was kept the same in the illustration, but the antipad for the drill plus 12 mil should grow since the pad edges are getting close to the antipad edges. A good design rule of thumb is a minimum of 5 mils clearance from pad to each antipad edge.



Drill plus 10 mils Drill plus 12 mils

Trace Routing Considerations (cont)

- As the via passes through various layers on its way to the signal layer, each non-signal layer may or may not have additional “non-functional pads”.
  - These “non-functional” pads have an adverse effect on signal integrity.
  - Some customers desire non-functional pads for mechanical via integrity reasons.

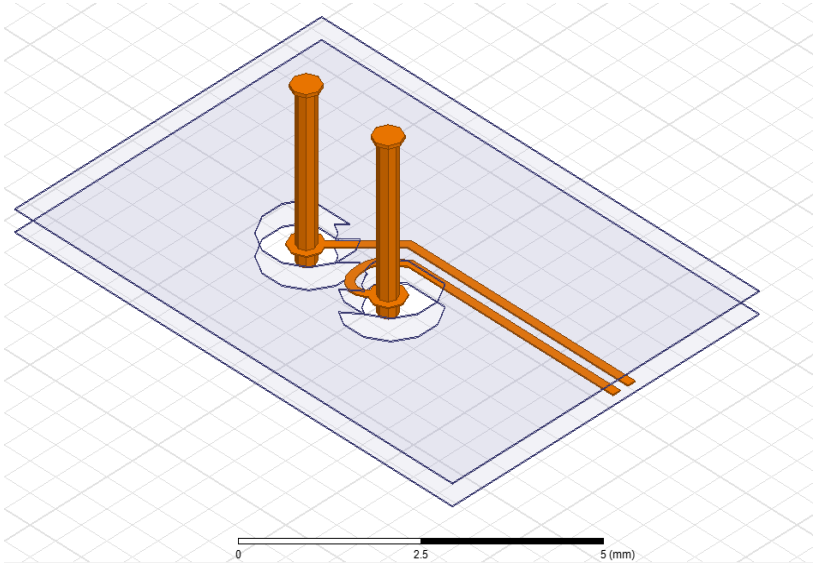
  The images below and on the next two slides shows the difference.

With Non-functional Pads Without Non-functional Pads

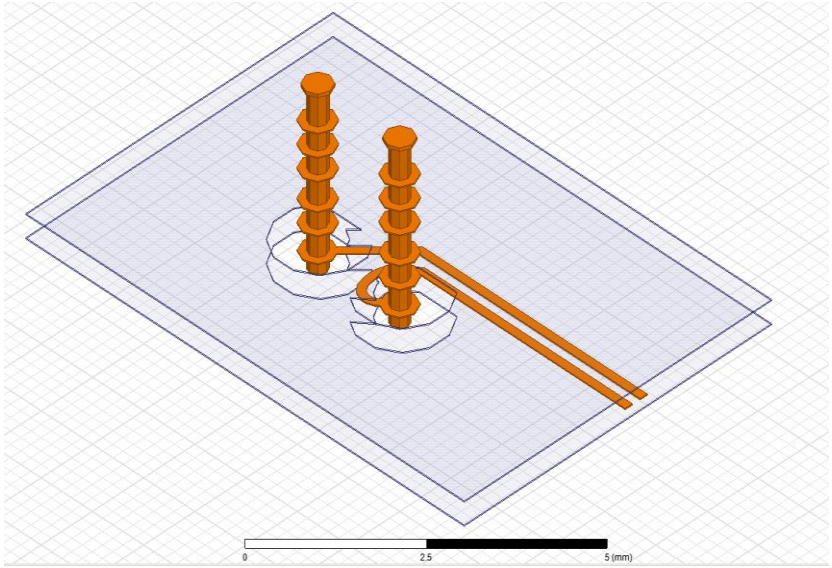
Trace Routing Considerations (cont)

Modeled Impedance Comparison with and without Non-Functional Pads

Full 3D HFSS Model

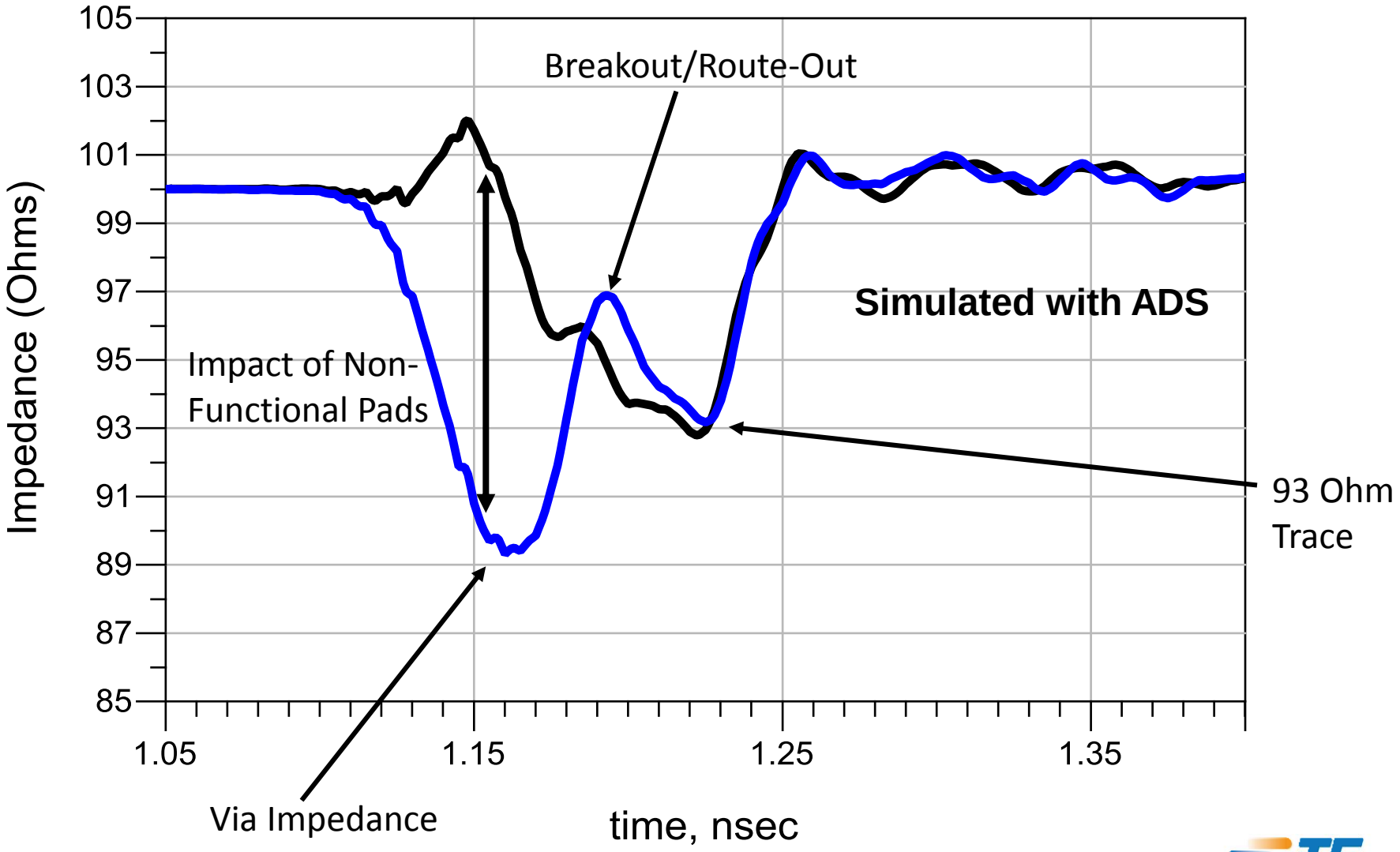


Without Non-functional Pads



With Non-functional Pads

Trace Routing Considerations (cont)



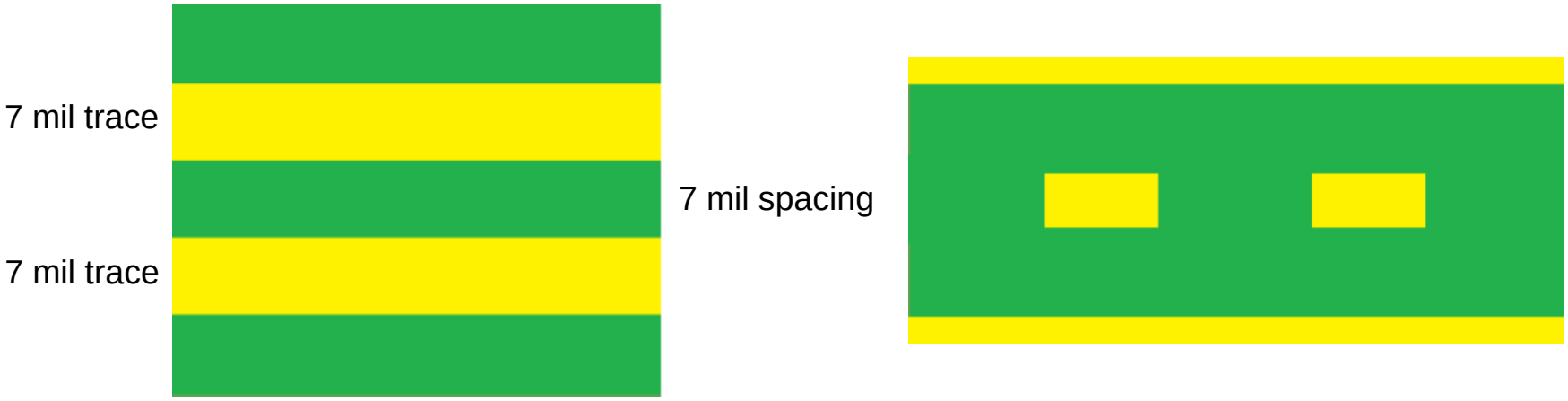
Trace Routing Considerations (cont)

- Backplane designs require longer trace routes often in excess of 10-18 inches or more. Because of this, narrow traces are less desirable on long backplane runs due to excessive copper loss.

- There are various configurations of trace widths and trace spacings for differentially routed stripline traces. A typical configuration for a backplane can be 7 mil wide traces, and 7 mil spacing between each signal as shown on the illustration on the next slide.

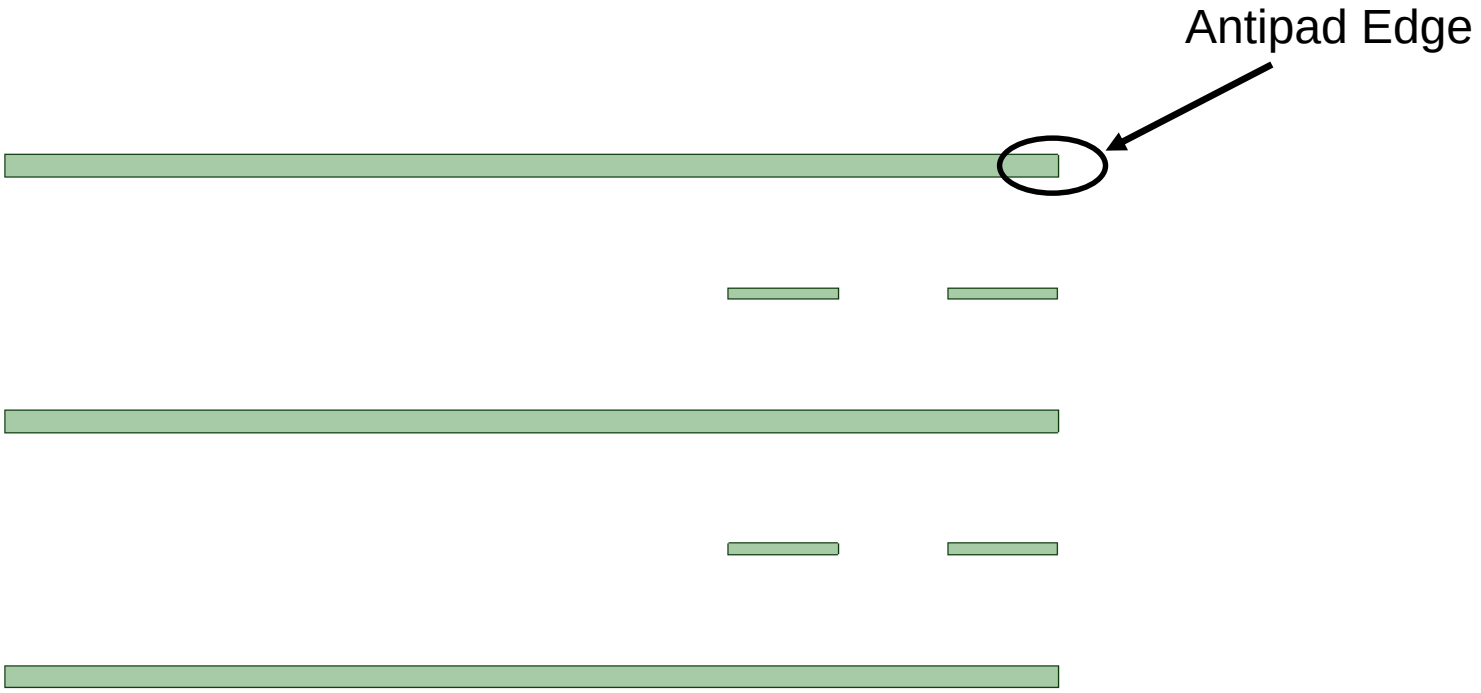
Trace Routing Considerations (cont)

- The below illustration shows the configuration for a backplane channel routing configuration with 7 mil wide traces, and 7 mil spacing between each signal trace.



Trace Routing Considerations (cont)

- Before the advent of 10GBPS data rates, differential trace routing could run right along the edge of the antipad region without much signal degradation. The image shown below illustrates this effect.

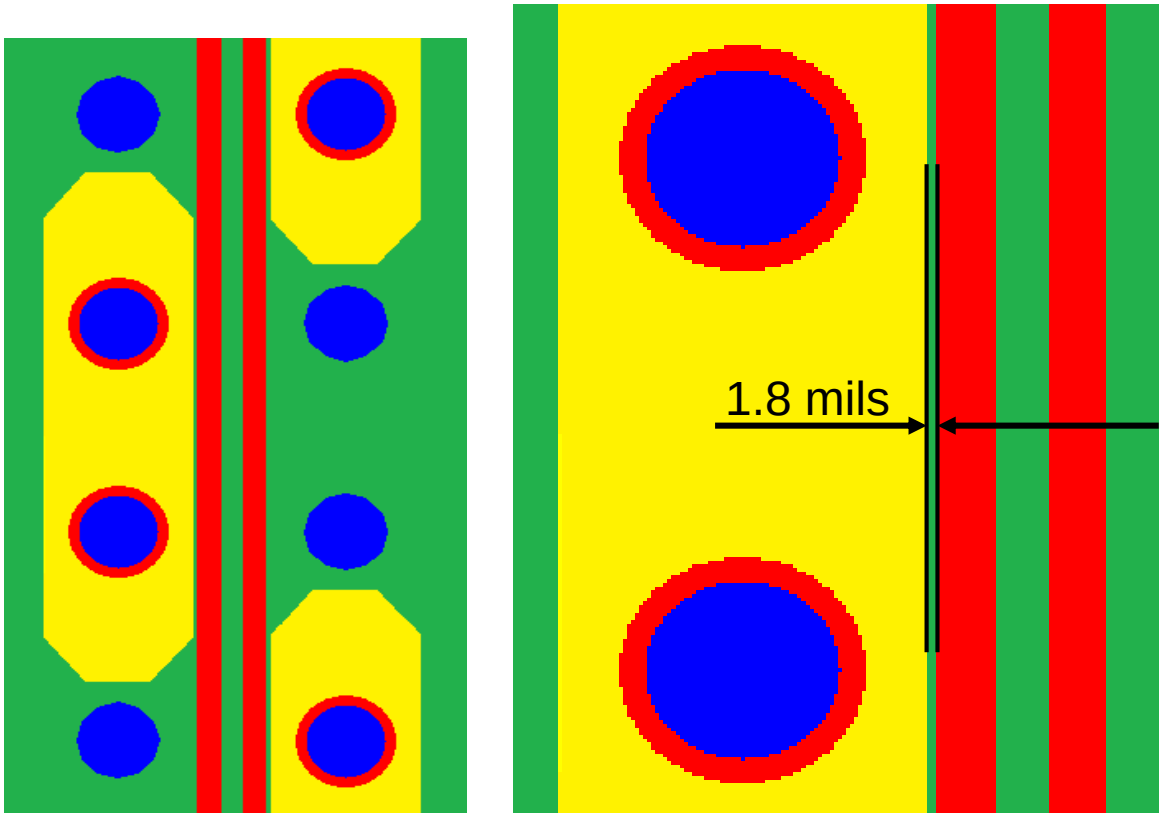


Trace Routing Considerations (cont)

- For speeds greater than 10GBPS, a clearance of 4-5 mils is desired to maintain excellent signal quality while also allowing for registration variation.
- Manufacturing capabilities also drives a minimum clearance of 8 mils from trace to ground vias. This also influences signal integrity performance.
- A case study of adapting a footprint for a connector designed originally for 3.125GBPS that is now running 10GBPS will now be visited.

Trace Routing Considerations (cont)

- Illustrated below is a 7-7-7 differential route for the TE Multigig RT2 backplane connector with a high performance drill plus 10 mil pad design, and optimized antipad sizing while meeting a min 5 mil clearance between pad and antipad edge.



Trace Routing Considerations (cont)

- The example shown is fully optimized in the pad and anti-pad region, however the 7-7-7 routing configuration only leaves a trace to anti-pad clearance of 1.8 mils on each side.

- The original design routing guide for this product was written when 3.125 GBPS was the current top speed and 6.25GBPS was just beginning to be implemented.

- The guide showed a drill plus 12-14 mil pad configuration of which the 14 mil config would have the traces right on the anti-pad edge.

- At the time, this was acceptable for these speeds, but now an alternate routing option is needed to gain clearance for the stripline trace to anti-pad.

Trace Routing Considerations (cont)

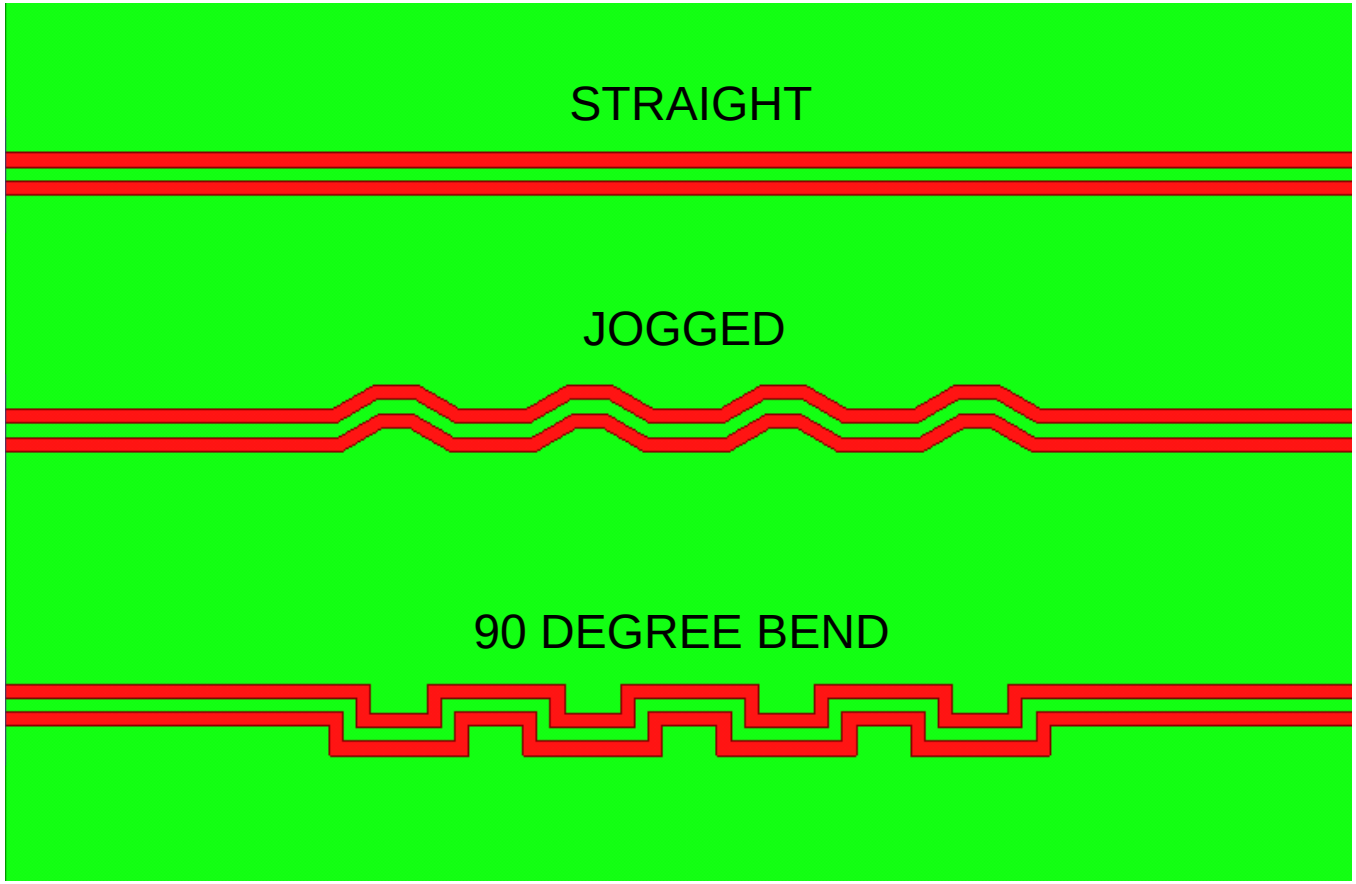
- Proposed solution-- in column trace routing that takes advantage of the double ground skip pattern and staggers the trace path.

- Since the pair of grounds between each differential pair have no anti-pads, traces can be routed closer to them while not violating the 8 mil clearance from trace to ground via.

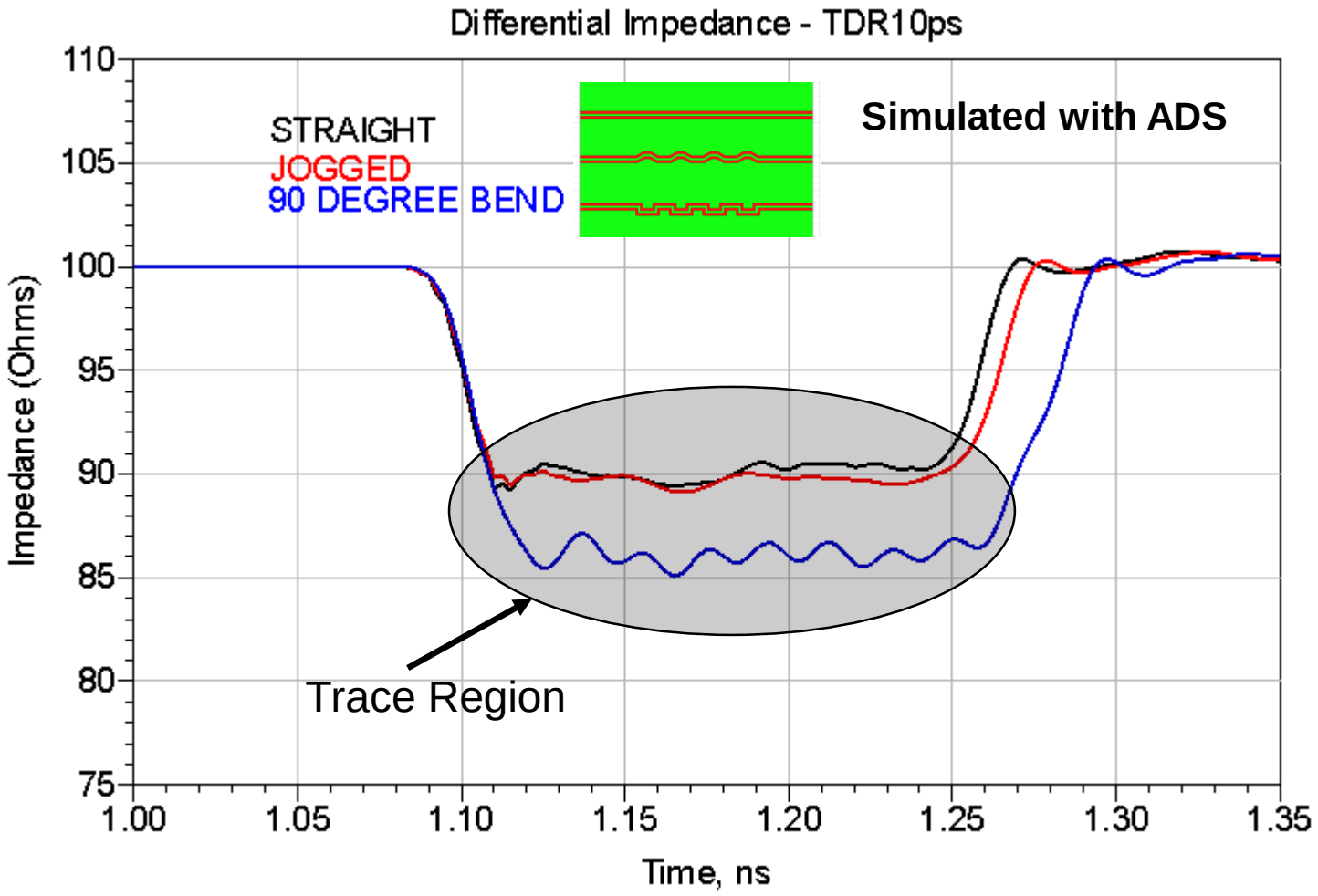
- The study shown on the next several slides illustrates signal integrity performance for three trace routing configurations. A jogged or zig-zag path is proposed as well as right angle bends.

Modeled Geometries of "Trace Only"

Three Cases Considered (Full 3D Modeled in HFSS)

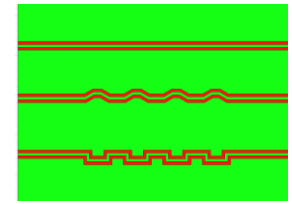


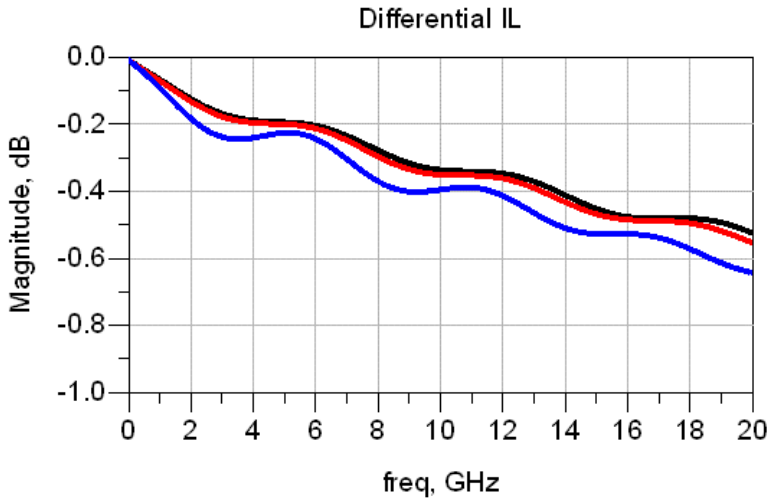
Impedance: Significant impact of 90-degree corners; 45-degree corners nearly imperceptible

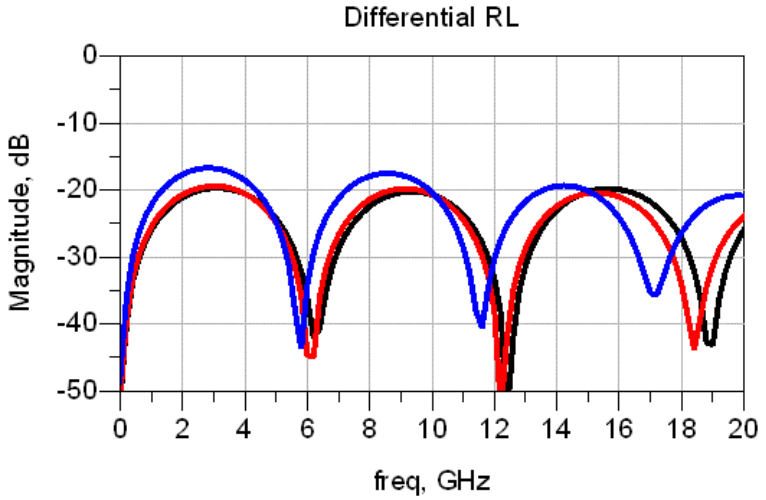


IL & RL: Significant impact of 90-degree corners; 45-degree corners nearly imperceptible

STRAIGHT
JOGGED
90 DEGREE BEND

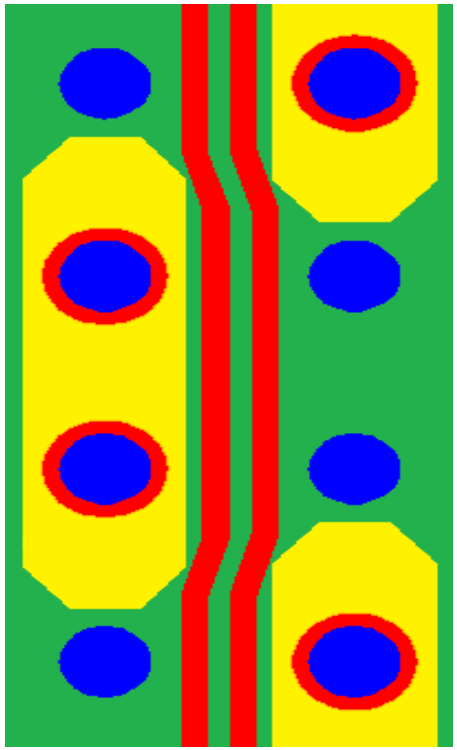


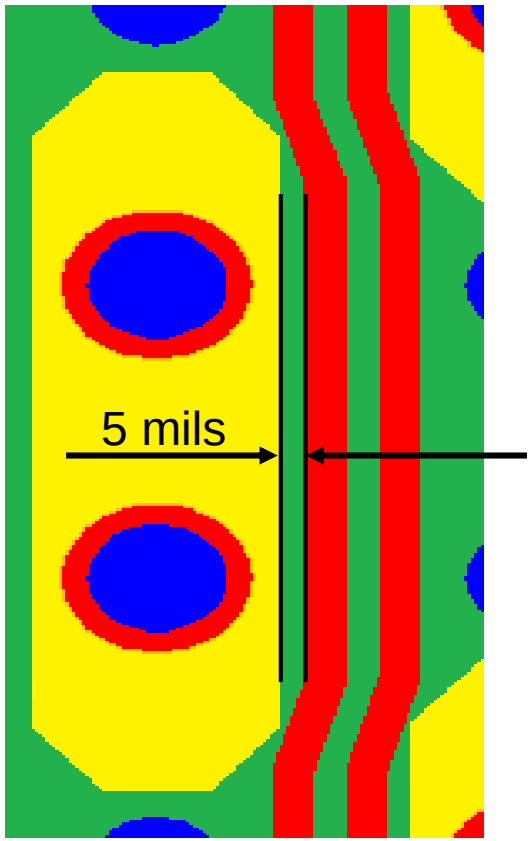




Trace Routing Considerations (cont)

- Right angle bends are not a viable option for routing the traces. The zig-zag method however showed minimal differences from the straight route.
- The illustration below is the same Multigig RT2 routing case study with the 7-7-7 in column trace routing in a zig-zag pattern.





Trace Routing Considerations (cont)

- Characteristics of zig-zag implementation
  - Allowed the traces to be shifted enough to have a full 5 mils clearance from trace to antipad for the majority of the route, while still maintaining at least 9 mils from trace to ground via.
  - The consequential “crossing region” where the traces pass between the two opposite corner antipads is only slightly closer than the full straight route implementation. (anti-pad corners could be trimmed to grow this distance)
  - This implementation yields a passing distance of 1.6 mils on the corners instead of the 1.8 mils in the straight configuration.
- Advantages of the zig-zag implementation
  - The discontinuity where the traces pass between the corners of the antipads is very short and hence minimal if any signal degradation will be encountered.
  - The overall majority of the route follows optimum design rules.

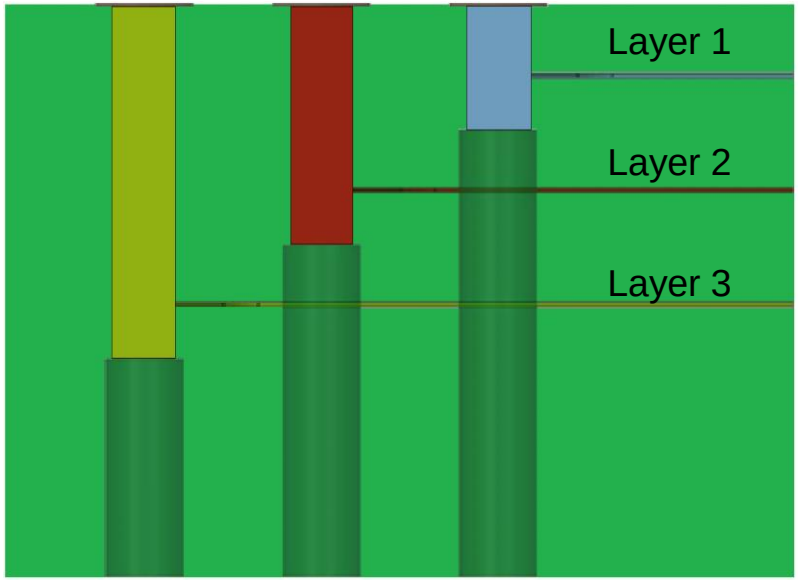
Trace Routing Considerations (cont)

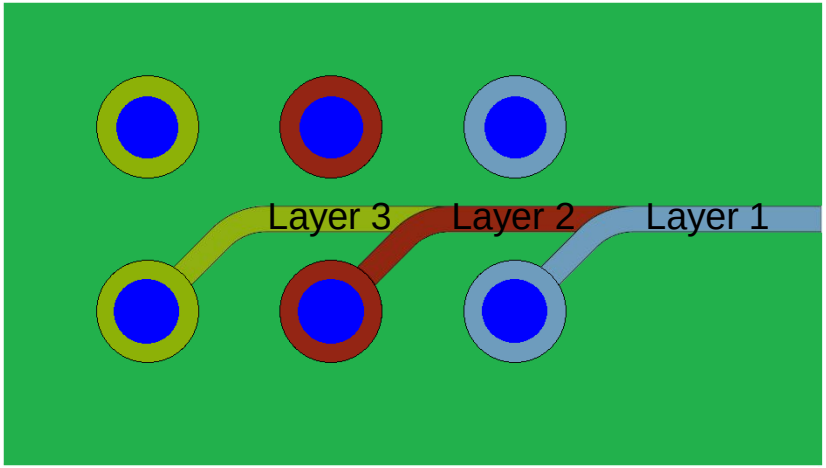
- The previous study focused on the backplane only for this connector pair for two reasons.
  - The daughter card drill for the eyes of needle (EON) is smaller at .55mm (21.65mils) instead of .65mm (25.59mils). This inherently allows for narrower antipads and greater channel routing width.
  - The daughter cards typically are thinner and have significantly shorter routing distances.
- Consequently the trace configurations for daughter cards are often times a 5-5-5 or 6-6-6 configuration.

- Another trace routing consideration is for when signal traces pass by a different signal via. One technique for addressing the potential noise from the proximity routing is something called layer dependent routing. The illustration on the next slide shows layer dependent routing.

Trace Routing Considerations (cont)

- The layer dependent routing takes advantage of the backdrill operation in that the sequential drill depth growing as traces progress down the channel allows traces to pass by the back drilled region versus the alien signal via.





Summary

- As high speed systems have increased data rates, the effects of the footprint region have become more significant and consequently design engineers must consider the effects of each design parameter.

- The case study illustrates how connectors designed years ago, but are being stretched to higher data rates, must have alternate routing considerations as such.

- A high speed channel must be designed with all segments optimized for high speed. Just like a system routed on FR4 will not perform well at high speeds, or a system with low tech silicon may have too much signal degradation, a system designed with poor PCB design rules and routing criteria will also perform poorly.

Summary (cont)

- As technology continues to increase data rates, more focus will be placed on the intricate details of a design and smaller details will matter when they previously did not. This trend will likely continue for some time.