# High Performance Computing using FPGAs

ALE System Integration

NI Technical Conference

November 10, 2009

# ALE SYSTEM INTEGRATION

www.aleconsultants.com – info@aleconsultants.com

- Based in Long Island, New York – projects nationwide
- National Instruments Certified Alliance Partner
  - All developers have National Instruments Certification
- Experience:
  - Test Labs, Manufacturers, Mil/Aero, Finance
  - Over 14 Years Test & Automation experience
- Design:
  - LabVIEW, LabWindows/CVI, TestStand, Visual Studio
  - FPGA Design using Xilinx Tools, Impulse C, LabVIEW

NATIONAL INSTRUMENTS
Certified Alliance Partner

# Terry Stratoudakis, P.E.

- Education/Certifications
  - B.S., M.S. in Electrical Engineering, Polytechnic University
  - NI Certified LabVIEW Developer and Certified Prof. Instructor
  - New York State licensed Professional Engineer
- Experience
  - Worked at Underwriters Laboratories for six years
  - Former Assistant Adj. Prof. at NYC College of Technology
  - Co-founder and President of ALE System Integration

# John Stratoudakis

- Education/Certifications
  - B.S. in Computer Science, Drexel University
  - NI Certified CVI Developer
  - Microsoft Certified Application Developer
- Experience
  - Five years as software developer for financial applications
    - S&P subsidiary Capital IQ, Investment Technology Group
  - LabVIEW FPGA, Visual Basic, .NET, C#, C/C++, Perl
  - Author of several open source software projects

# Overview

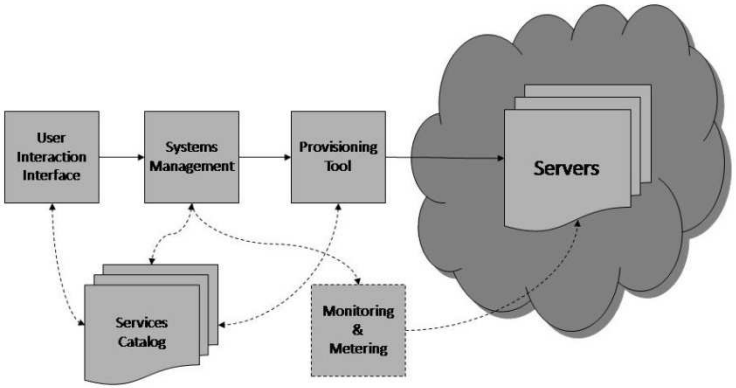
- Introduction
- Proof of Concept
  - Buffon's Needle
- Physics and Finance HPC Needs
  - Low Latency, Computational Power
- Case Studies
  - Finance: Option Valuation
  - Physics: Tomography and Matrix Math
  - RF: S-Parameter De-embedding
- Benefits of LabVIEW FPGA for HPC

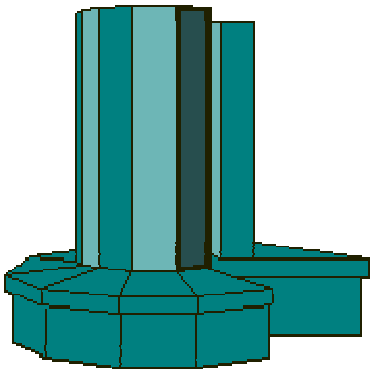
# Introduction

- Goal: Use FPGAs in HPC
  - Existing but limited FPGA use in HPC
- Proof of Concept – Buffon's Needle
  - Simple Monte Carlo Method
- Develop methods for using FPGAs in HPC
- Coded in LabVIEW for FPGA
  - Finance Stock Option application
  - Physics Tomography application
  - S-parameter de-embedding (RF application)

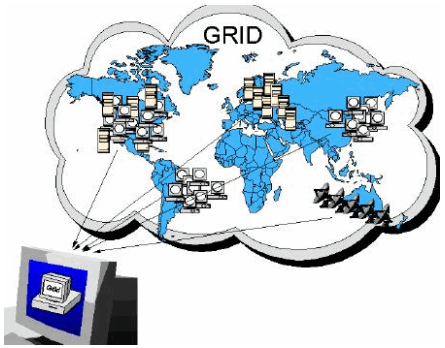
# What is HPC?

- Uses powerful computers to solve advanced computation problems
- HPC is successor of Supercomputing
- Hardware Accelerators
  - Custom Hardware for specialized task
- Cluster, Cloud, Grid, SaaS

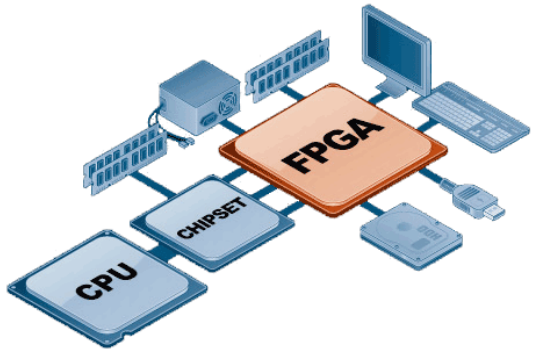


# HPC Implementations

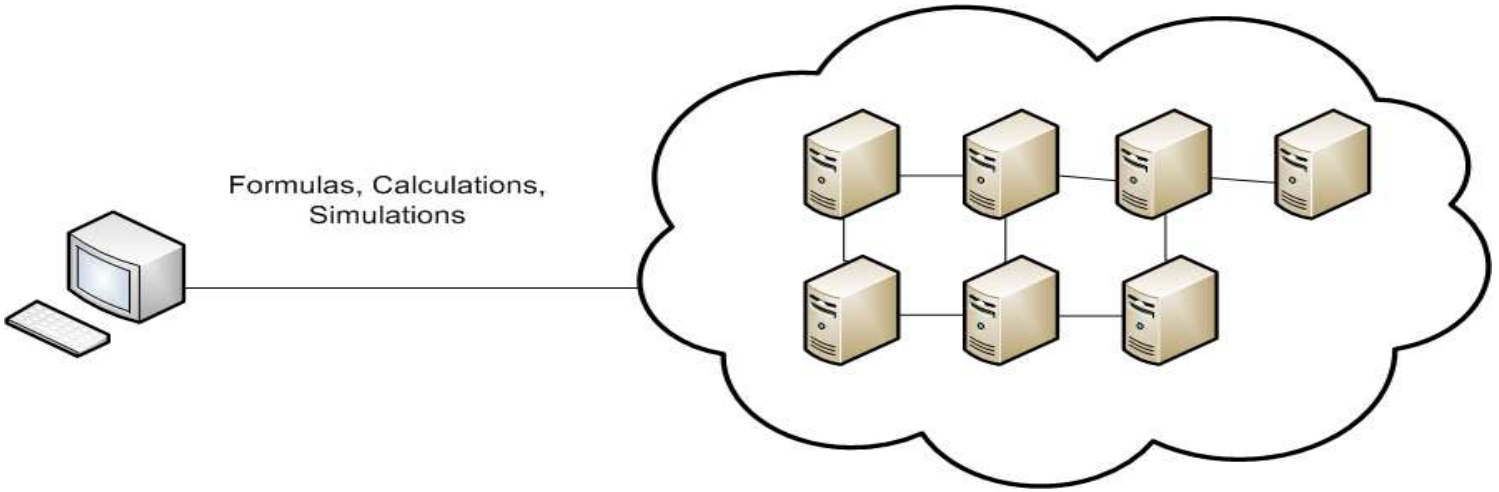



- Grid computing
  - Pros: fast, can be easily programmed
  - Cons: energy and space inefficient, high maintenance costs
- Hardware Accelerators (FPGAs)
  - Pros: fast, energy and space efficient
  - Cons: need to know Hardware Description Language (HDL)



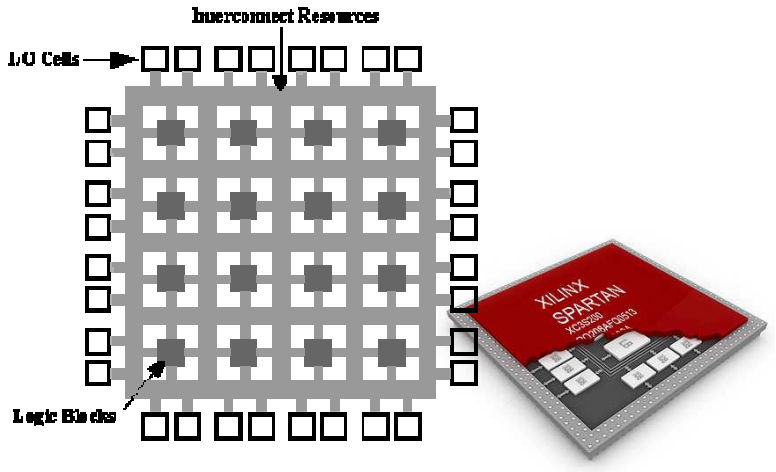
# Grid Computing

- Many networked computers working together
- Most existing software cannot run “as is”
- Requires special knowledge of parallel programming APIs and languages



# Hardware Accelerators

- Field Programmable Gate Arrays (FPGAs)
- Configured with Hardware Description Language
- *True* parallel execution



# Field Programmable Arrays (FPGA)

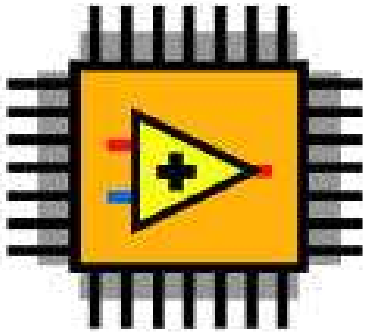
- Introduced in 1987
- Parallel Execution
- Low Power Usage
- Customizable Integrated Circuit
- Millions of configurable gates on a single chip
- No Operating System

# LabVIEW

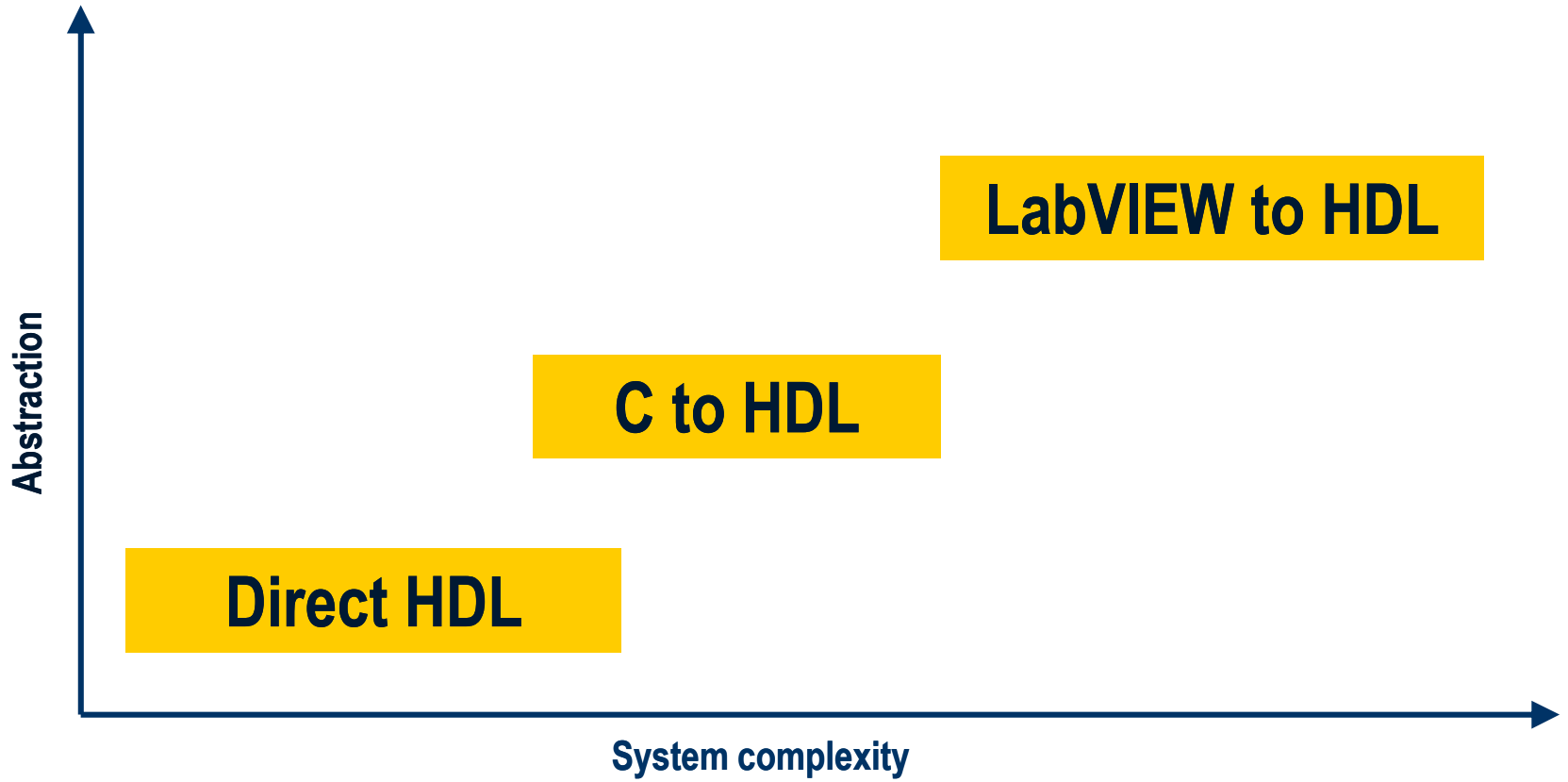
- Introduced in 1986
- Graphical programming language
- Multiple execution targets
- Runs on Windows, Mac, Linux
- Easy to write parallel programs
- Broad industry use:
  - Military/Aerospace, Research, Industrial, Control, and Embedded Applications
- Taught in most educational institutions

# LabVIEW FPGA Module

- Add-on to LabVIEW
- Use LabVIEW skill set to quickly program *Xilinx* FPGAs
- Converts LabVIEW Block Diagram to HDL
- Higher level of Abstraction
- IP Net has many tools
  - www.ni.com/ipnet



# Evolution of Software Abstraction



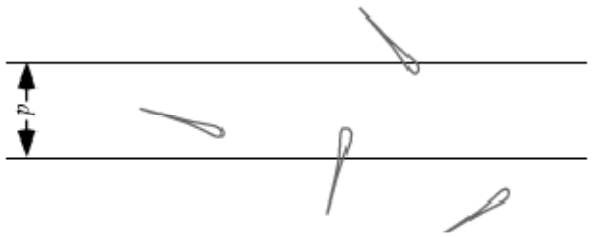
# Overview

- **Proof of Concept**
  - **Buffon's Needle**
- Physics and Finance HPC Needs
  - Low Latency, Computational Power
- Case Studies
  - Finance: Option Valuation
  - Physics: Tomography and Matrix Math
- Benefits of LabVIEW FPGA for HPC
  - Fast Development
  - Performance Improvements
  - Energy and Space Savings

# Buffon's Needle

- Early Monte Carlo Method for calculating $\pi$
- Drop a needle and count how many times it lands on a line (repeat)
- Test case for programming Monte Carlo method on LabVIEW FPGA

$$\pi = \frac{2ln}{dh}$$



# Buffon's Needle Results

- Proof of concept a success
  - Development time – One (casual) day
  - LabVIEW for FPGA ran faster than PC
  - Defined process used in Case Studies
- Identified challenges
  - Understand algorithm
  - Fixed point math
  - Parallelization
  - Verification

# HPC to LabVIEW FPGA Process

1. Understand algorithm
   a. Look for ability to parallelize
   b. Identify math functions needed
      - e.g. logarithmic, division, multiply, exp, random numbers)
      - See NI IPNet (www.ni.com/ipnet)
2. Implement in LabVIEW FPGA
   a. Goal: run in single-cycled timed loop
   b. Pipelining
3. Test with simulated mode
4. Verification with known data

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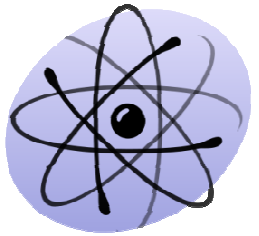
# Physics and Finance HPC Needs

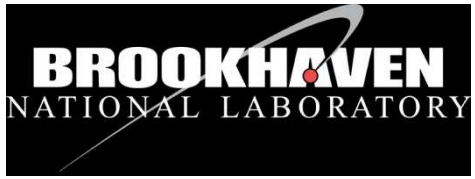
- Goals and motivations are polar opposites
  - Physics: advancement of science
  - Finance: corporate/personal financial gain
- Technical needs are nearly identical
  - Low Latency
    - Fast trade execution and market data routing
    - Routing of research data to super computing nodes
  - Computational Power
    - Matrix Math, large data sets
    - Monte Carlo Methods, custom algorithms

# HPC in Big Physics



- Used to process research data from colliders, synchrotrons, etc.
- Large control systems such as telescopes
- Used by Labs, Research Institutes
- Examples:
  - Brookhaven National Labs (BNL)
  - Princeton Plasma Physics Lab (PPPL)
  - National Energy Research Scientific Computing Center (NERSC)






# HPC in the Finance Industry

- Used to process market data and value financial instruments
- Used by Exchanges, Investment Banks, Hedge Funds, Mutual Funds
- Recent crashes demonstrate dynamic needs
- Dedicated Conferences & Periodicals








# Fat Tails in Finance

- Current models assume events are “well-behaved”
- Fat tail events are rare and not “well-behaved”
  - oil shock
  - large corporate bankruptcy
  - abrupt change in a political situation
- Example:
  - An investment strategy may have an expected return, after one year, that is five times its standard deviation.
  - Assuming a normal distribution, the likelihood of its failure (negative return) is less than one in a million; in practice, it may be higher.

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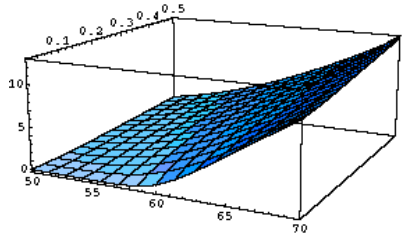
# Black-Scholes Option Valuation



- Published in 1973
- Basis for Quantitative Finance
  - Equity price modeled as stochastic time series
- Pricing of Options and Corporate Liabilities
- Basis for multi-trillion dollar Options Trading
- Computed with a Monte Carlo Simulation

$$dS_t = \mu S_t\,dt + \sigma S_t\,dW_t$$

$$\nu = \frac{\partial V}{\partial \sigma}$$

$$u(x,\tau) = \frac{1}{\sigma\sqrt{2\pi\tau}} \int_{-\infty}^{\infty} u_0(y) e^{-(x-y)^2/(2\sigma^2\tau)}\,dy.$$

$$\frac{1}{\sqrt{2\pi}} \int_{-\infty}^{x} e^{-\frac{z^2}{2}}\,dz$$

$$dV = \left(\mu S \frac{\partial V}{\partial S} + \frac{\partial V}{\partial t} + \frac{1}{2}\sigma^2 S^2 \frac{\partial^2 V}{\partial S^2}\right) dt + \sigma S \frac{\partial V}{\partial S}\,dW.$$

# European-style* Option Valuation

$$c = S_0 N(d_1) - Ke^{-rT} N(d_2)$$

$$p = Ke^{-rT} N(-d_2) - S_0 N(-d_1)$$

$$d_1 = \frac{\ln\left(\frac{S_0}{K}\right) + \left(r + \frac{\sigma^2}{2}\right)T}{\sigma\sqrt{T}}$$

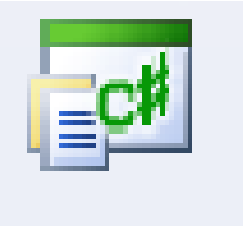
$$d_2 = d_1 - \sigma\sqrt{T}$$

**As opposed to American, Asian, Bermudan, Barrier, Exotic, Vanilla-style options*

# Challenge

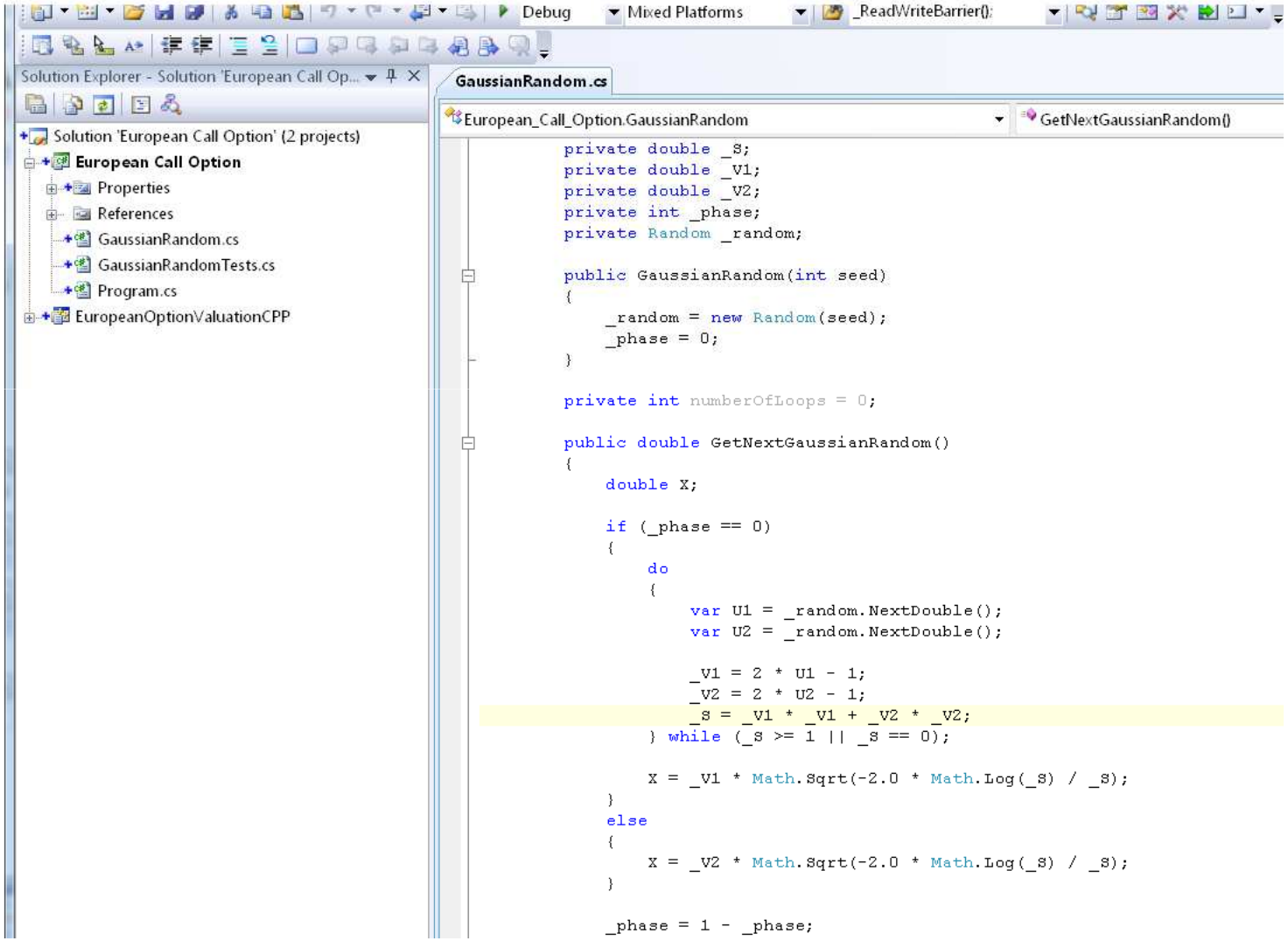

- Program Black–Scholes European Option Valuation on:
  - NI Compact-RIO platform (Xilinx FPGA)
    - Running National Instruments LabVIEW 8.6.1
  - Alienware PC
    - Running Microsoft Visual C# .NET 2.0
- Benchmark
  - Development time
  - Execution time
  - Energy Consumption

# Visual C# on Dual-Core PC

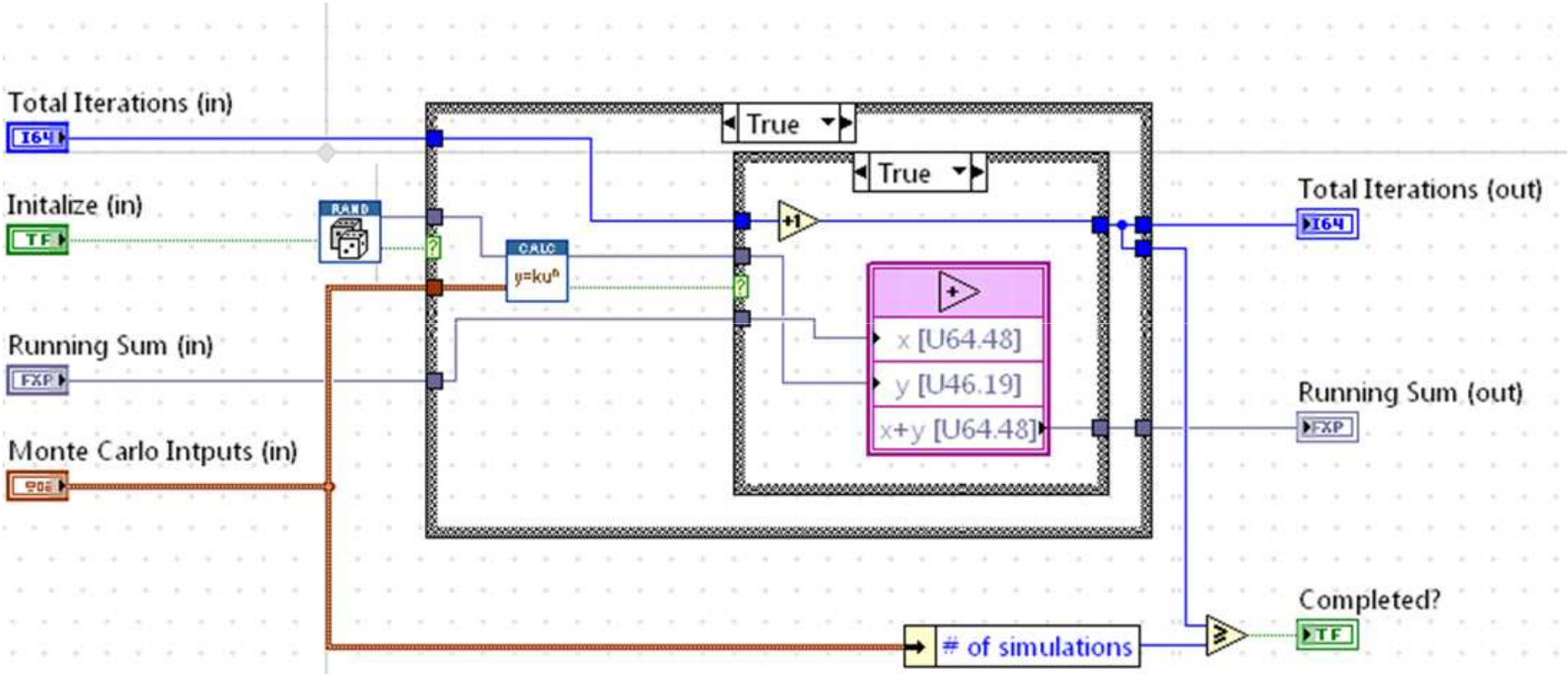



- Microsoft Windows Vista Ultimate Edition
- High-Performance Gaming Machine
- 3.0 GHz Intel Core 2 Duo E6850
- SATA RAID-0 10,000 RPM Hard Drives
- 4 GB RAM
- .NET 2.0 Runtime

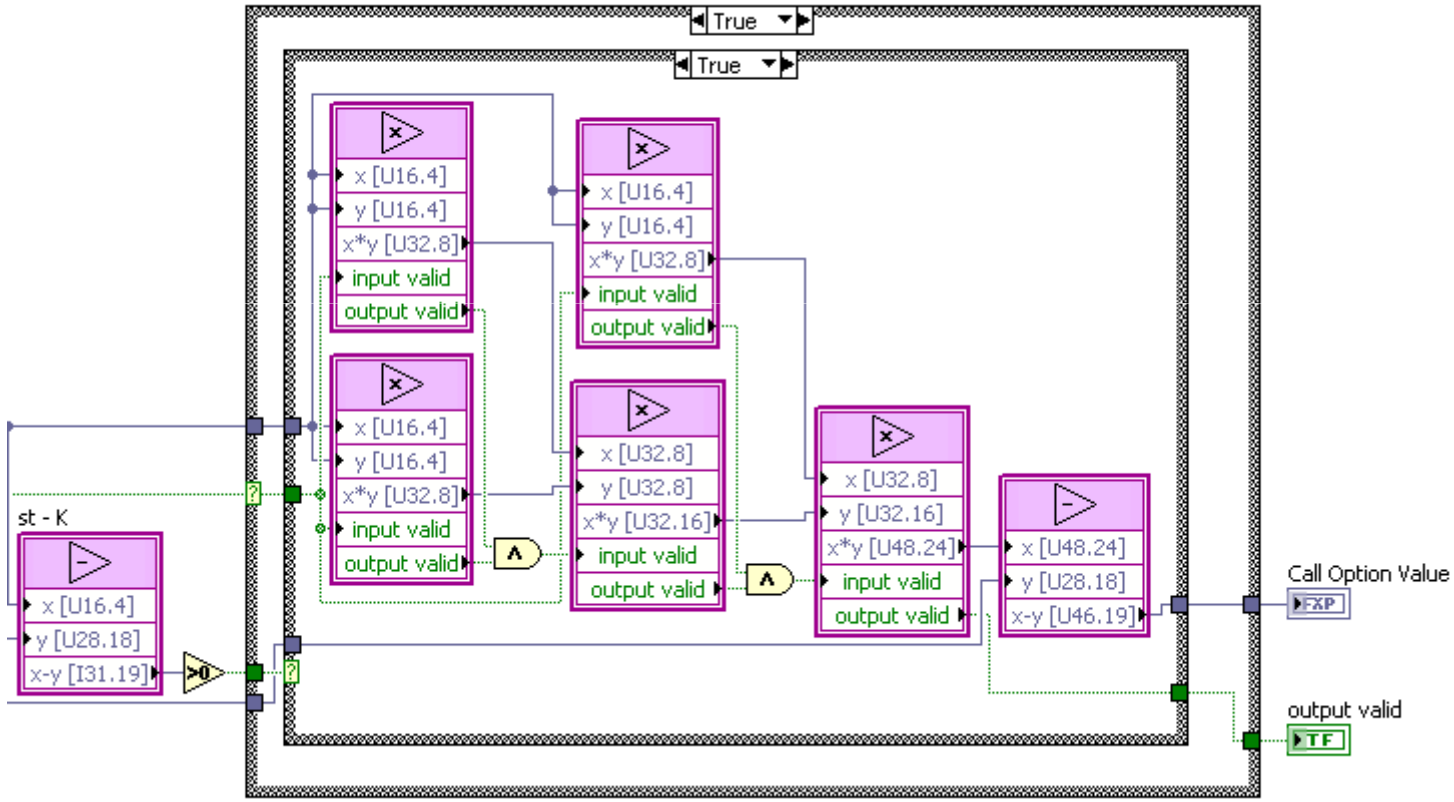
# Black Scholes - Visual C#



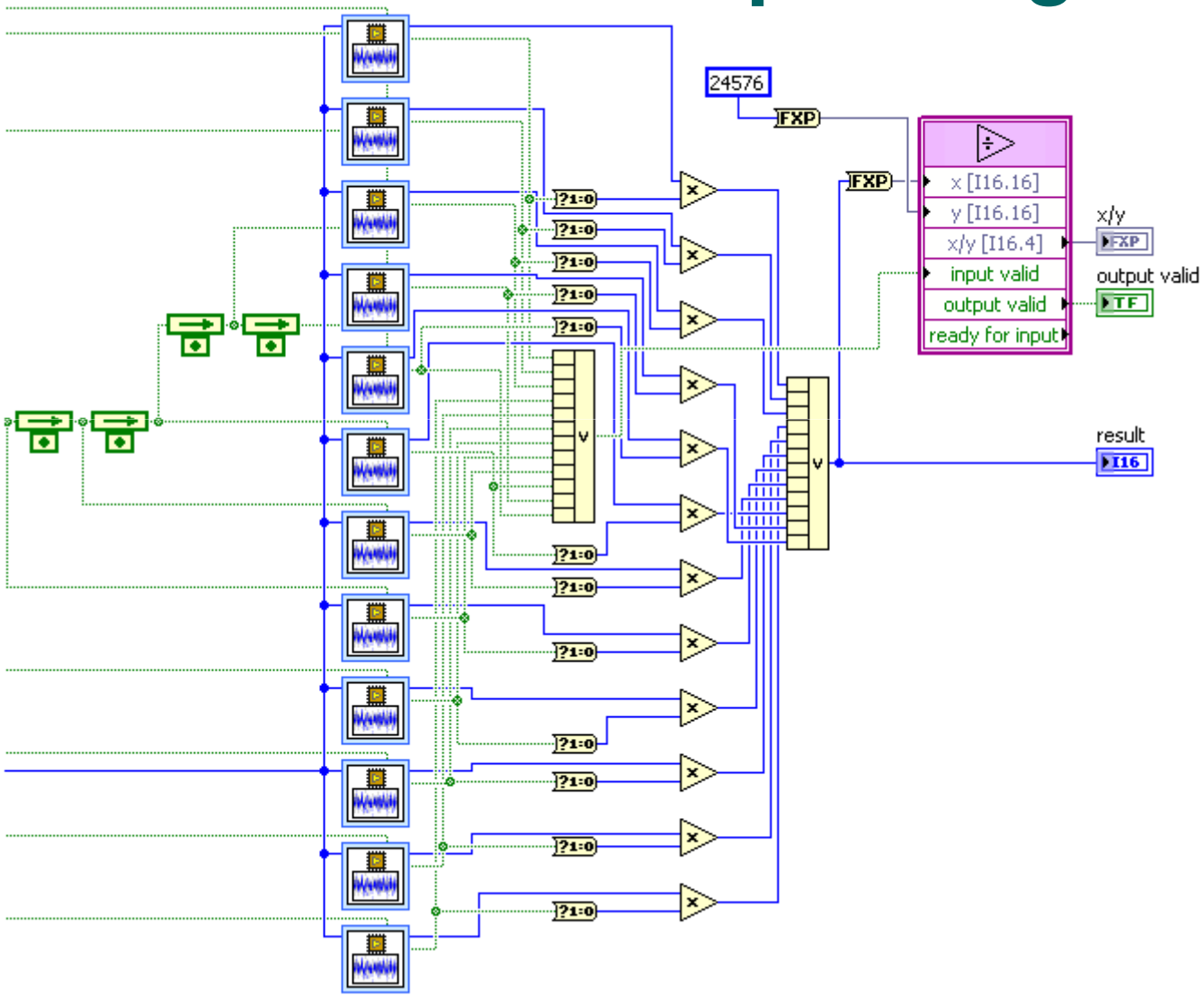
# Black-Scholes on LabVIEW FPGA



# LabVIEW FPGA – Fixed Point Math



# LabVIEW FPGA – Pipelining



# Results

- Development times were comparable
- LabVIEW on FPGA ran 49X faster
- LabVIEW on FPGA had 33X energy reduction
- Compact-RIO takes up 1/8 the space

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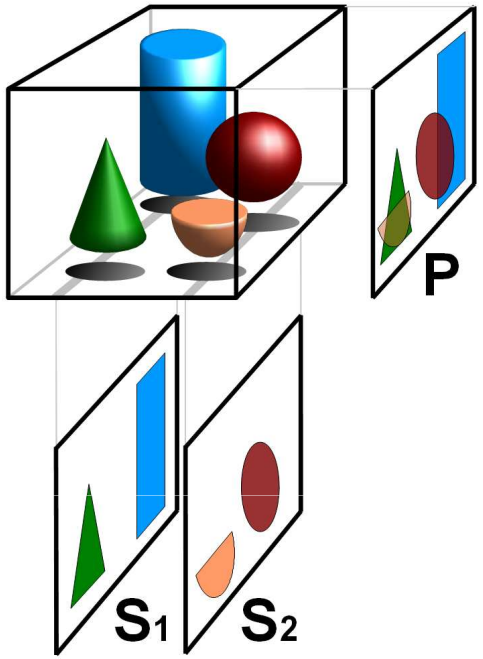
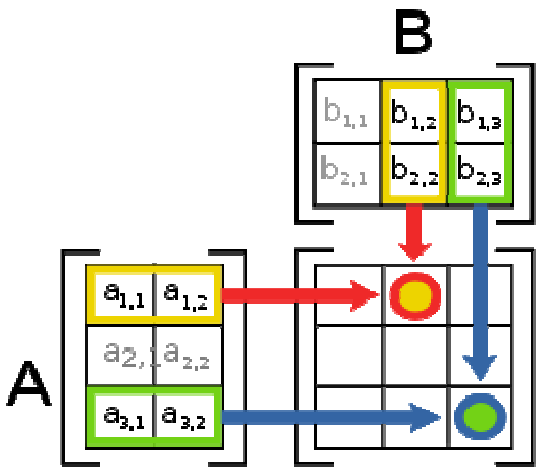
# Tomography

- Imaging by sections
- Used in various fields
- Computed with Matrix Math



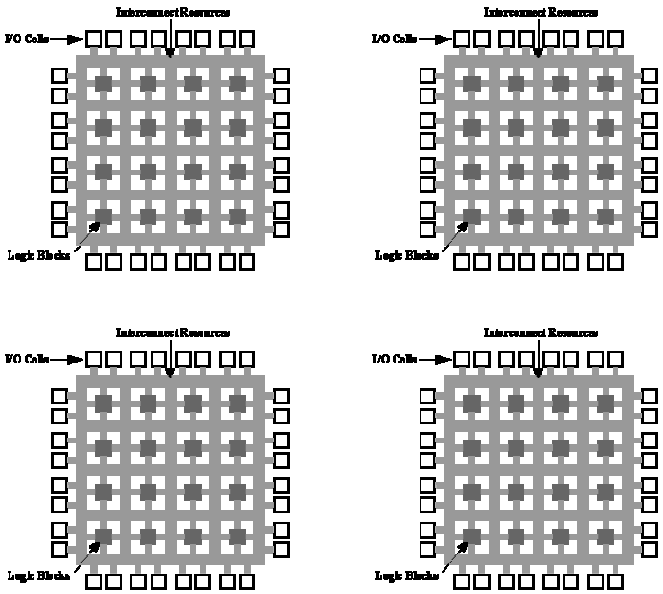
# Matrix Math on LabVIEW for FPGA

- One FPGA did not show performance gain
- Designed two FPGA chip solution
  - FPGA 1: Calculate resultant vector
  - FPGA 2: Matrix Math
- Speed gains came from simultaneously multiplying Matrix rows
- Could add more FPGAs for Matrix Math
  - Using FlexRIO

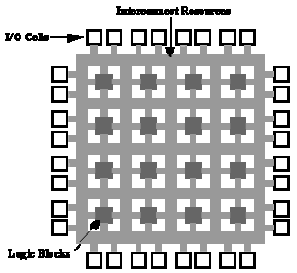
# Multi-FPGA Architecture

**Parallelized**

**Matrix Multiplication**




**Vector Result**

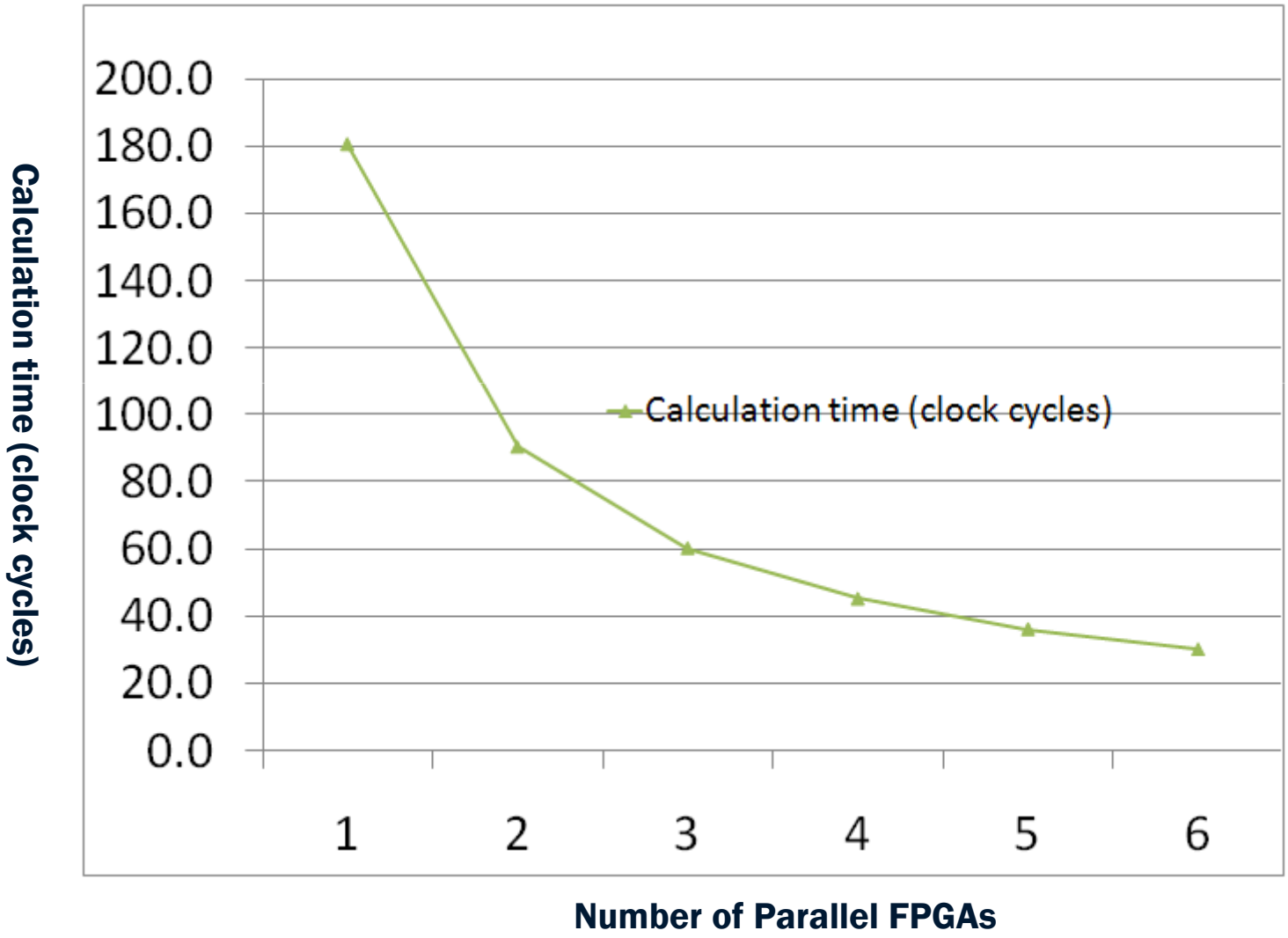



**Check Vector**

**Result Accuracy**

**Accuracy Met?**

# Multi-FPGA Performance Gains



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# Benefits of LabVIEW FPGA for HPC

- LabVIEW for FPGA is an HPC solution
  - Quick development
  - Energy efficient
  - Fast execution
- Physics & Finance have HPC needs
- LabVIEW for FPGA can be faster than text based programming running on a grid
- Moore's Law still applies to FPGAs