

Modeling Tools For Power Supply Impedance Analysis

By VITO DERASMO, MSEE
NYU Poly

FOR PDH CREDIT:

www.ieee.li/forms/3777

© 2024 VITO DERASMO



Introduction

- The concept of impedance matching has been addressed in prior publications.
 - Ex - MIL-HDBK-241 issued in 1983.
 - Ex – *Fundamentals of Power electronics* – Erickson, Maksimovic
- This presentation builds on these foundations to enhance understanding of these topics.
 - Useful tools and Methods are provided.
 - Less complex Math.
 - Demonstrates value of using SPICE.
- Real life Test scenarios are discussed.



```
2370 REM ** ROUTINE TO DETER**
2380 REM ** NINE IF MORE PLOTS*
2390 REM ** ARE WANTED **
2400 REM
2410 DISP "Would you like to cha
nge:"
2420 DISP
2430 DISP "1)all component value
s?"
2440 DISP "2)filter component va
lues only?"
2450 DISP "3)source and load val
ues only?"
2460 DISP "4)characteristic to b
e Plotted?"
2470 DISP "5)frequency limits?"
2480 DISP "6)number of points Pl
otted?"
ontinue";
2790 INPUT Cs
2800 PRINT ALL
2810 DISP "Impedances are refere
nced to oneohm.The output i
mpedance,Zs,is"
2820 DISP "the impedance looking
back into the filter with
Vs short cir-"
2830 DISP "cuted.The loaded fil
ter will bedisplayed and yo
u will be asked"
2840 DISP "to enter the value of
each com-"
2850 DISP "ponent.You will also
be asked which characteri
stic you would"
2860 DISP "like plotted, the fre
```

$$Q_1 = 20 \log_{10} \sqrt{(1 + L_1/C_1 R_c^2)/((C_2/C_1)^2 + (L_1/C_1 R_c^2)(1 - C_2/C_1 - L_2 C_2/L_1 C_1)^2)}$$

thus

$$Q_1 = 20 \log_{10} \sqrt{(1 + (R_1/R_c)^2)/((C_2/C_1)^2 + (R_1/R_c)^2 [1 - C_2/C_1 - (\omega_1/\omega_2)^2]^2)}$$

$$Q_1 = 20 \log_{10} 2.05 = 6.3 \text{ dB}$$

and at the second stage,

$$Q_2 = 20 \log_{10} \sqrt{L_2/L_1} = -4.7 \text{ dB}$$

Why are we concerned with Impedance Matching?

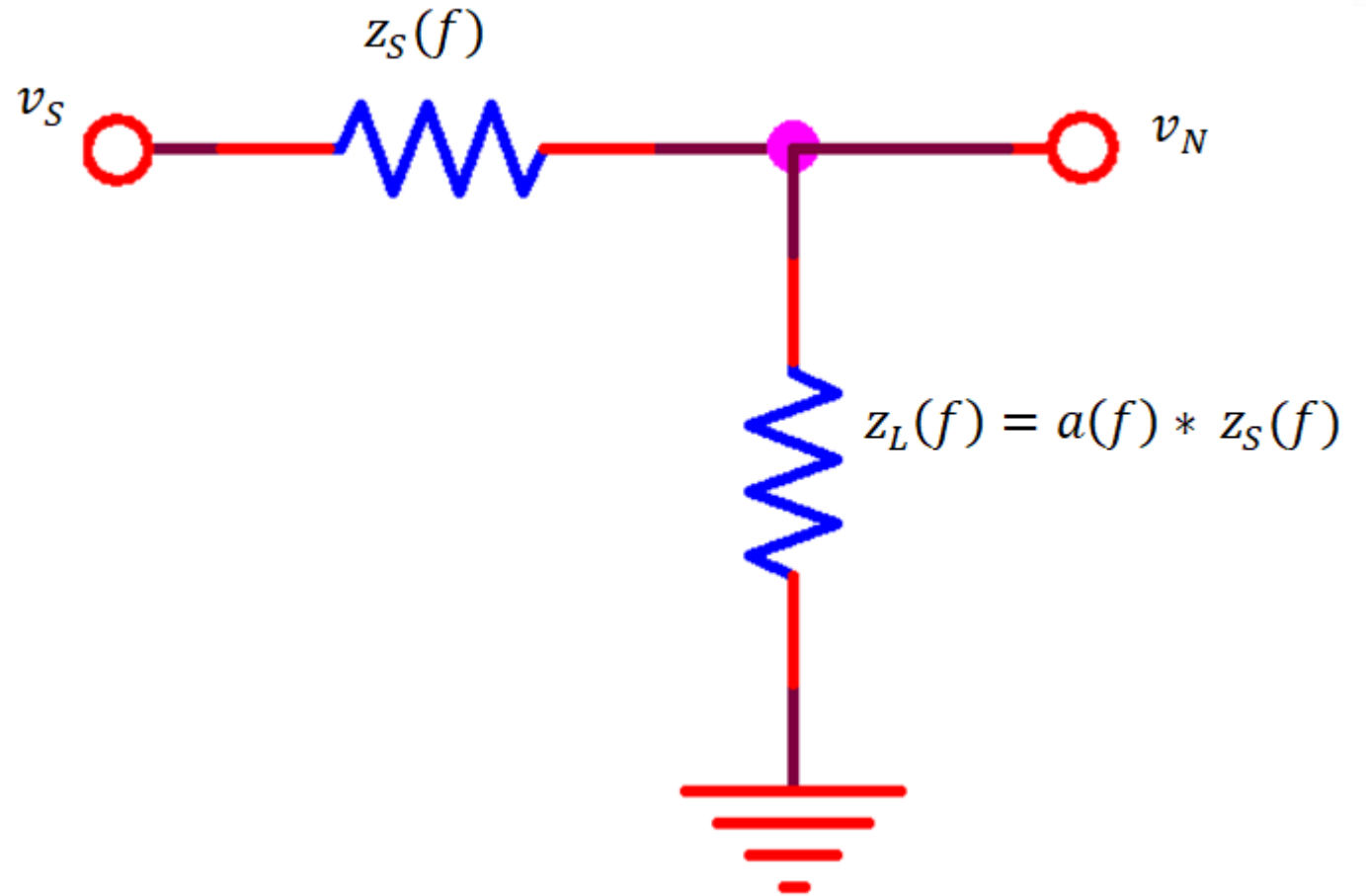
Whenever two 'Boxes' are connected, the source impedance, and the load impedance should be evaluated.

For the circuit shown, nodal analysis produces the gain function $\frac{v_N}{v_S} = \frac{a(f)}{a(f)+1}$

As a approaches -1, v_N goes to infinity.

Since Power Supplies have negative input impedance within the control loop band, $|z_L| > z_S$ must be maintained.

A 10 db Margin is recommended.



Do Power Supplies have a Negative Input Impedance?

Given an input voltage with a sinusoidal component $v_{In}(t) = a \sin(\omega t) + V_{DC}$

For an ideal power supply, the input Power will not vary with input voltage. The current can be represented as $i_{In}(t) = \frac{P_{Const}}{a \sin(\omega t) + V_{DC}}$ for frequencies within the control loop range. This offset inverted sine function produces a fundamental with even harmonics, however for small signal analysis, 98% of the waveform is a first harmonic 180° sine function, as shown.

Therefore, the power supply represents a significant negative impedance for small signal analysis.

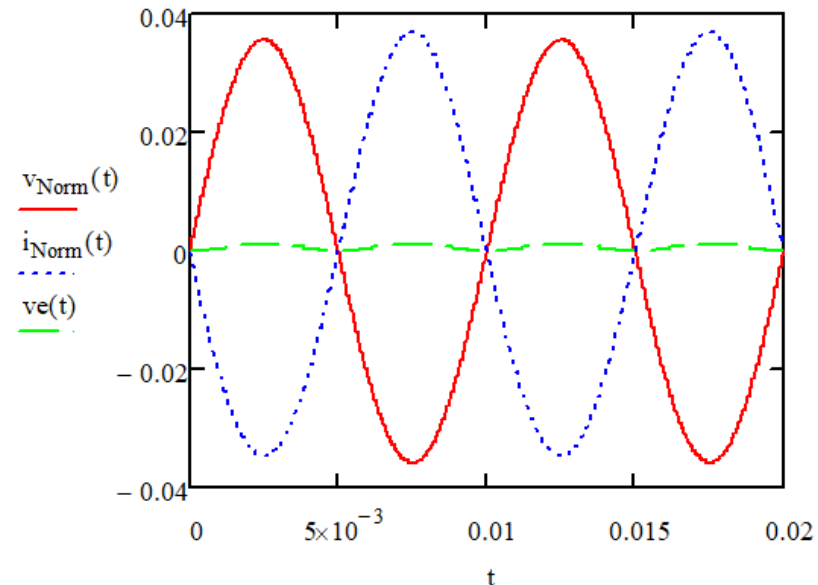
$$f_r = 100\text{Hz} \quad \omega = 2\pi \cdot f_r$$

$$a = 1\text{V} \quad V_{DC} = 28\text{V} \quad P = 100\text{W} \quad I_{DC} = \frac{P}{V_{DC}} = 3.571\text{A}$$

$$v_{In}(t) = a \cdot \sin(\omega \cdot t) + V_{DC} \quad i_{In}(t) = \frac{P}{v_{In}(t)}$$

$$v_{Norm}(t) = \frac{v_{In}(t)}{V_{DC}} - 1 \quad i_{Norm}(t) = \frac{i_{In}(t)}{I_{DC}} - 1$$

$$\text{Error} \quad v_e(t) = v_{Norm}(t) + i_{Norm}(t) \quad +$$



The normalized voltage is a pure sine, when added to the normalized current a small error is produced.

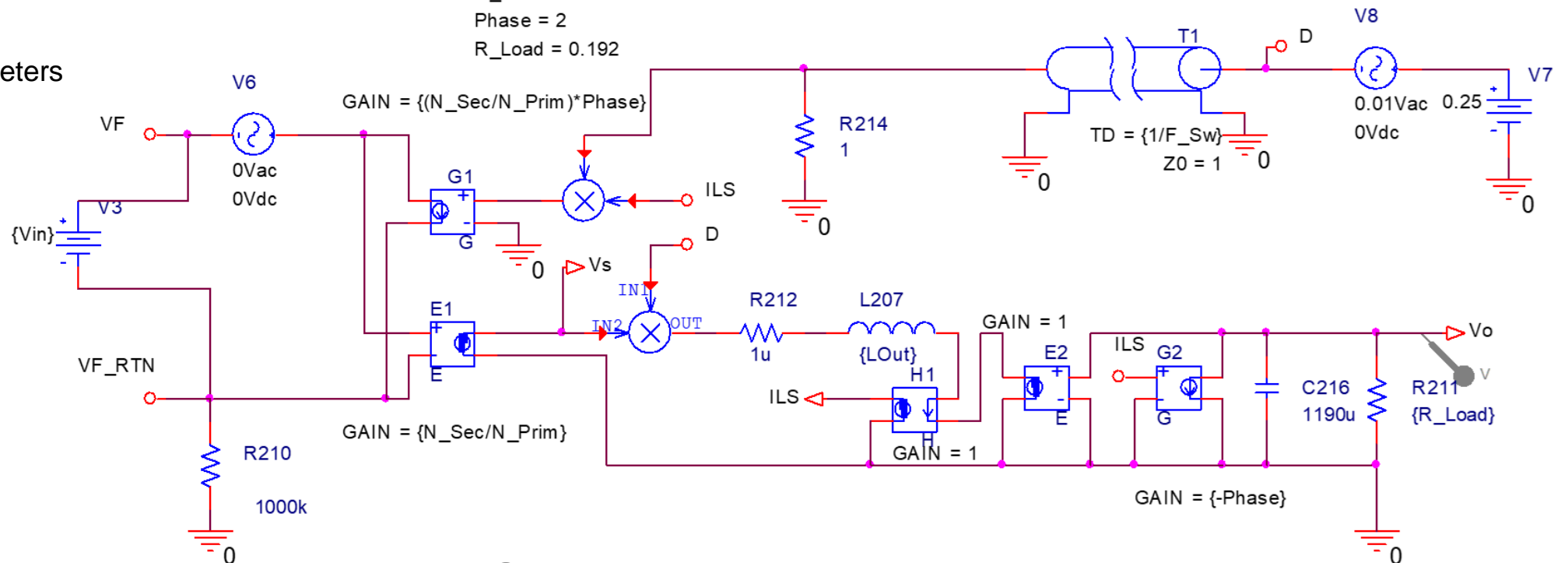


Power Train SPICE Model

- Inputs are V3 (input voltage) and D (Duty Cycle).
- The Transmission line adds delay due to PWM.
- Output is Vo.
- Load is R211.
- Notice the use of Parameters

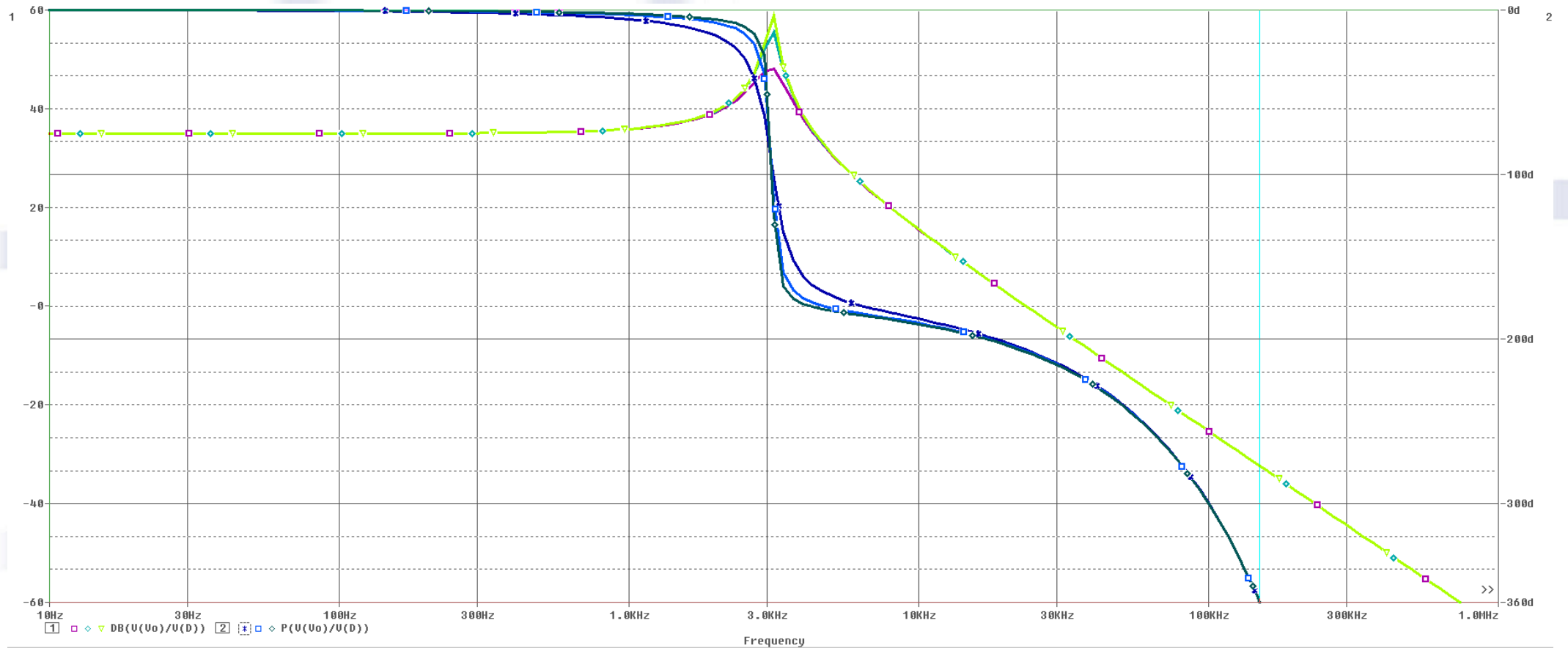
PARAMETERS:

LOut = 4.4u
 Vin = 28
 F_Sw = 300k
 N_Prim = 4
 N_Sec = 8
 Phase = 2
 R_Load = 0.192



Power Train Sweep, Duty Cycle to V_o

Using Parameters, Load is Swept from 0.2 to 0.8 ohms

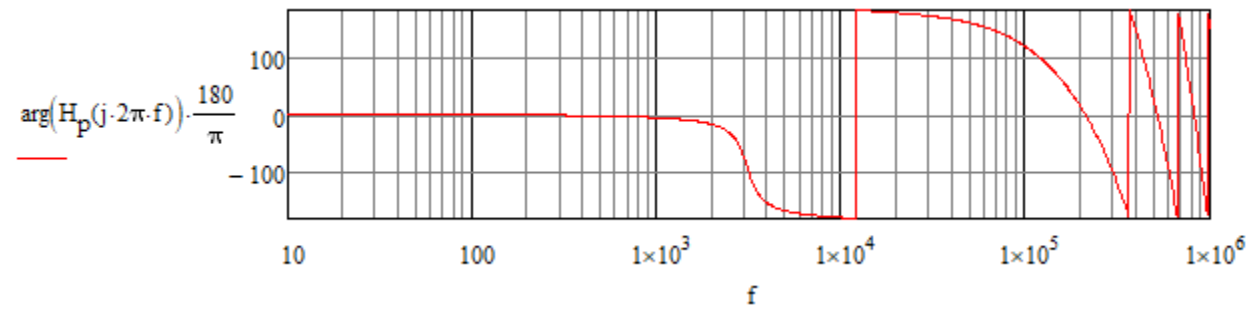
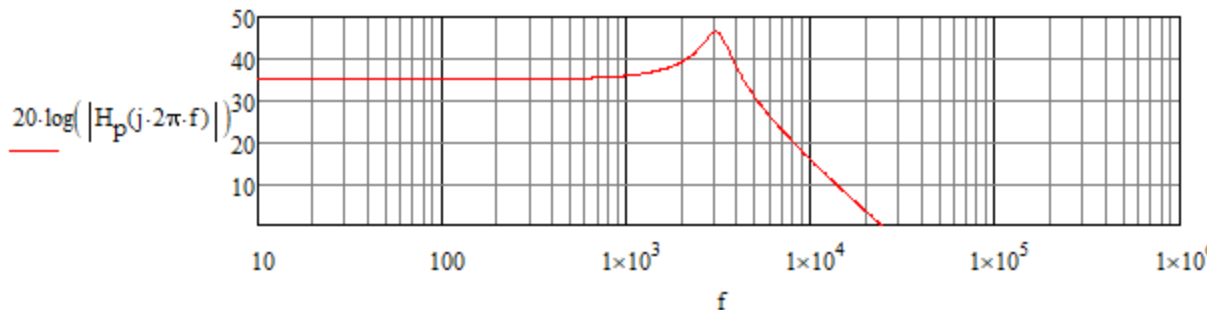


Closing the VM Loop

- This Full process will be condensed, as this falls outside the focus of this material.
- The Nominal DC Gain is simply the Nominal V_o / Nominal DC $G_{DC} = \frac{V_o}{D_{nom}} = 56$
- Nodal analysis can be used to calculate the Plant Gain as a function of frequency

$$H_p(s) = G_{DC} \cdot \frac{s \cdot R_L \cdot R_{esr} \cdot C_o + R_L}{s^2 \cdot \left(\frac{L_o}{Phase} \cdot C_o \cdot R_L + \frac{L_o}{Phase} \cdot C_o \cdot R_{esr} \right) + s \cdot \left(R_L \cdot R_{esr} \cdot C_o + \frac{L_o}{Phase} \right) + R_L} \cdot e^{-s \cdot T_m}$$

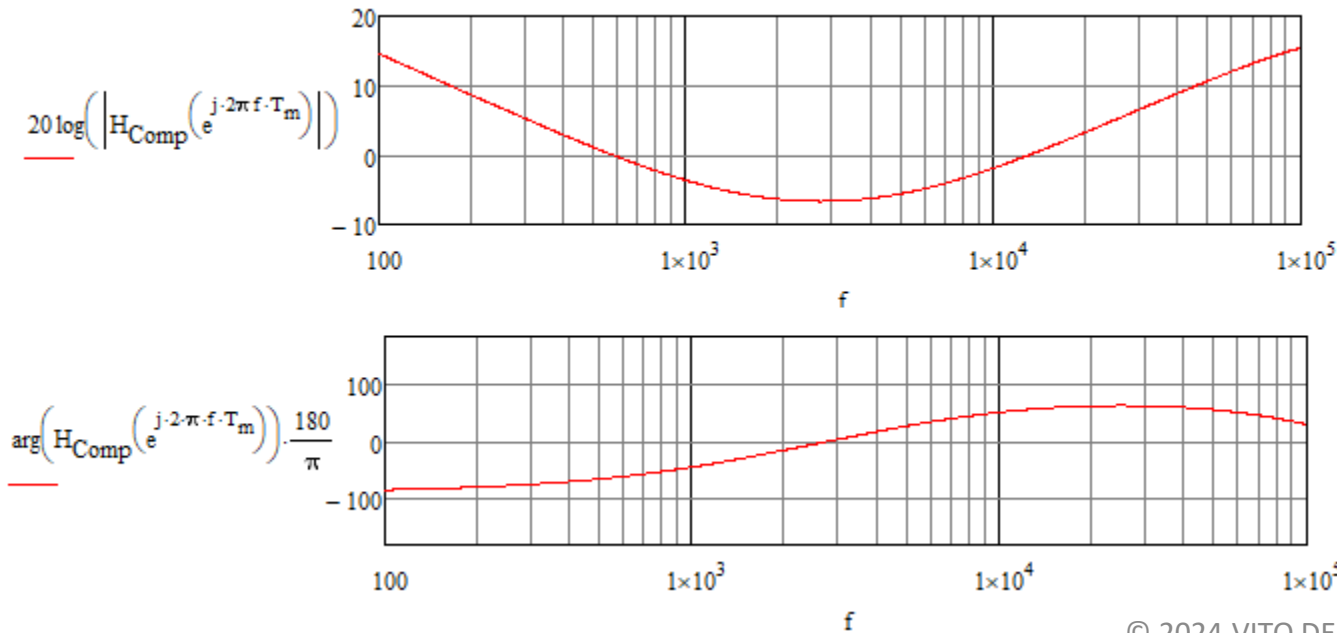
- This yields results consistent with SPICE



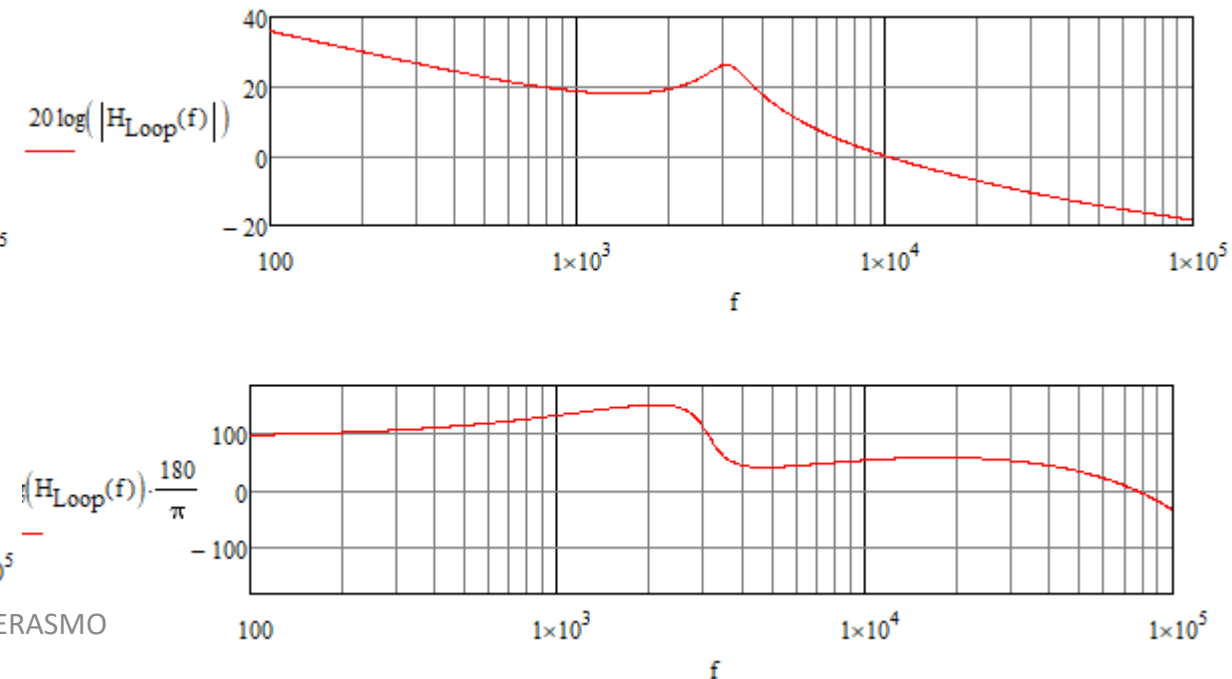
Closing the VM Loop (continued)

- A pole and 2 zeros will be used to compensate the Loop.
- The zeros will be placed slightly before and after the resonant frequency.
 - Be sure to include Load Capacitance in the bulk Output Capacitance. ESR can also be added.
- Zeros are installed at 1500 and 5000Hz in this case. Integrator is set to yield a 10kHz crossover.

Compensator

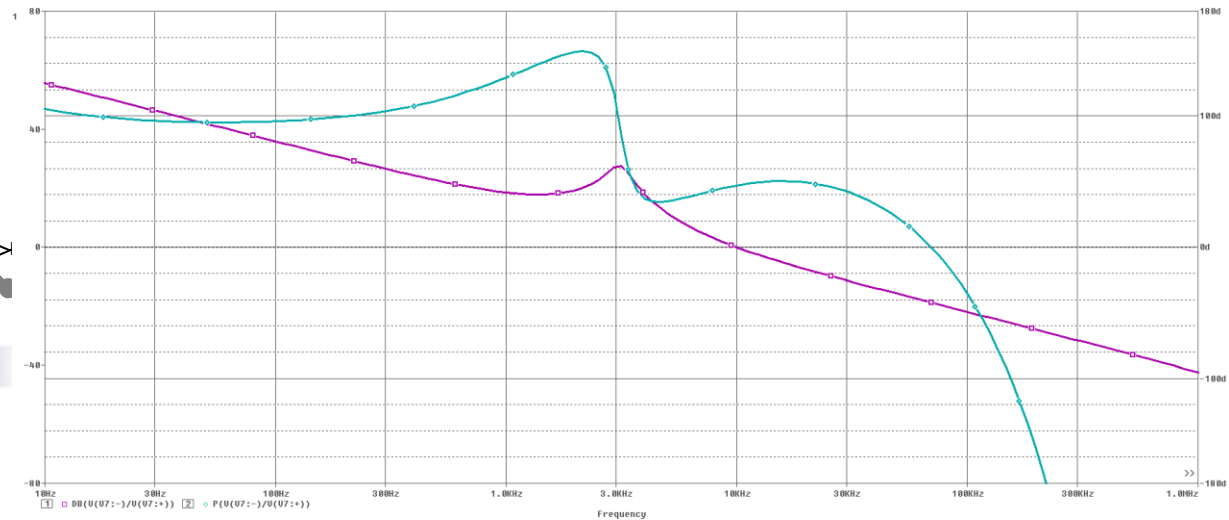
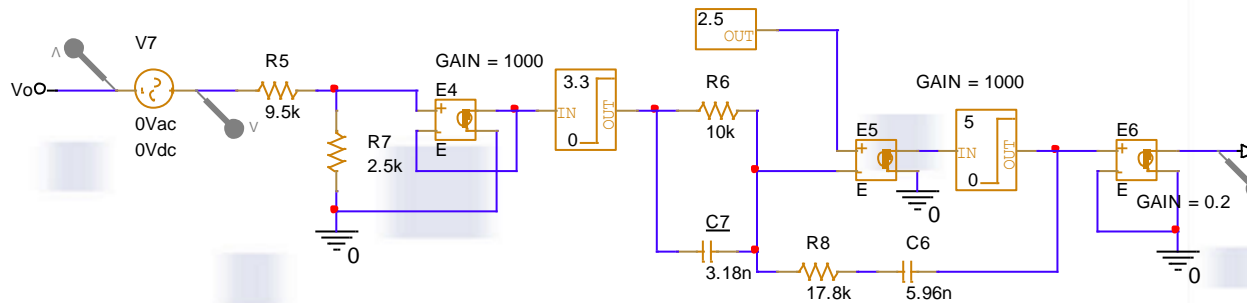


Complete Loop



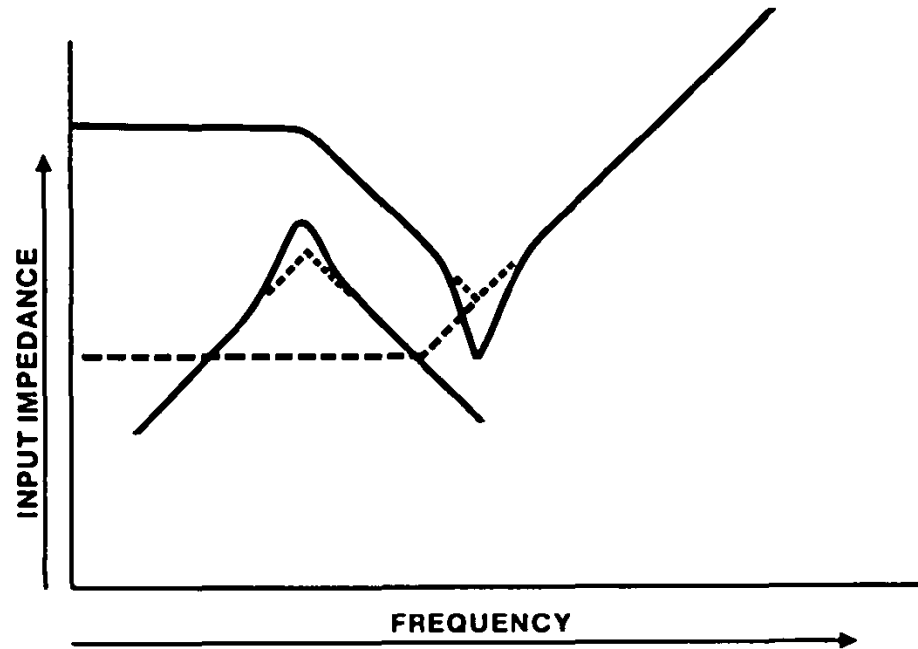
Closing the VM Loop (continued)

- The Compensator is added to the SPICE Model



- The SPICE Model Validates the Math Model.
- SPICE can now be used to generate an input impedance plot for the VM converter.
- On the power train schematic (Slide 5), an AC sweep on V6 produces the impedance plot.

Impedance Match Criteria



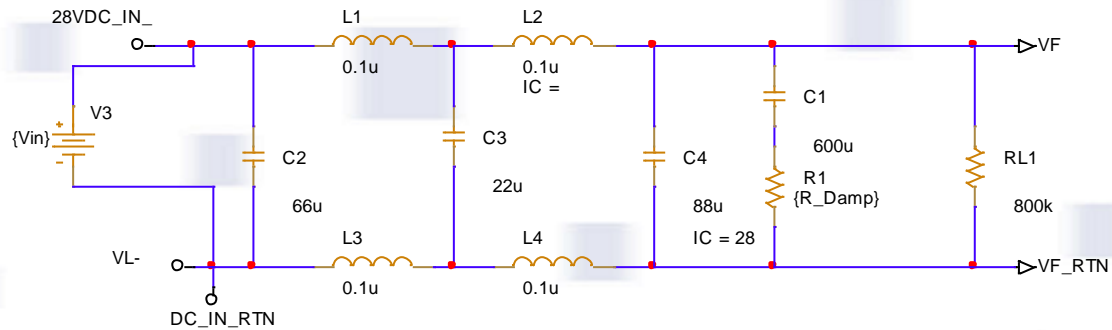
Excerpt from MIL-HDBK-241

A Voltage Mode Controller is shown

- Characterizing the input impedance of the converter becomes important when we add our EMI filter to the design.
- The Middlebrook Criterion request 10 db margin between the source and load impedances.
- This has proven a difficult target to hit when considering all operating conditions.

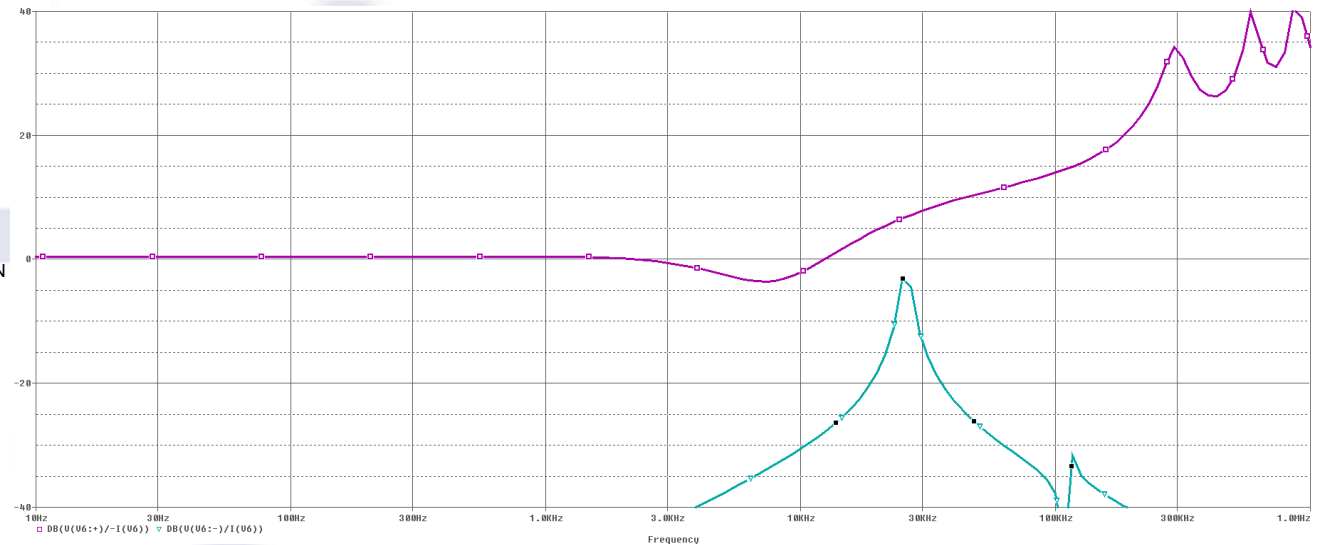
Voltage Mode Impedance Match

- An EMI Filter is added to the Front End.
- The Resonance of the filter is carefully selected to be higher than the Resonance of the output filter.
- This maintains Margin between the input and output impedance.



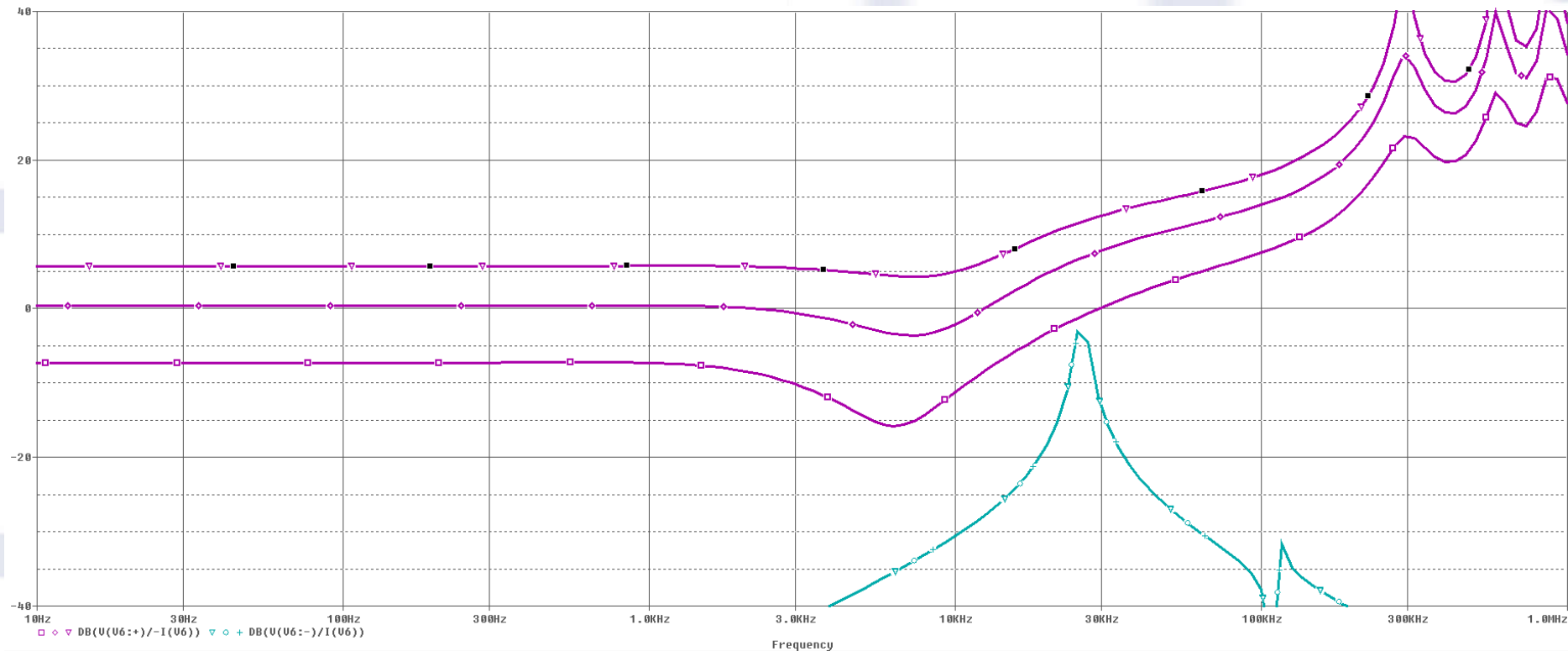
PARAMETERS:

L_{Out} = 4.4u
V_{in} = 28
F_{Sw} = 300k
N_{Prim} = 4
N_{Sec} = 8
Phase = 2
R_{Load} = 0.192
R_{Damp} = 1

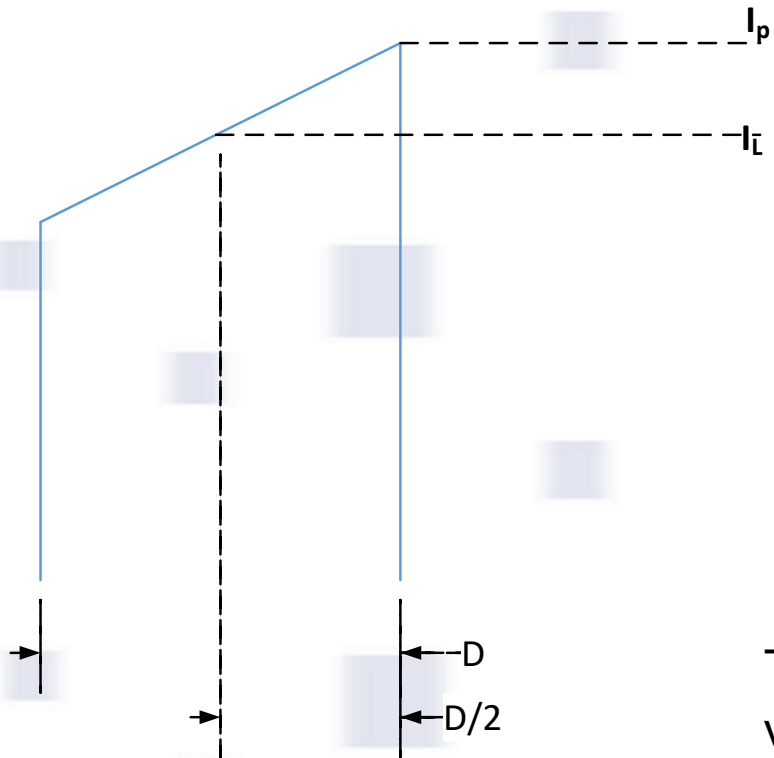


Voltage Mode Impedance Match – Need For Margin

- Using Parameters, the input voltage is swept from 18V to 38V
- Margin helps to Maintain Stability



Average Modeling for a Current Mode Controller



The commanded Current from the controller is i_p , The resulting average current is i_L

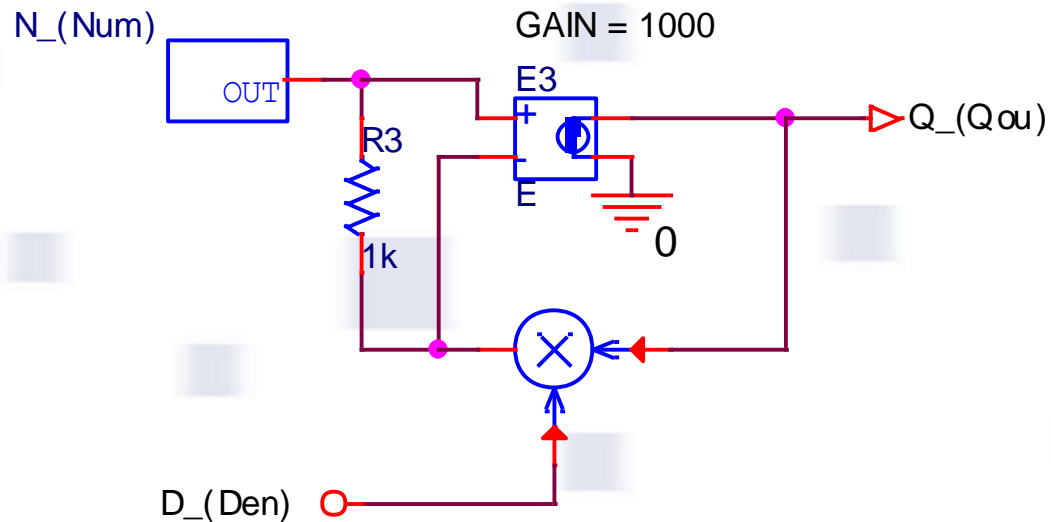
$$i_p = i_L + \frac{v_L}{L} * \Delta T , \text{ where } \Delta T = \frac{d}{2} * \frac{1}{F_{SW}}$$

Solving for d yields...

$$d = (i_p - i_L) * \frac{2F_{SW}L}{v_L}$$

This is a fairly simple equation, except for one problem... The inductor voltage varies and requires SPICE to perform real-time division. There is no such function in SPICE, so we must introduce a method.

Emulating Division in SPICE



Following the schematic, we can write an expression for Q

$$Q = 1000 * (N - (Q * D))$$

We can now expand the equation

$$Q = 1000N - 1000Q * D$$

Gather the Q terms

$$Q(1 + 1000D) = 1000N$$

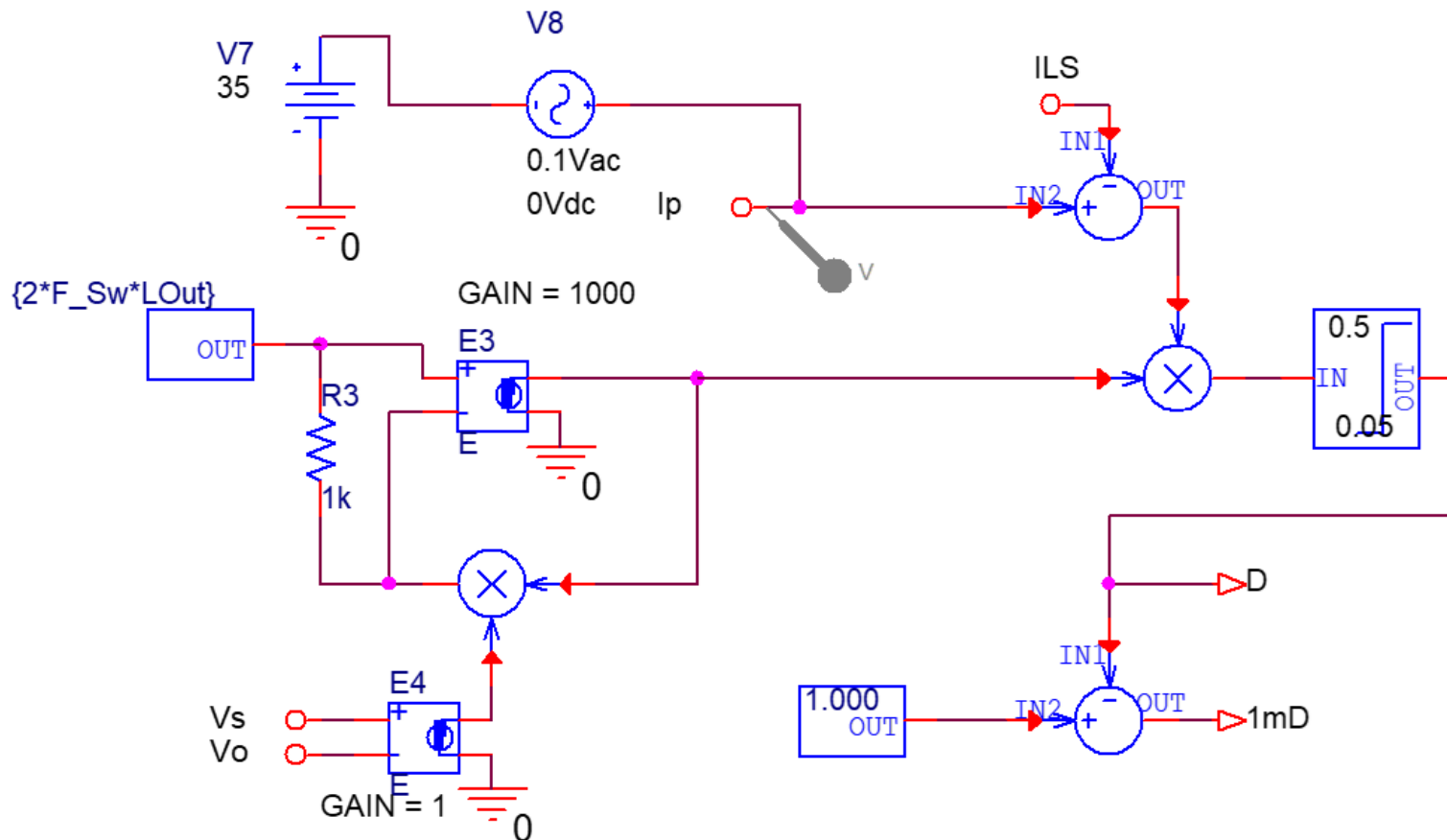
Solve for Q

$$Q = \frac{1000N}{1 + 1000D}$$

We can see that Q is a pretty good representation of division, as long as $1000D$ is much greater than 1.

Credit to George C Gallios who introduced this method

CMC Duty Cycle Generator

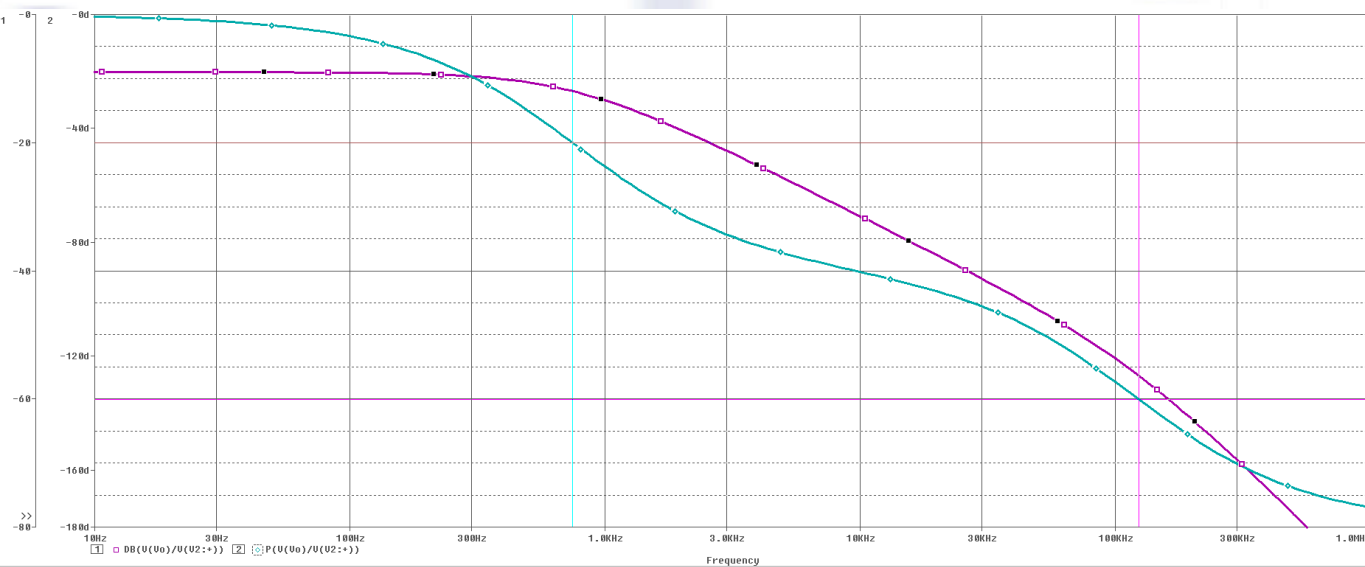


Implementing

$$D = (i_P - i_L) * \frac{2F_{SW}L}{v_L}$$

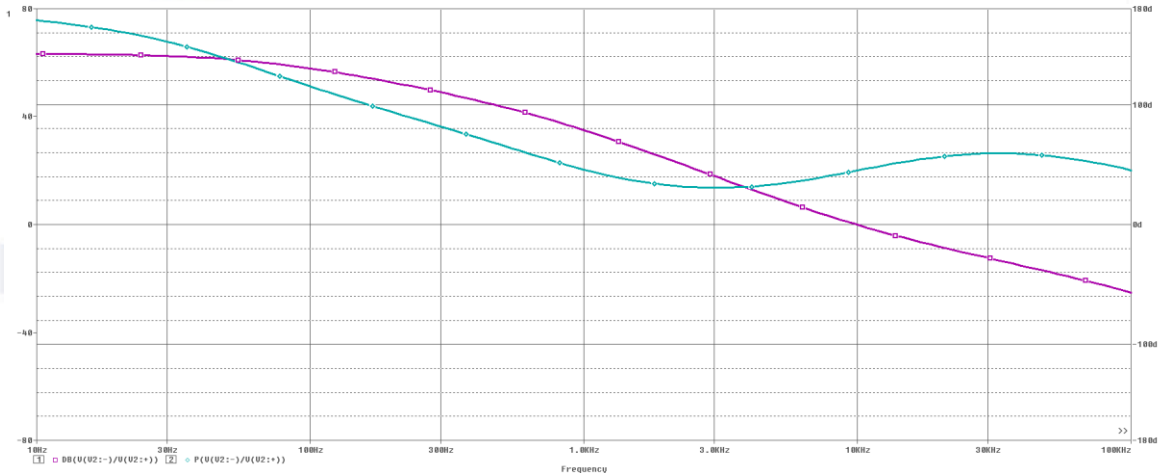
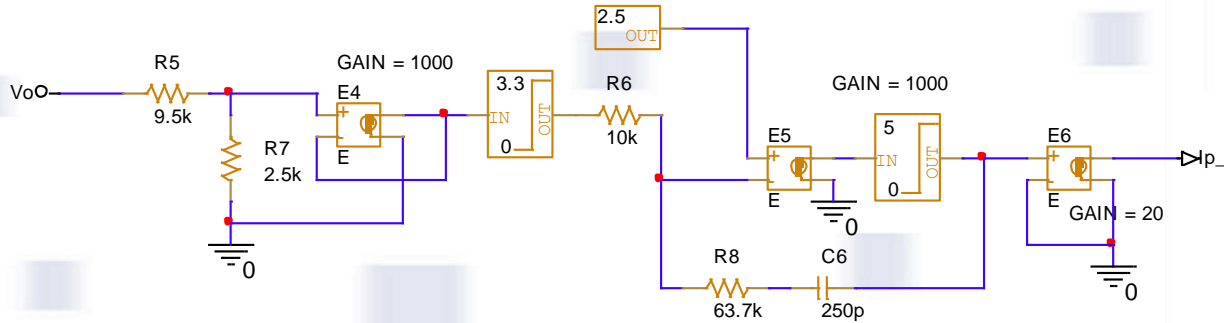
- i_P represents the Commanded Current.
- i_{LS} is the measured inductor current.
- $v_S - v_O$ is the inductor voltage during the charge time.

CMC Plant AC Sweep



- Low frequency gain is flat. This is the Commanded current times the load resistor
- Dominant pole at 750 Hz. This is where the output capacitor becomes dominant over the load resistor.
- Second pole at 125kHz, this is approximately $\frac{1}{2}$ the switching frequency where the current mode control process breaks down.
- Goal for this example is to design a control loop to a target crossover frequency of 10 kHz.
- At 10 KHz, the plant gain is -31.5 db and the phase is -90°.

CMC Controller



- Voltage sense has a gain of 2.5:12 or -13.6db
- Current sense has a gain of 20 or 26db.
- Previous Page, Plant is -31.5 db at the 10 kHz desired crossover (Unity Gain)

$$G_{Comp_{10kHz}} = -(G_v + G_{CS} + G_{Plant_{10kHz}})$$

$$G_{Comp_{10kHz}} = -(-13.6db + 26db - 31.5db) = 19.1 db = 9.02 X$$

$$R_{Comp} = G_{Comp_{10kHz}} * 0.707 * R_{FB}$$

$$R_{Comp} = 9.02 * 0.707 * 10k = 63.7k$$

$$C_{Comp} = \frac{1}{2\pi * F_{Cr} * R_{Comp}}$$

$$C_{Comp} = \frac{1}{2\pi * 10 kHz * 63.7k} = 250 pF$$

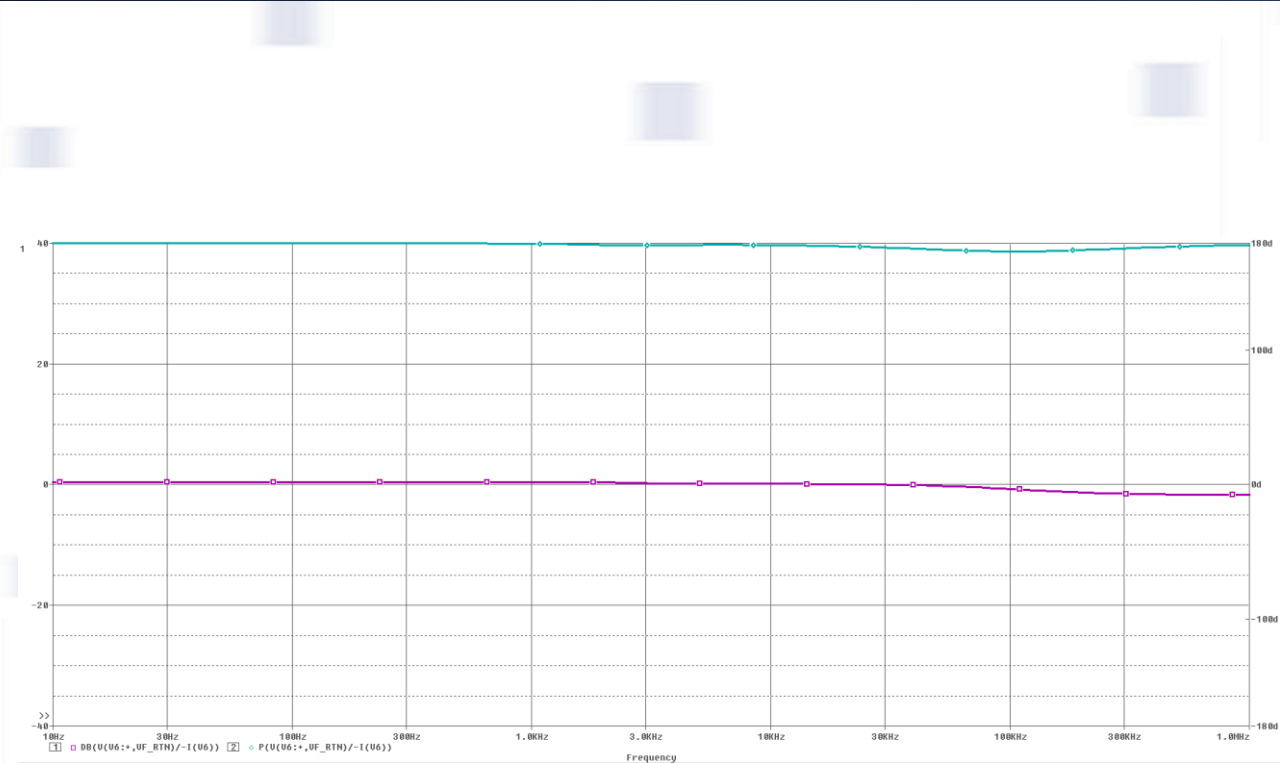
Current Mode Input Impedance plot.

By changing the insertion point to the input, an input impedance plot can be taken.

Input voltage and Current are measured.

Spice performs the $\frac{v(f)}{i(f)}$ math in the post-processor tool.

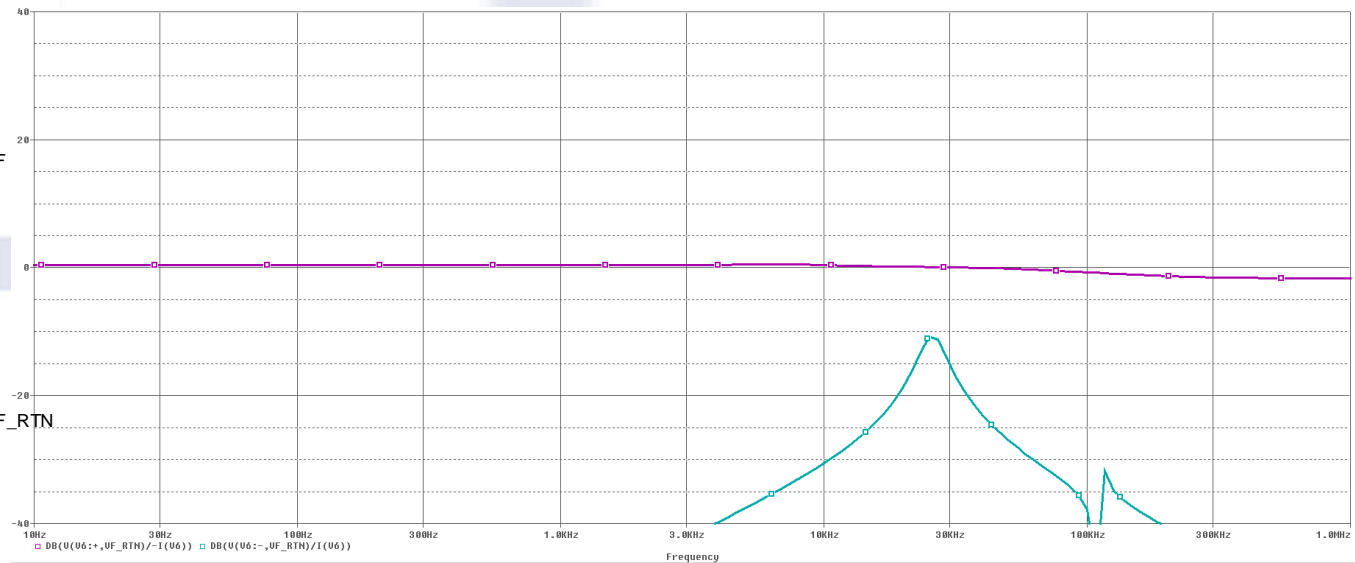
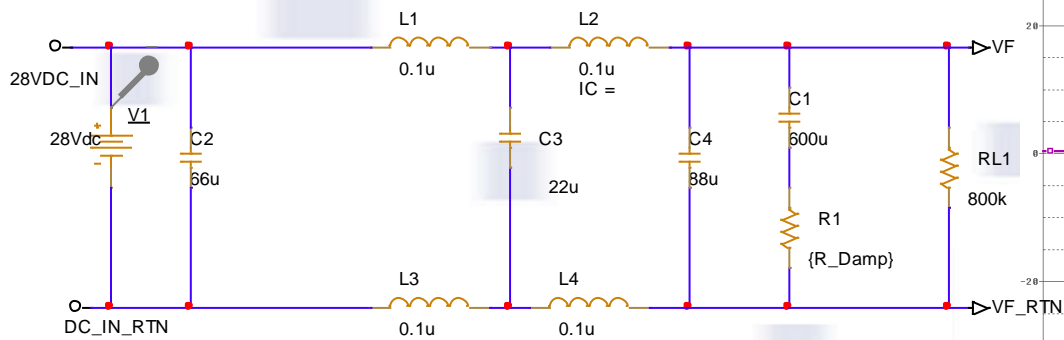
For this example, there is a 1 ohm impedance at 180° phase shift.



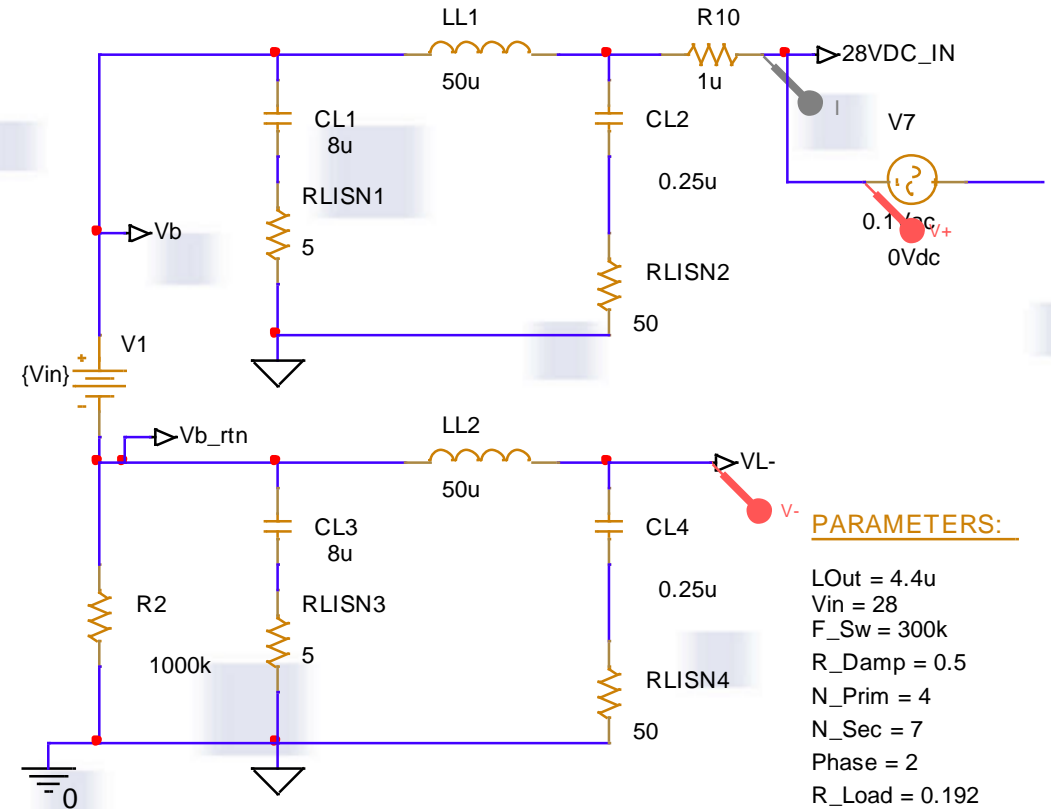
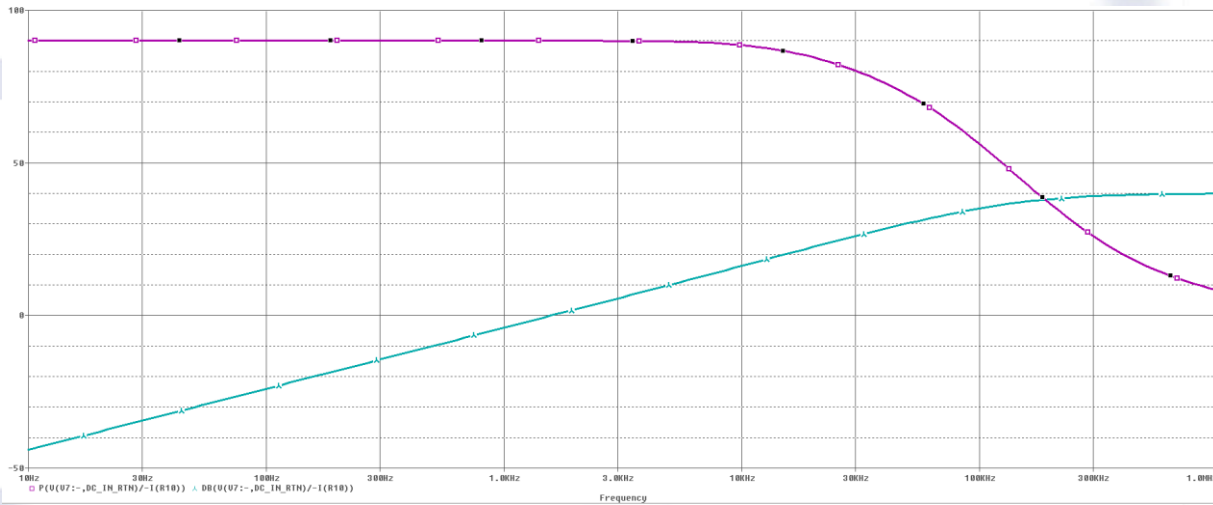
Input Filter Match

Typical EMI Filter matched with Ideal Source

10db Target Margin is Achieved

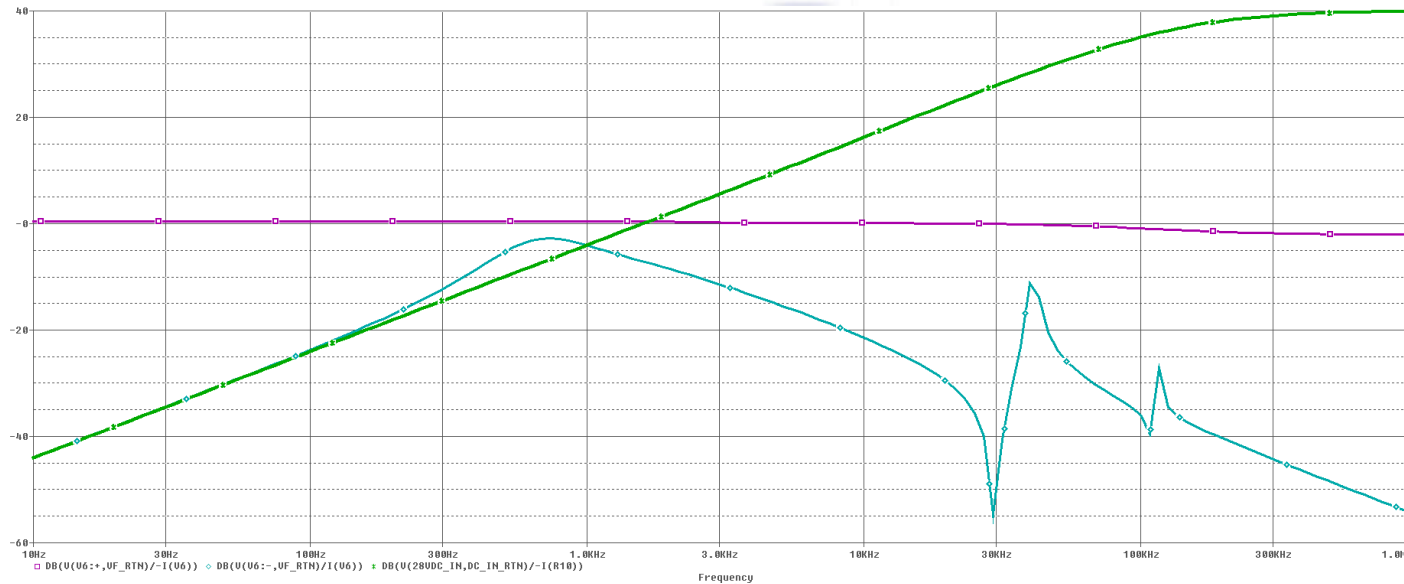


Impedance of LISN Circuit



- 0db Ohms at 1.59kHz
- Breakpoint at 147 kHz

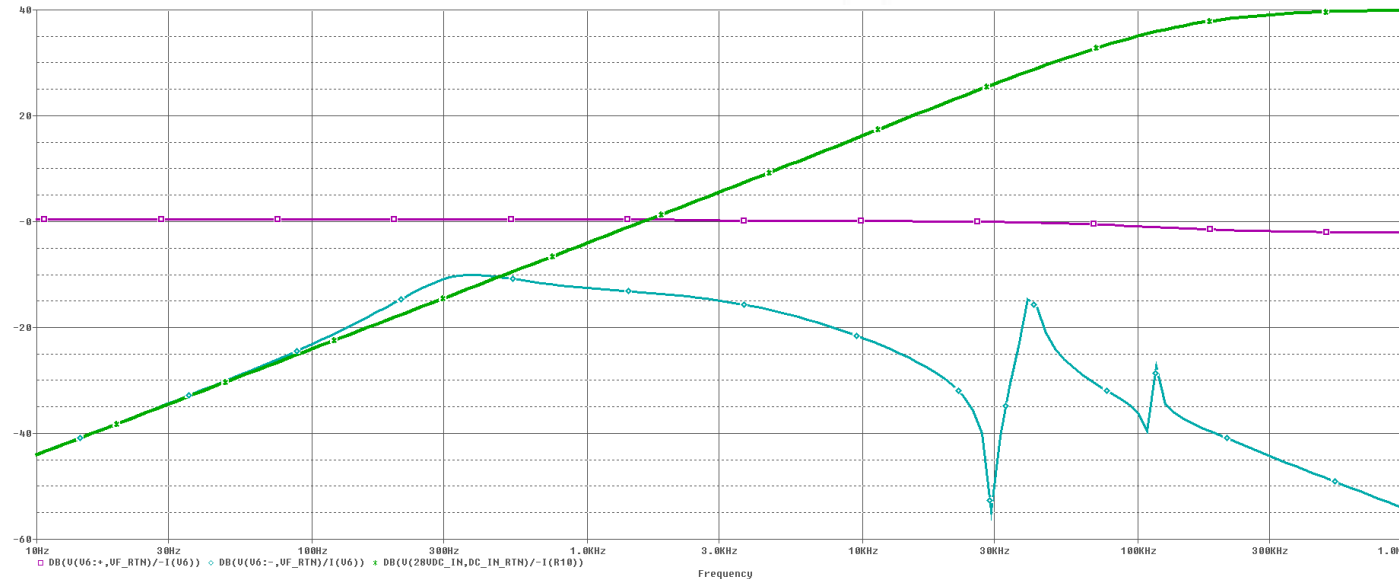
Impedance Match with LISN Added to Input



LISN Impedance
Shown in Green for
Reference

- Margin is reduced from 10db to less than 3db
- A New Low Frequency Resonance is Introduced.
- **The LISN Impedance has become the Dominant Limiting Design Factor.**
- Must Re-Select the Dampening Network to Account for the LISN

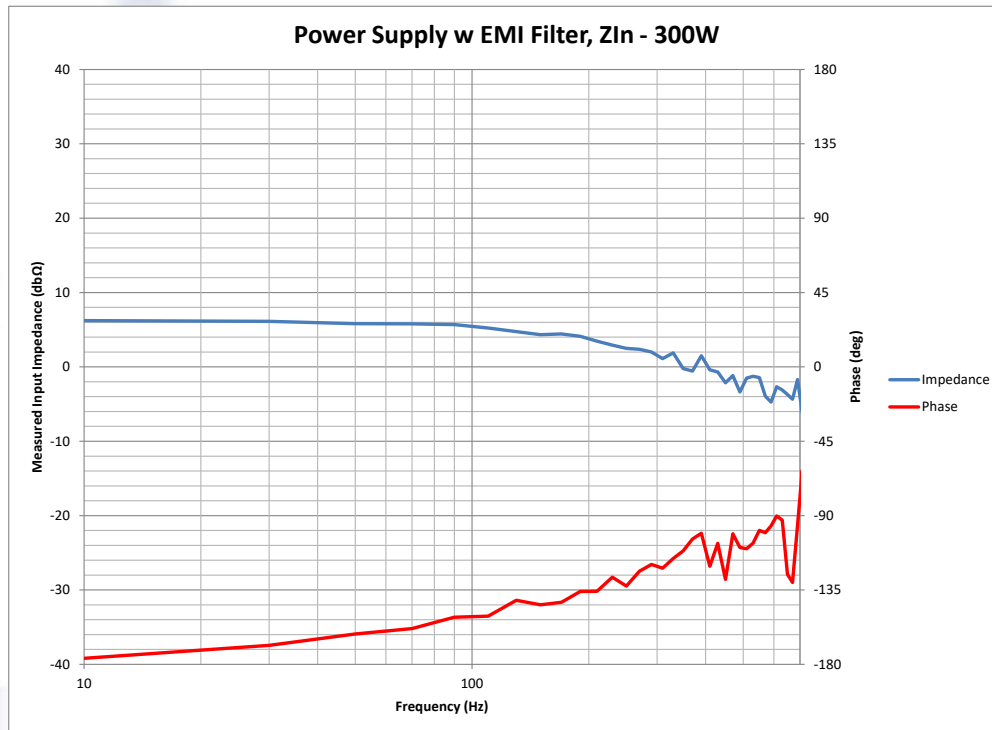
Impedance Match with Updated Dampener



LISN Impedance
Shown in Green for
Reference

- Target LF Resonance to occur where LISN is 15db Lower than the converter. 300Hz.
 - This allows for some level of Q Factor.
- Calculate Dampening Resistor to Provide 10db Margin. $R_D = -10\text{db}\Omega * 0.707 = 0.22\Omega$
- Calculate Dampening Cap to Resonate at 300Hz. $C_D = \frac{1}{2\pi f X_C} = \frac{1}{2\pi * 300 * 0.22} = 2400\mu\text{F}$
- 10 db Margin is restored.

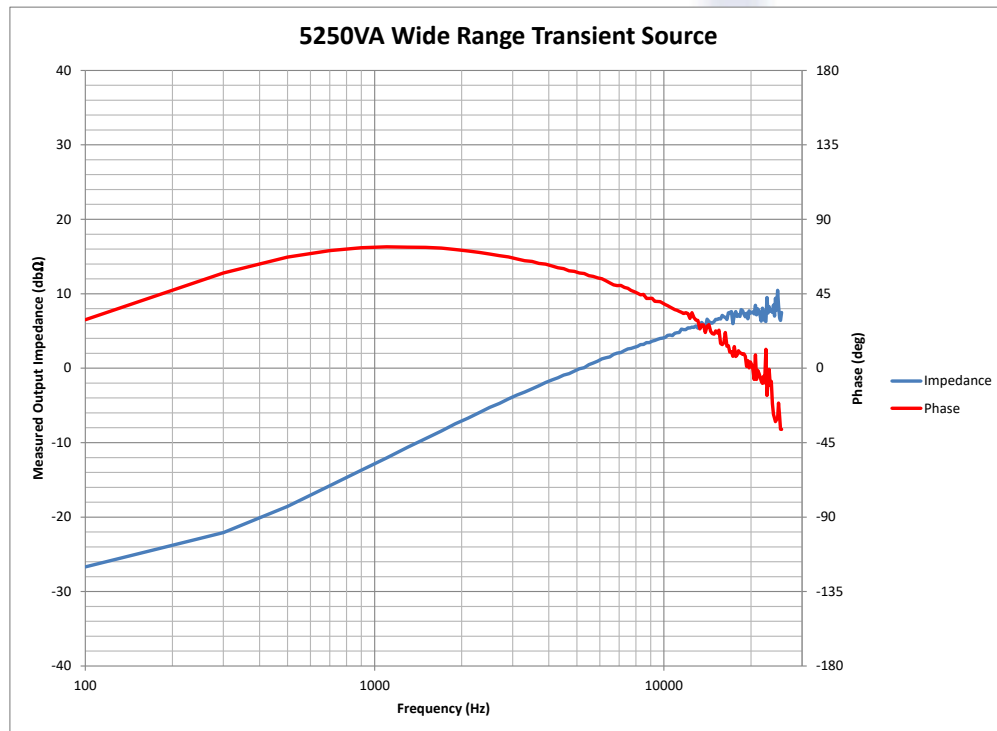
Power Supply Input Impedance With EMI Filter



- Input Impedance Measurements Are Taken on a Similar Power Supply with a 350W Load.
- The Dominant Breakpoint is a Result of the Dampening Network.
- We must now Match this to our power source.

Power Source Impedance is a Concern

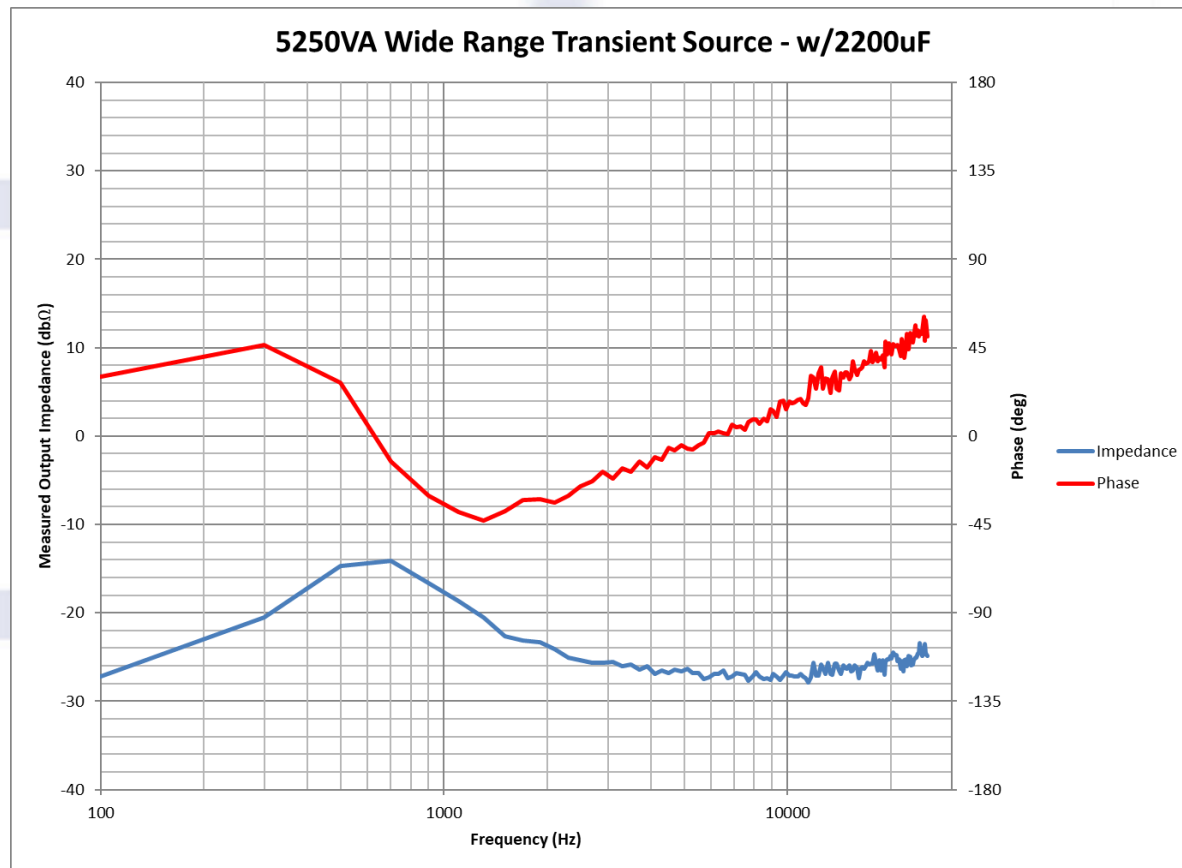
- Many 0-60V Sources Have Acceptable Output Impedance for their expected Load Range.
- Wide Range Sources Designed for Transient Testing Need to be Evaluated.



- The Graph shows the Measured Impedance of a 5.25KW Transient source.
- It will have difficulty Powering a 750W+ Power Supply.
- Crosses 0dbΩ at 5kHz
- Violates 10db Margin at 1.5kHz
- Wide Range Sources are also designed for High Voltage Transients. Manufacturers are reluctant to install low impedance components.

Working with Wide Range Sources

- When Using Low Range Mode – Add a High Capacitance to the Output

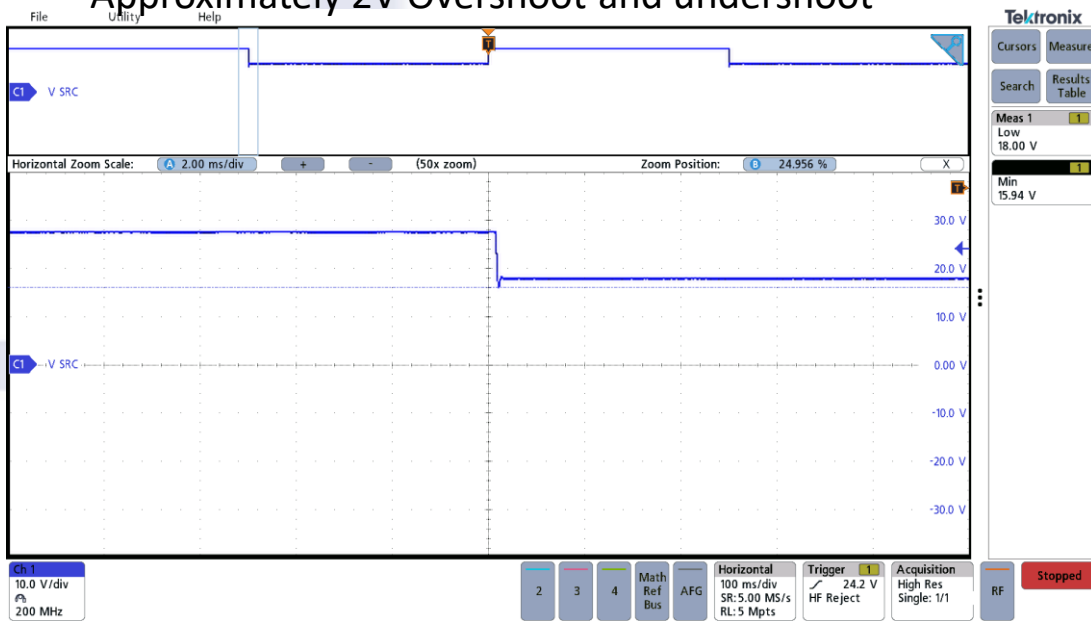


- Impedance is Dramatically Reduced.
- Dominated by the added Capacitor for most of the range.
- Resonance Occurring at 600Hz.

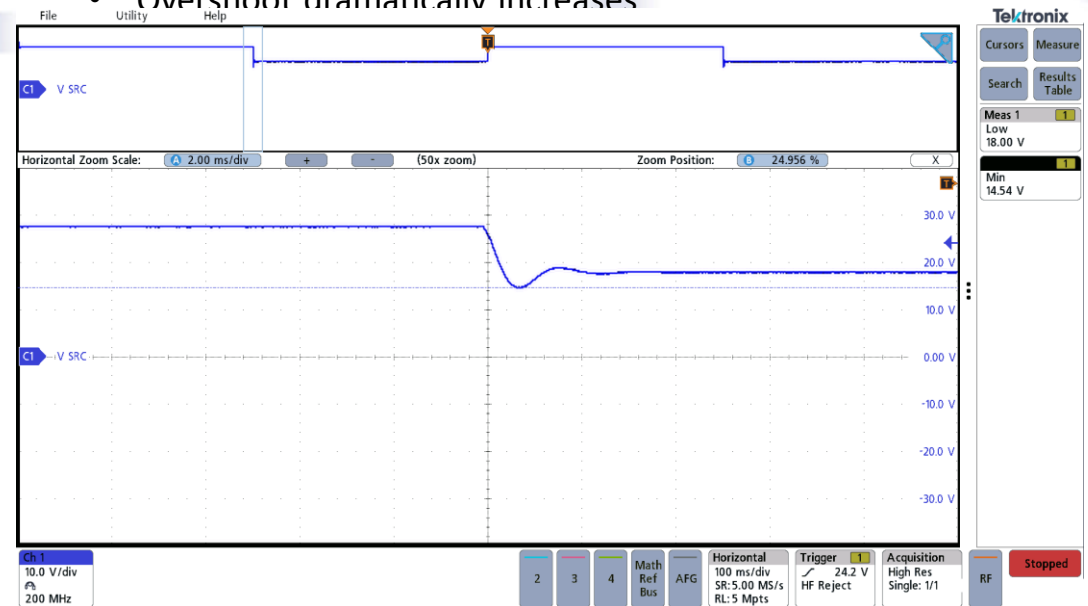
Effect on Performance

- Adding this Capacitor does not come without a cost
- It interferes with the basic function of the Transient Generator.

- 5250VA Transient Generator 5A load No Capacitor
- Approximately 2V Overshoot and undershoot

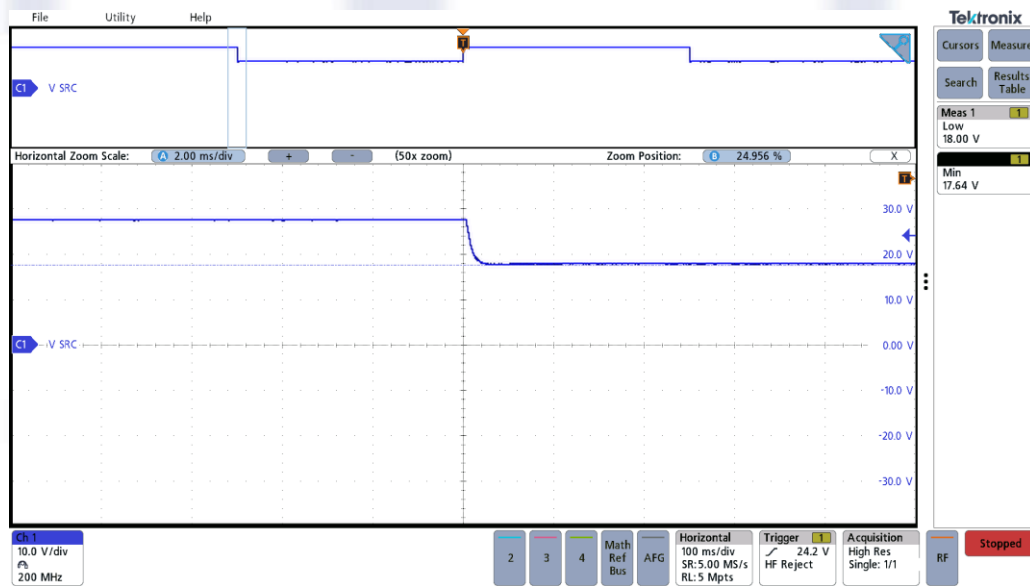


- 5250VA Transient Generator 5A load with 2200uF Capacitor.
- Edges are Slowed
- Overshoot dramatically increases

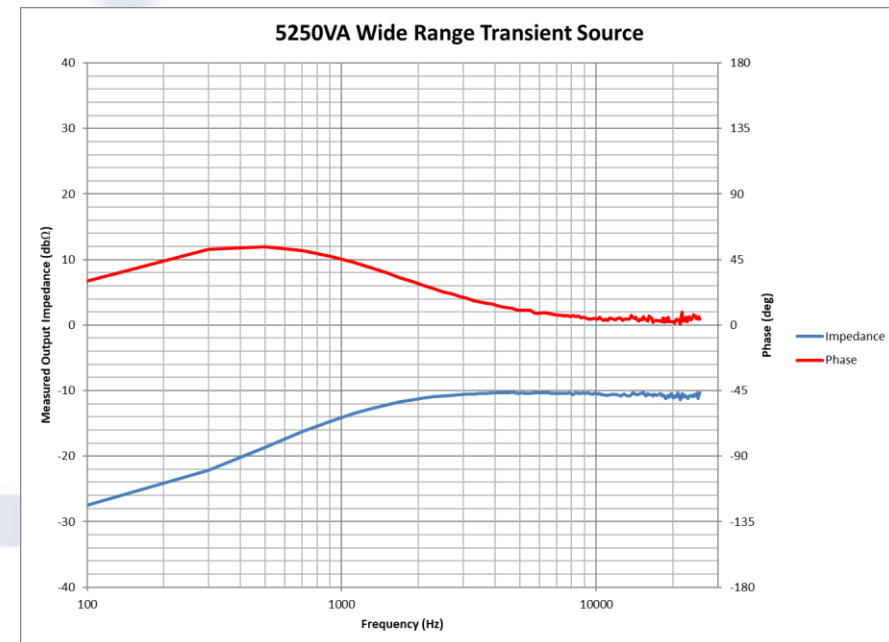


Minimize Over-Shoot

- Compromise by adding series RC instead of pure Capacitor.
- Reduces Load on the source.
- Reduces Source impedance for Downstream Power Supply
- 5250VA Transient Generator w/2200u and 0.3Ω Dampener



- Impedance Match Acceptable.
- Eliminates Overshoot and improves Slew Rate.
- Limits Peak Load
- Dampening Resistor Must be Robust – Desing for Ip being Continuous.



A Word of Caution for Dampeners

- Make sure Dampeners are properly sized.
 - This applies for Internal Dampeners and Dampeners that are part of a test setup.
- The Change in energy level in the dampening capacitor will be dissipated in the dampening resistor for every transient.
- Conducted susceptibility testing will add stress to dampening components.

Review – Topics that were covered.

- Power Supplies Present a Negative Input Impedance.
- Impedance Matching Needs to be Considered.
- An Average Model for Voltage Mode for SPICE has been provided.
- A real time SPICE division Emulator was presented.
- A method for Emulating Average Duty cycle for current mode controller was presented.
- ‘Middlebrook Criterion’ from MIL-HDBK-241 was referenced.
- LISN Impedance Identified as a Major Design Consideration.
- Impedance of Transient Power Sources need to be Evaluated.
- Expect to Add Dampening Networks to High Impedance Power Sources.