Mixed-Signal Systems-on-Chip: Architectures and Design Tools

Alex Doboli, PhD

Associate Professor

Department of Electrical and Computer Engineering

State University of New York, Stony Brook, NY 11794

Email: adoboli@ece.sunysb.edu

The “Wish List”

- A new development paradigm that:
  - Much more efficient design methodologies
  - Higher Level Of Abstraction For Development
  - Exploit design reusability & retargeting
  - Frees Designers From Low Level Implementation Details
  - Produces Interoperable And Portable Designs
  - Supports Reconfigurability
  - Provides Extensive, and Extensible, Third-Party Device Libraries
  - Is Self-Documenting
  - Is scalable and extensible

Research, Entrepreneurial & Educational Challenges

- **High-level AMS synthesis?**

Stephan Ohr, "Synthesis proves to be Holy Grail for analog EDA", EE Times, 06/08/1999

Research, Entrepreneurial & Educational Challenges

- AMS design is “art” and less “science”
  - Theory? Methodology? How to invent application-specific topologies & circuits?
- Architectures?
- Few CAD tools (mostly simulators: SPICE etc.)
  - Transistor is not a switch! (modeling)
  - Design usually at a low level (transistors, layout)
- Who will develop the architectures & tools?
- Who designs AMS systems? EE/CE/CS/all?

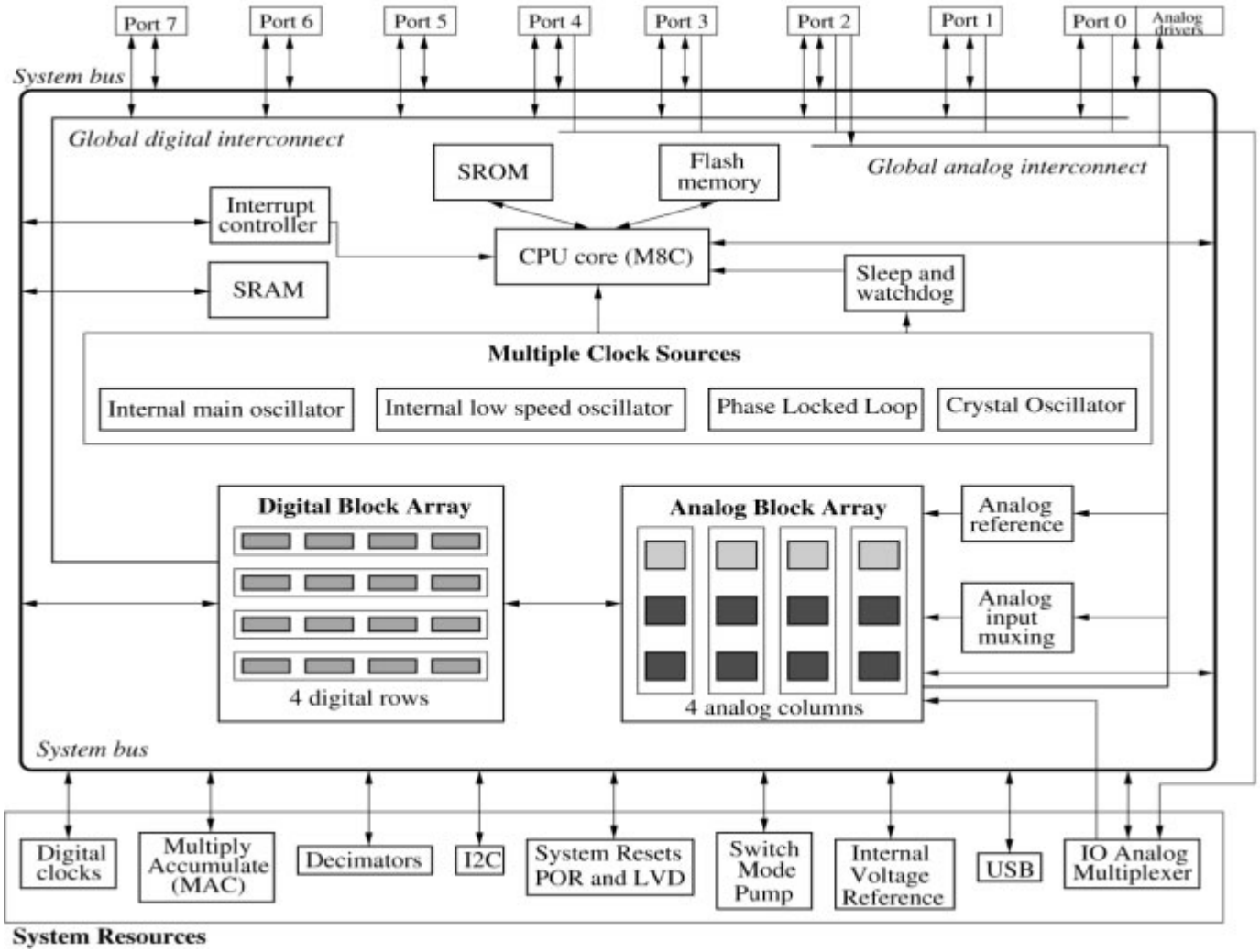
Presentation outline

- PSoC: embedded mixed-signal architecture
- Related research at Stony Brook
- Systematic methodology for $\Delta\Sigma$ ADC design
- Automated circuit modeling
- Education & training
- Conclusions

Embedded Mixed-Signal Architectures

- Cypress' programmable PSoC mixed-signal SoC
- Main features:
  - Hardware programmability
    - Programmable analog blocks
    - Programmable digital blocks
    - Programmable interconnect
    - Programmable I/Os
    - Programmable clocks
    - Selectable power supply
  - Integration as an SoC

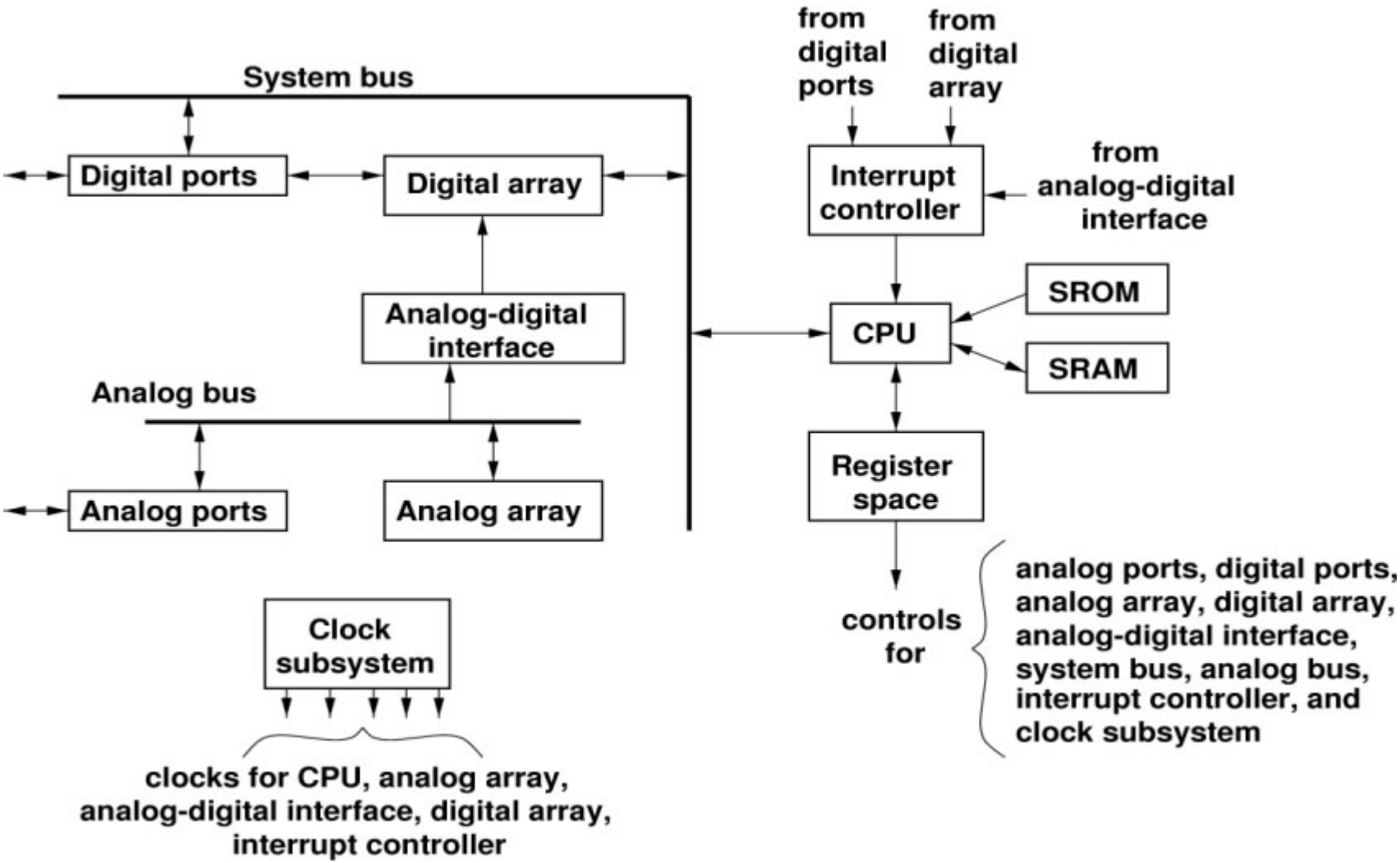
PSoC Mixed-Signal Architecture



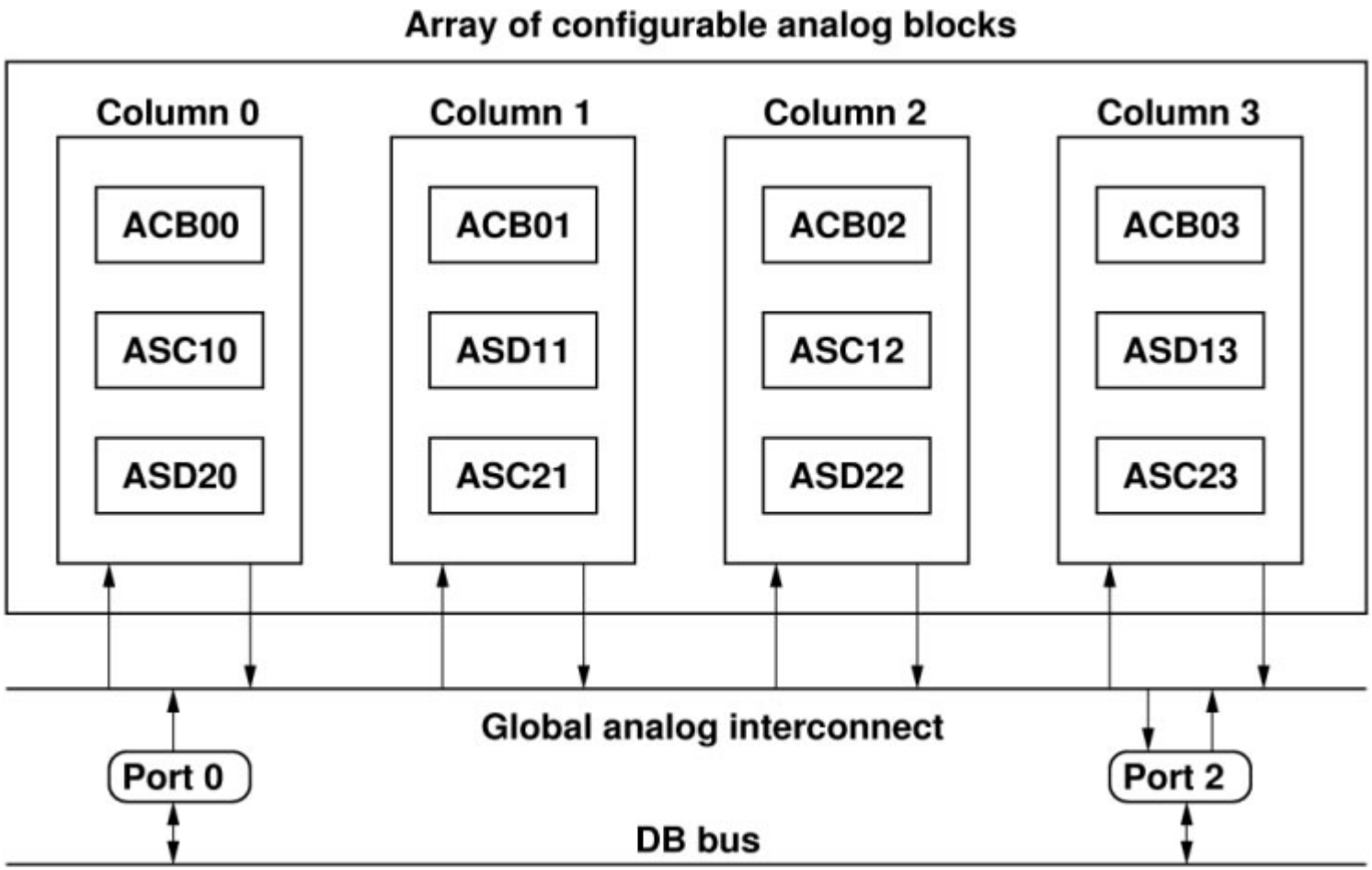
Why PSoC-like architectures ?

- **PSOC supports/helps:**
  - **Design reusability & retargeting (library)**
  - **Predictable performance (library of models)**
  - **Frees designers from low level implementation (pre-characterized cells)**
  - **Supports Reconfigurability**
  - **Supports extensive, and extensible, third-party device libraries**
  - **Is scalable and extensible (programmable transceivers, PLLs, software radio)**

PSoC Mixed-Signal Architecture



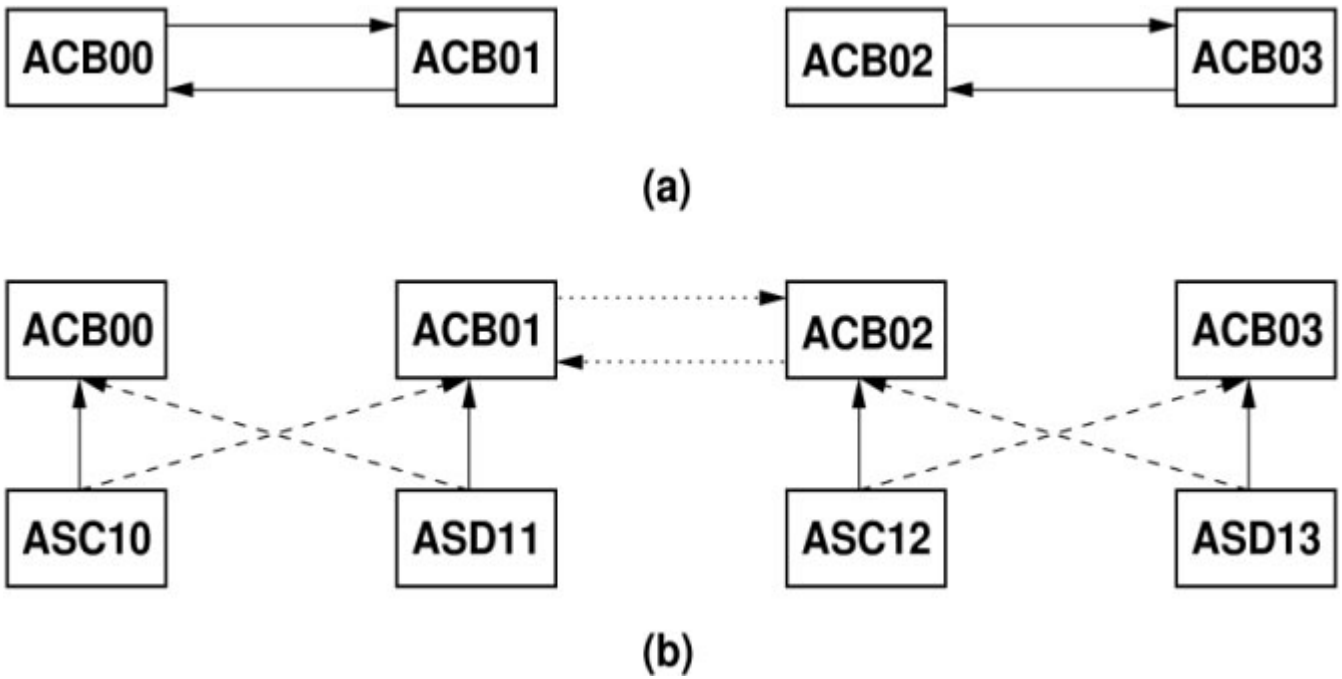
PSoC Mixed-Signal Architecture



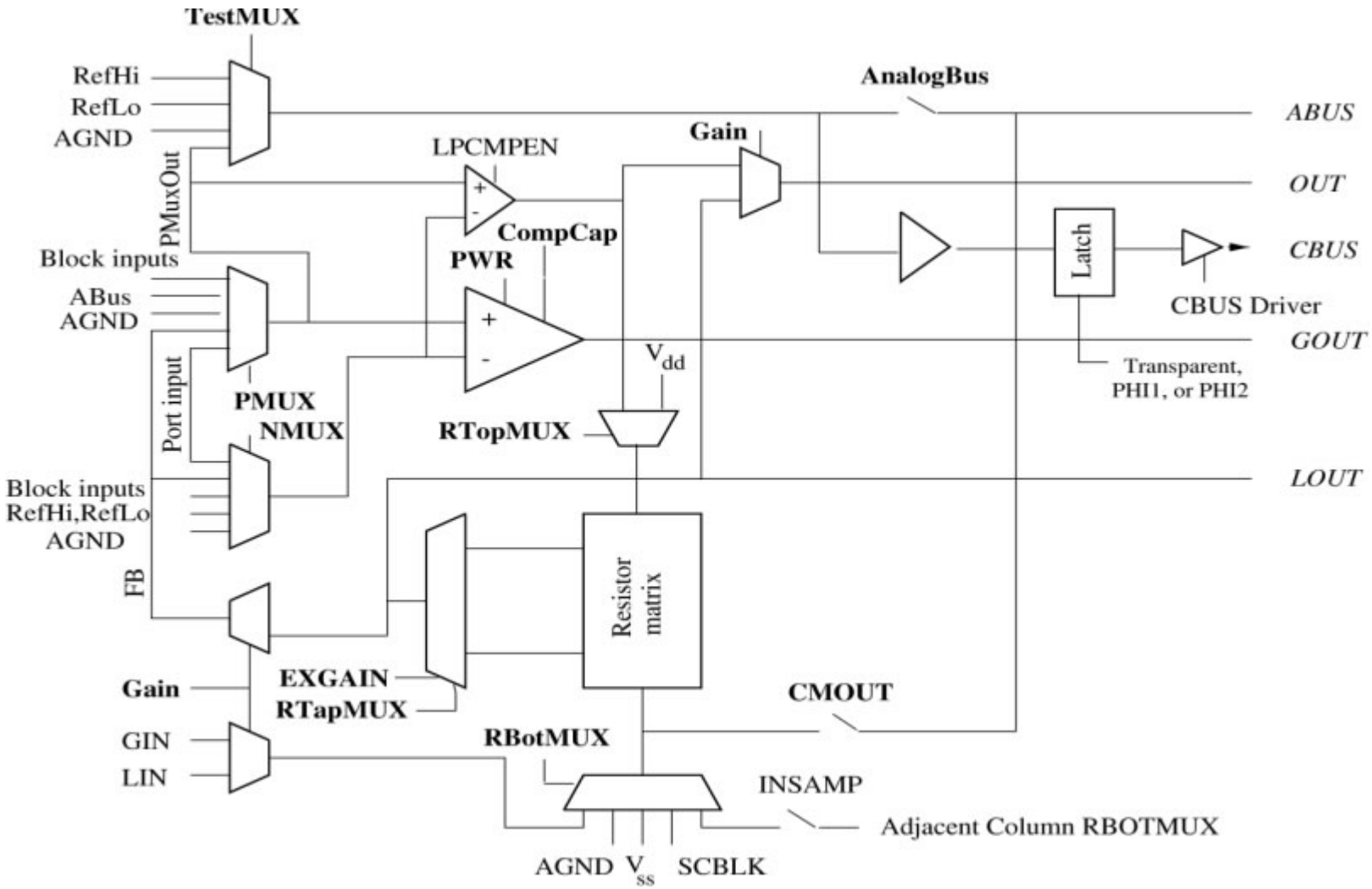
PSoC Mixed-Signal Architecture

- Analog blocks are programmable
  - Programmable functionality (control registers)
  - Programmable inputs & outputs
- Analog blocks of two types
  - Continuous time blocks
  - Switched capacitor blocks (type C and type D)
- Connected to programmable I/O ports
- Programmable interconnect
  - Three kind of programmable interconnect

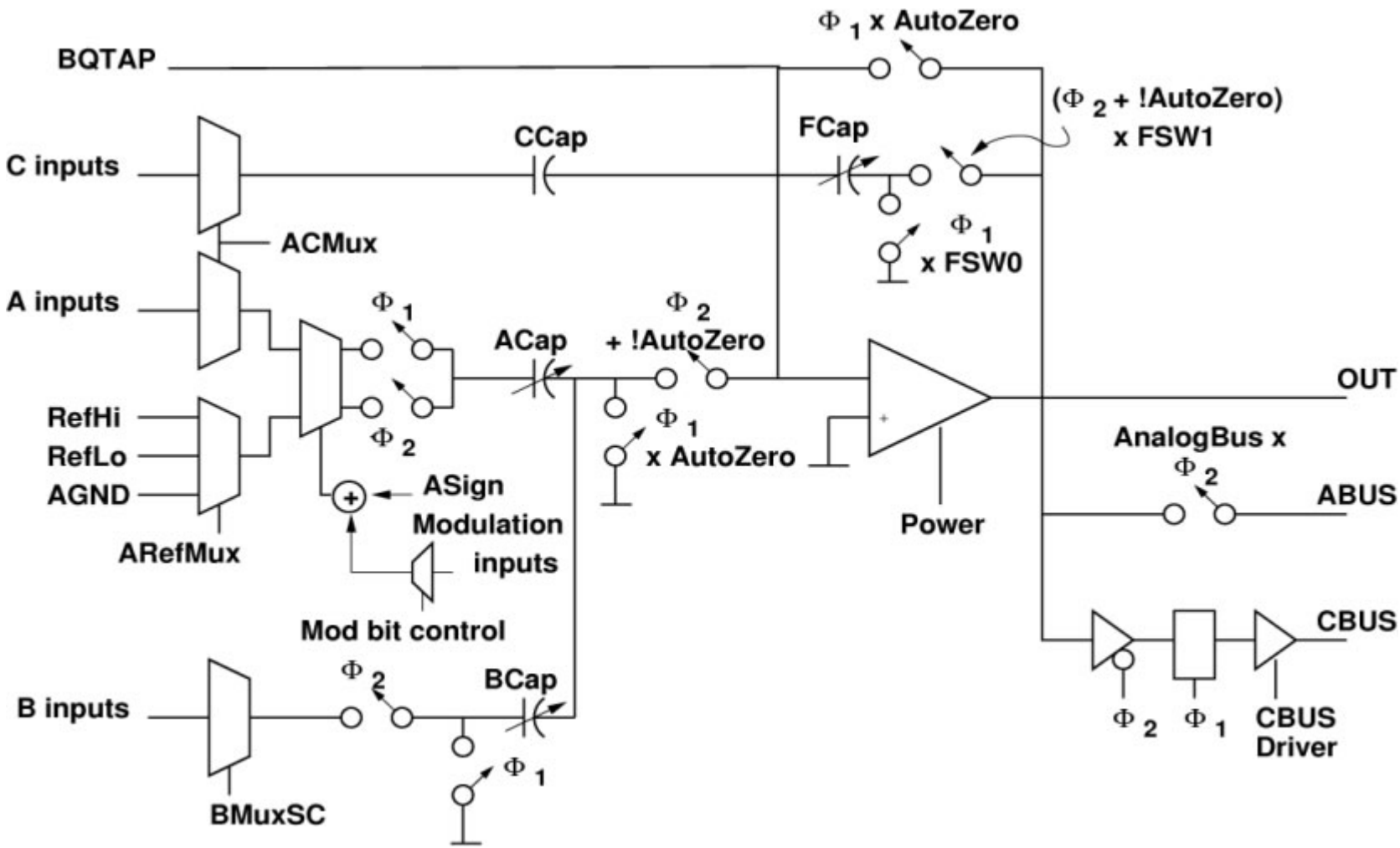
Programmable interconnect



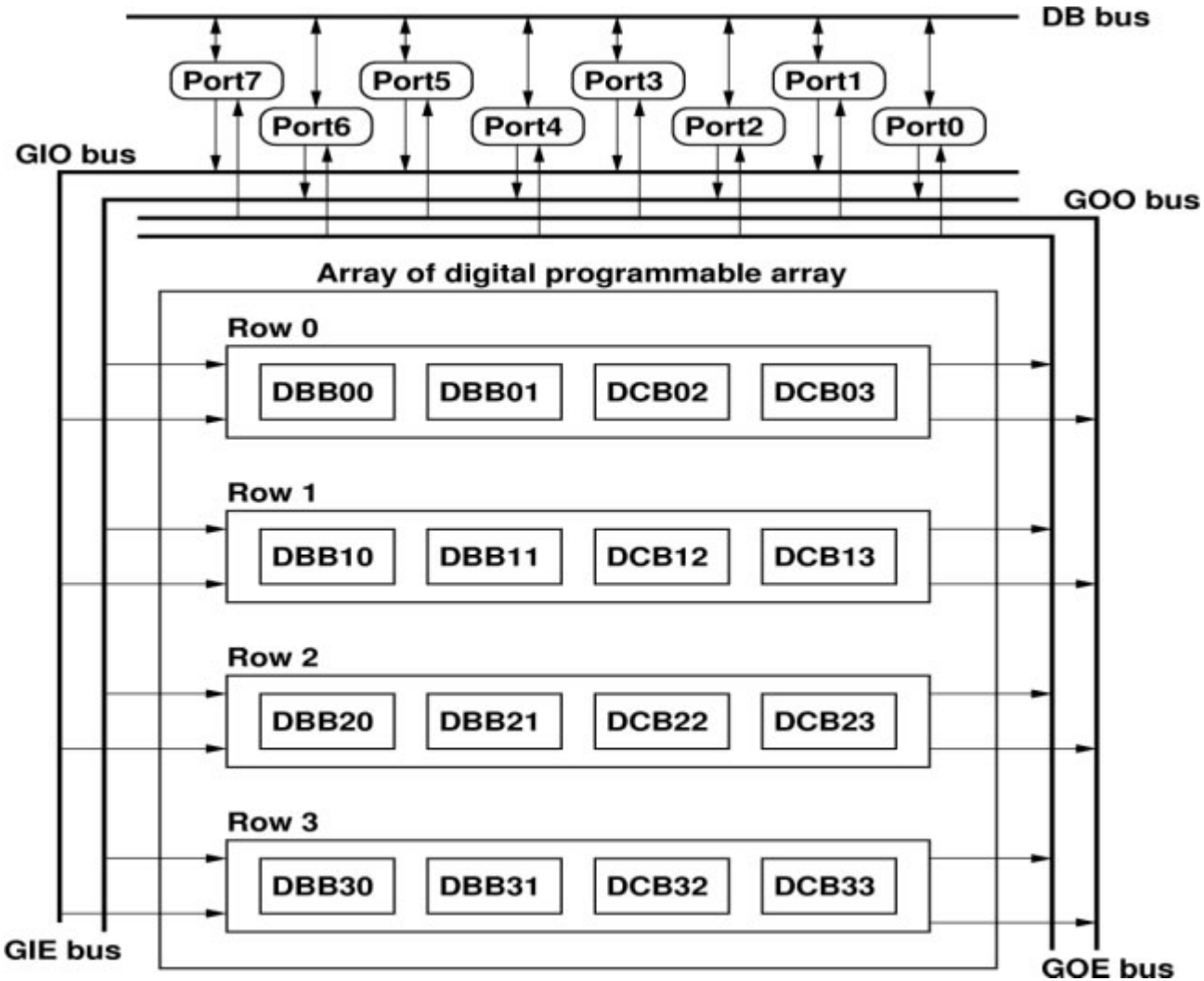
Programmable CT blocks



Programmable SC blocks



PSoC Mixed-Signal Architecture



Some CAD related Issues

- **Higher Level Of Abstraction For Development**
  - What behavioral descriptions are synthesizable? DAEs, TFs, SFGs?
  - How do you correctly mix together continuous time and discrete time descriptions?
  - What standard specification notations? VHDL-AMS, Verilog-A, MATLAB/SIMULINK, UML?
- **Frees Designers From Low Level Implementation Details**
  - How do you synthesize a set of DAEs? (application-specific topologies)
  - Does the design work? (circuit modeling)
  - CAD tools for transistor sizing and layout (Neoliniar CADENCE)
- **Supports Reconfigurability**
  - Reconfigurable AMS architectures, reconfigurable ADCs, filters

VLSI System Design Laboratory

(http://www.ece.sunysb.edu/~vsdlab)

Lab director: Dr. Alex Doboli,

Email: adoboli@ece.sunysb.edu,

Phone: 631-632-1611

Lab expertise:

- Embedded mixed-signal systems
- CAD for system&circuit optimization
- Analog circuit modeling
- IP core integration

Academic results:

- 3 PhDs graduated
- 3 MS graduated
- 19 journal papers
- 65 peer reviewed conference papers

IC Developments:

- **Rhapsody** CAD tool (ADC design)
- **ISIS** CAD tool (SoC integration)
- **SoC** design in 0.18μm process

Research funding (since 2001):

- NSF Center for Design of Analog and Digital IC
- AFRL
- NSF ITR
- DARPA, IBM, DAC, Cypress

VLSI System Design Laboratory

(http://www.ece.sunysb.edu/~vsdlab)

- **G. Gielen, R. Rutenber, "Computer-Aided Design of Analog and Mixed-Signal Integrated Circuits", Proceedings of IEEE, Vol. 88, No. 12, pp. 1825-1852, 2000:**

"Recently, a first attempt was presented towards the full behavioral synthesis of analog systems from (annotated) VHDL-AMS behavioral descriptions".

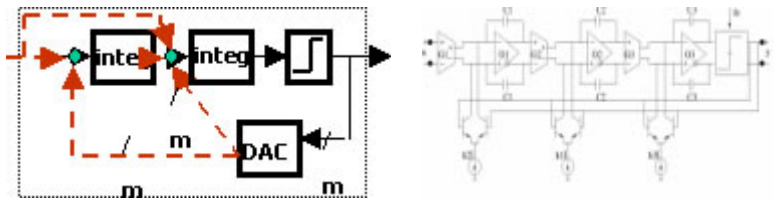
- **A. Doboli, R. Vemuri, "*Behavioral Modeling for High-Level Synthesis of Analog and Mixed-Signal Systems from VHDL-AMS*", IEEE Transactions on CADICS, Vol. 22, No. 11, 2003, pp. 1504-1520. (among the most downloaded papers in 2005)**

Rhapsody: Automated design of analog and mixed-signal systems

VHDL-AMS specifications:

```
entity aaa is
…
end entity;
```

Topology generation and system architecture selection:

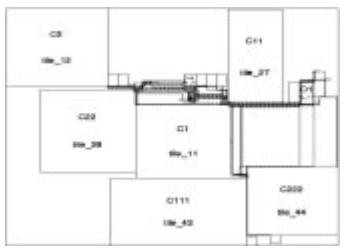


Performance evaluation

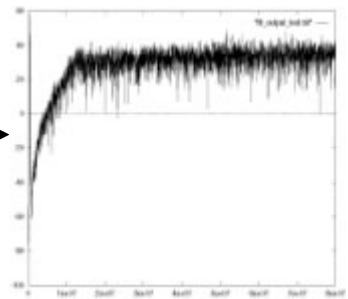
Circuit and interconnect models

Performance evaluation (simulation)

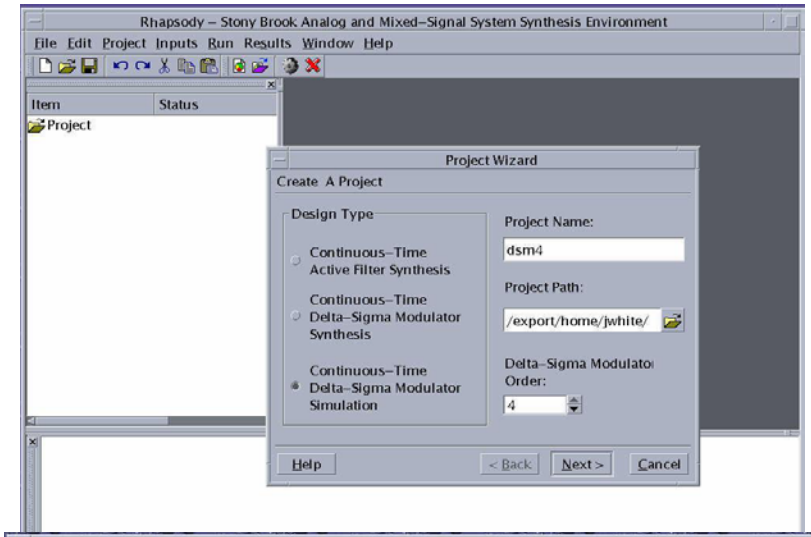
Constraint transformation, floorplanning and global routing

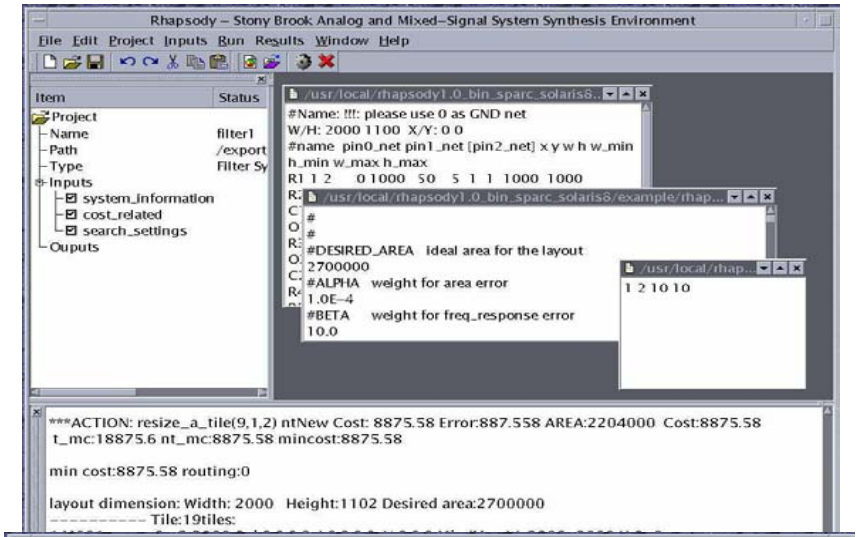


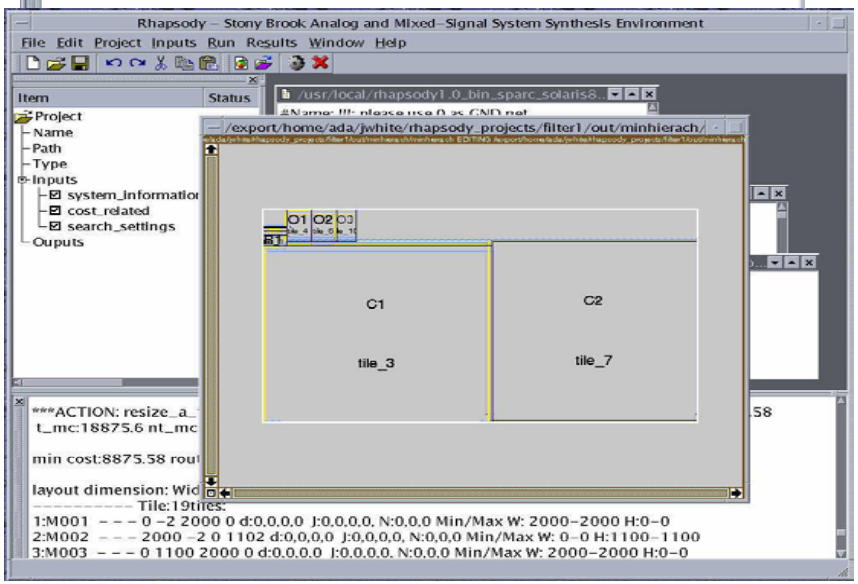
Obtained performance

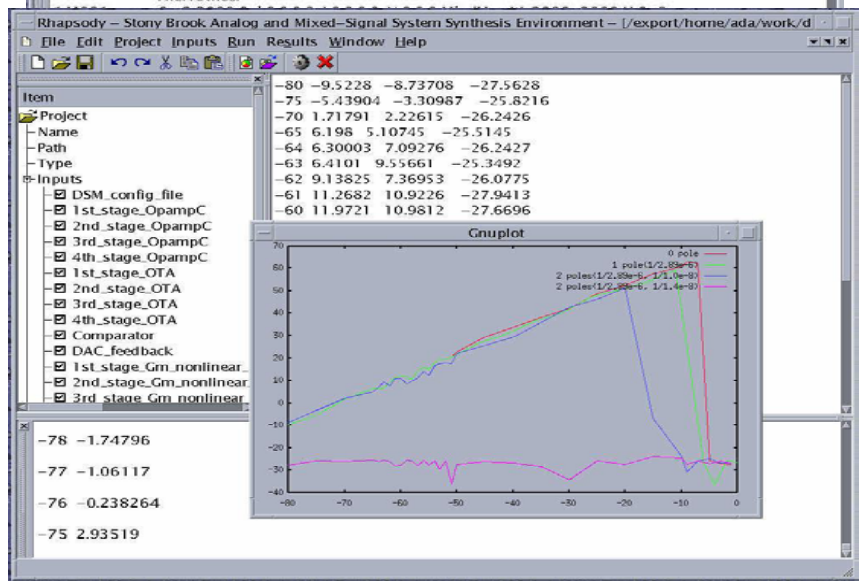


Rhapsody (snapshots)









Benefits

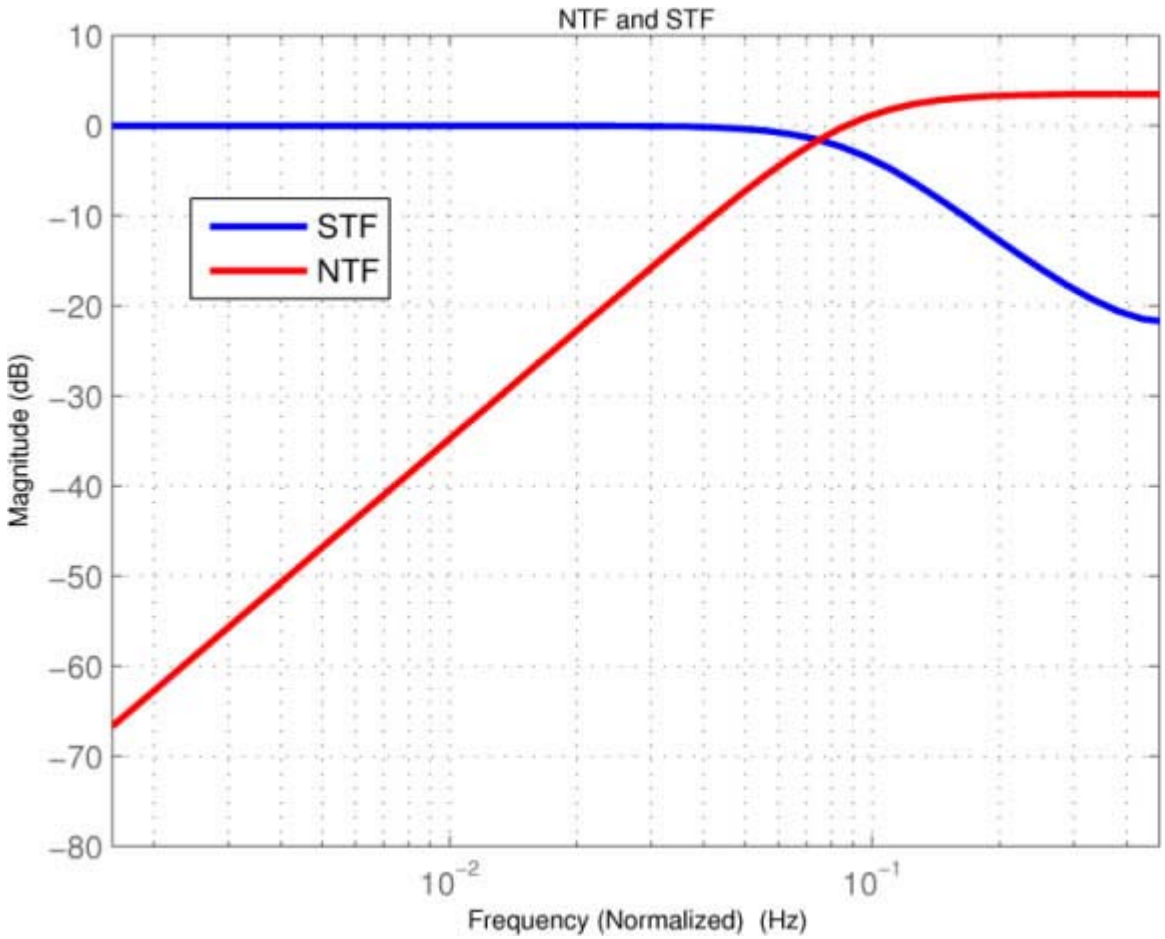
Quality:

- Complements SD toolbox (finding NTF and STF), Cadence's NeoCircuit (transistor sizing) and NeoCell (layout generation)
- Produces SD topologies customized to performance specific requirements
  - less complex, better sensitivity to parameter variations, and lower power consumption
- Finds 6x-10x more constraint-satisfying solutions than CircuitExplorer (Synopsis) and NeoCircuit (Cadence)

Effort:

- Designs (including circuit sizing using NeoCircuit and layout using NeoCell) can be ready much faster
- Designers can focus on more challenging issues, like system topology, selecting circuits
- Can be used by less-experienced designers
- Prototyping of new applications, e.g., reconfigurable SD ADC

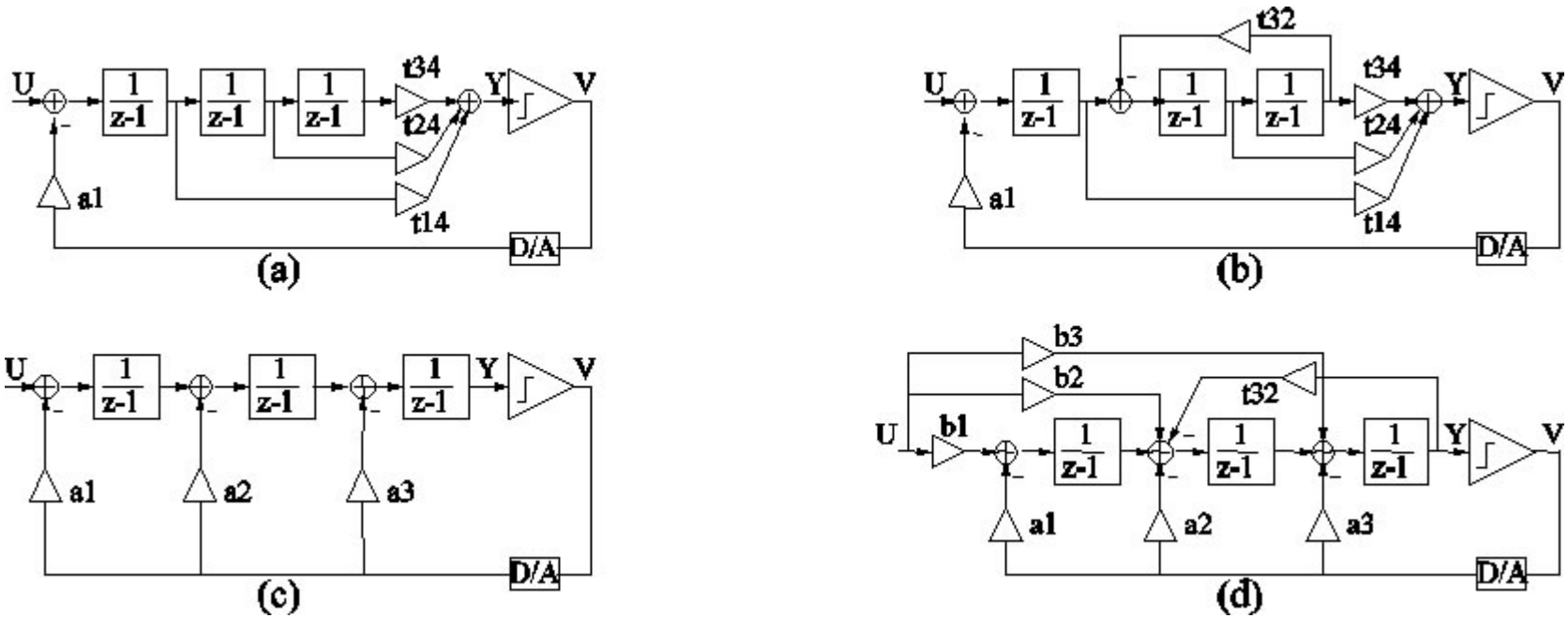
Application-specific $\Delta\Sigma$ modulator topologies



Application-specific $\Delta\Sigma$ modulator topologies

- **The topology is an SFG containing *integrators* and having all *signal paths* and *coefficients* of the signal paths defined**
- **A topology differs from another one in terms of**
  - **the type of the integrator**
  - **signal paths definition**
  - **numerical coefficients of the signal paths**
- **For topology synthesis, they are the control parameters and uniquely determine a topology**

Traditional ΔΣ modulator topologies



3rd order Delta-Sigma modulator topologies

(a) Chain of Integrators with Feedforward Summation

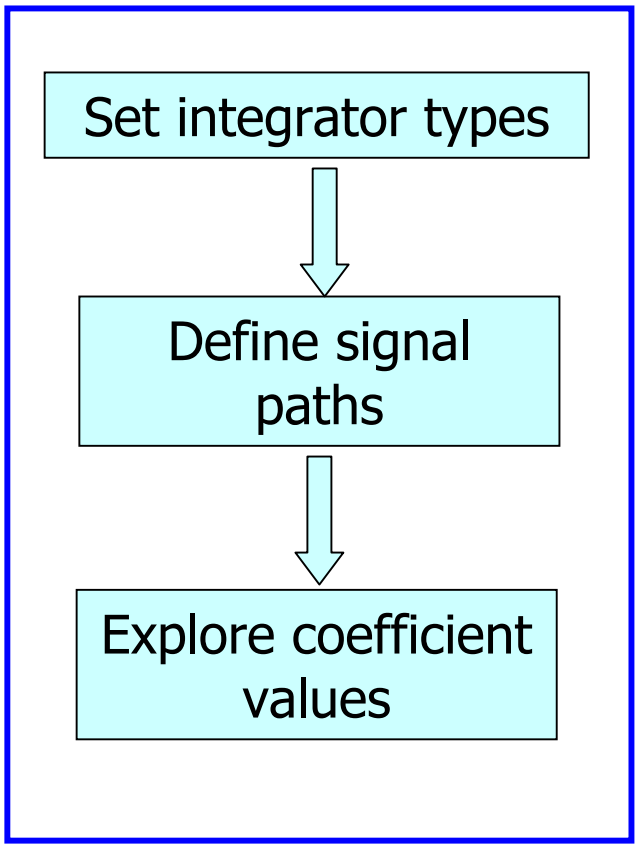
(b) Chain of Integrators with Feedforward Summation and Local Feedback

(c) Chain of Integrators with Distributed Feedback

(d) Chain of Integrators with Distributed Feedback, Distributed Feedforward and Local Feedback

Previous work: I

F. Medeiro, A. Verdu, A. Vazquez, "Top-down Design of High Performance Delta-Sigma Modulators", *Kluwer*, 1999

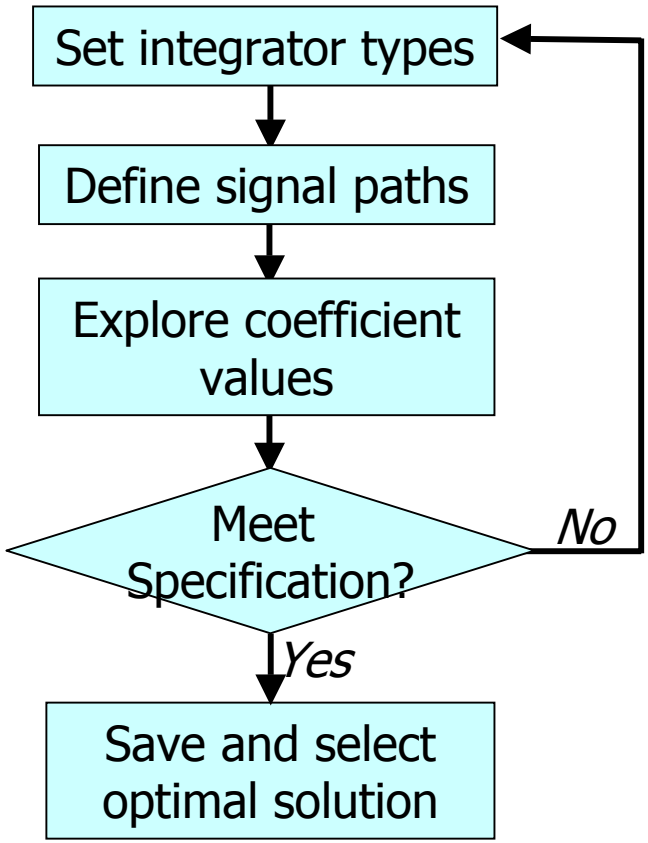


An incomplete topology is defined

- **Designers have to select an incomplete topology based on experience**
- **Coefficient design is the only degree of freedom to be explored.**

Previous work: II

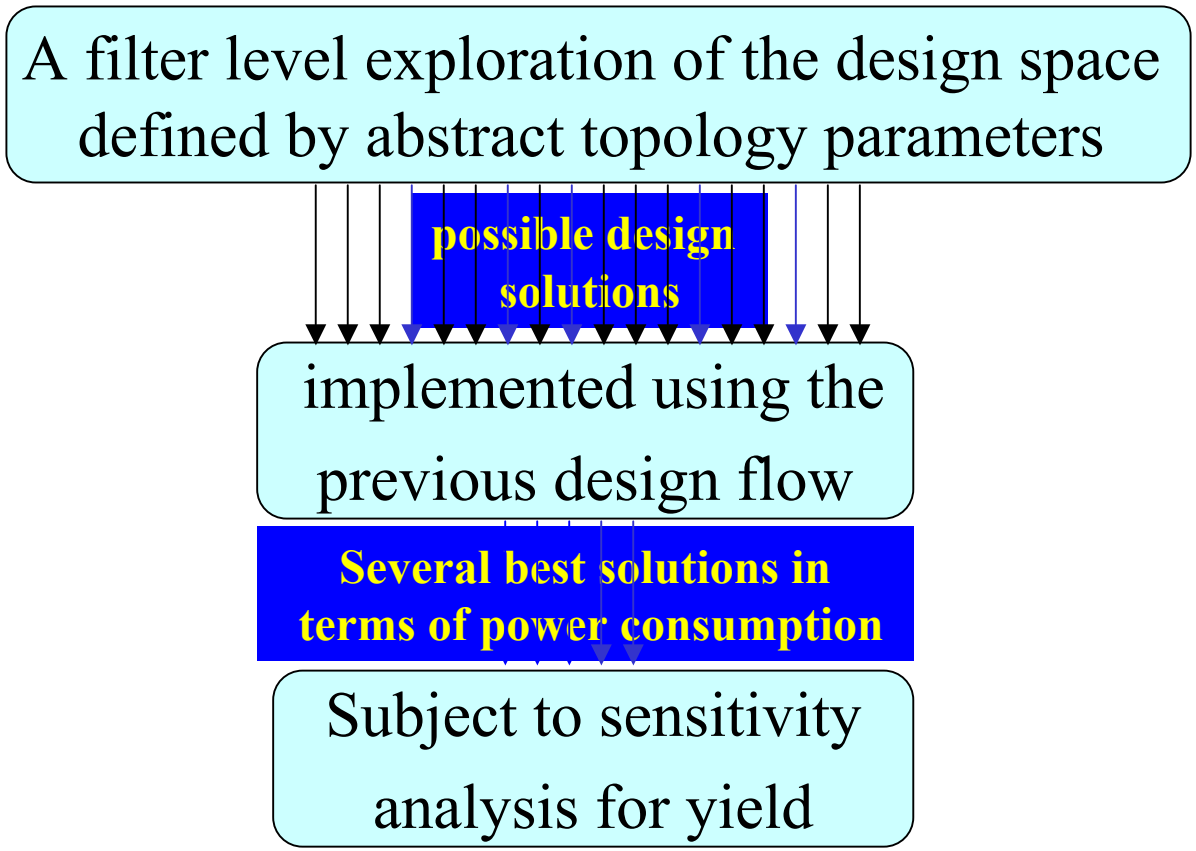
K. Francken, G. Gielen, "A High-level Simulation and Synthesis Environment for Delta-Sigma Modulators", *IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems*, Vol. 22, No. 8, 2003, pp. 1049-1061.



- **Selected incomplete topologies (or complete topologies) are stored in a library**
- **Given design specifications, such as SNR and DR, the tool selects one with the smallest power consumption**

Previous work: III

O. Bajdechi, G. Gielen, J. Huijsing, "Systematic Design Exploration of Delta-Sigma ADCs", *IEEE Transactions on Circuits and Systems I*, Vol. 51, No. 1, Jan 2004, pp. 86-95.



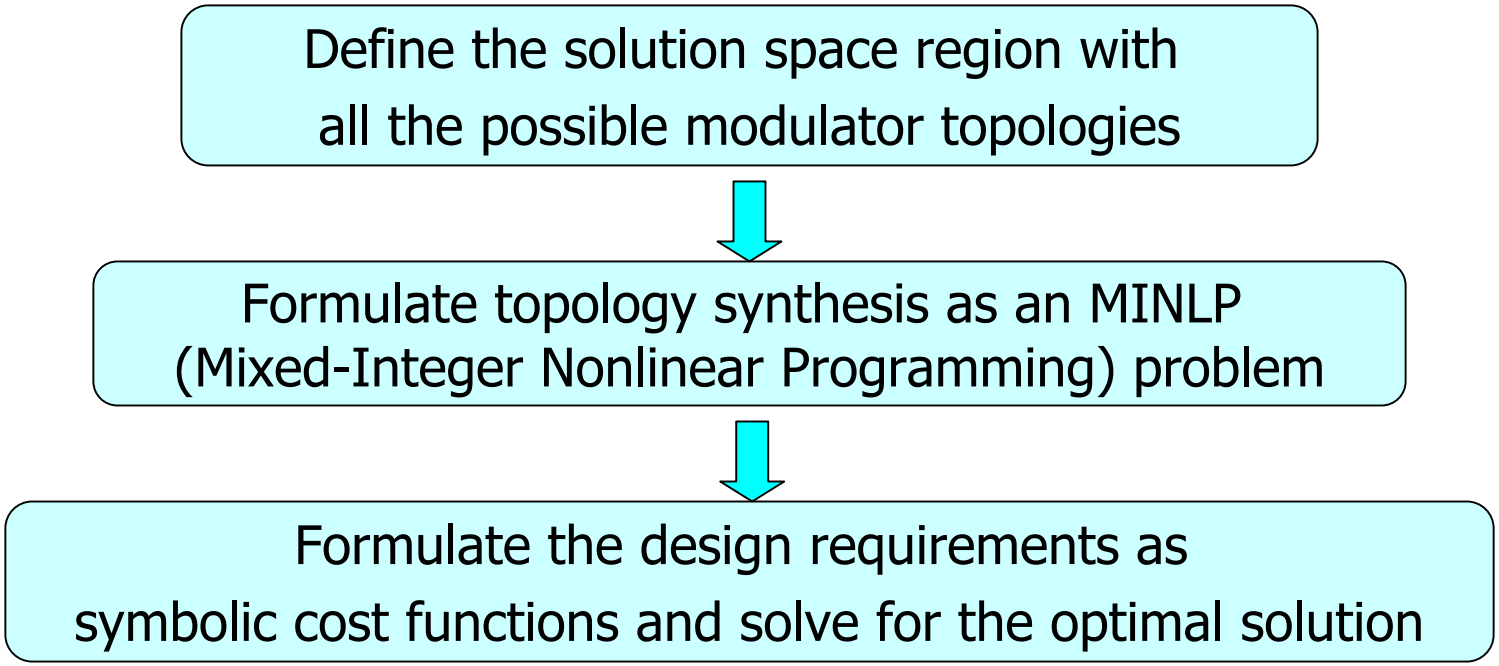
Application-specific ΔΣ modulator topologies

- **Y. Wei, H. Tang, A. Doboli, "*DATE06: Systematic Methodology for Designing Reconfigurable Delta Sigma Modulator Topologies for Multimode Communication Systems*", invited paper, IEEE Transactions on CADICS, accepted for publication.**

- **H. Tang, H. Zhang, A. Doboli, "*Refinement based Synthesis of Continuous-Time Analog Filters Through Successive Domain Pruning, Plateau Search and Adaptive Sampling*", IEEE Transactions on CAD of Integrated Circuits and Systems, Vol. 25, No. 8, pp. 1421-1440, August 2006.**

- **H. Tang, A. Doboli, "*High-Level Synthesis of Delta-Sigma Modulators Optimized for Complexity, Sensitivity and Power Consumption*", IEEE Transactions on CAD of Integrated Circuits and Systems, Vol. 25, No. 3, pp. 597-607, March 2006.**

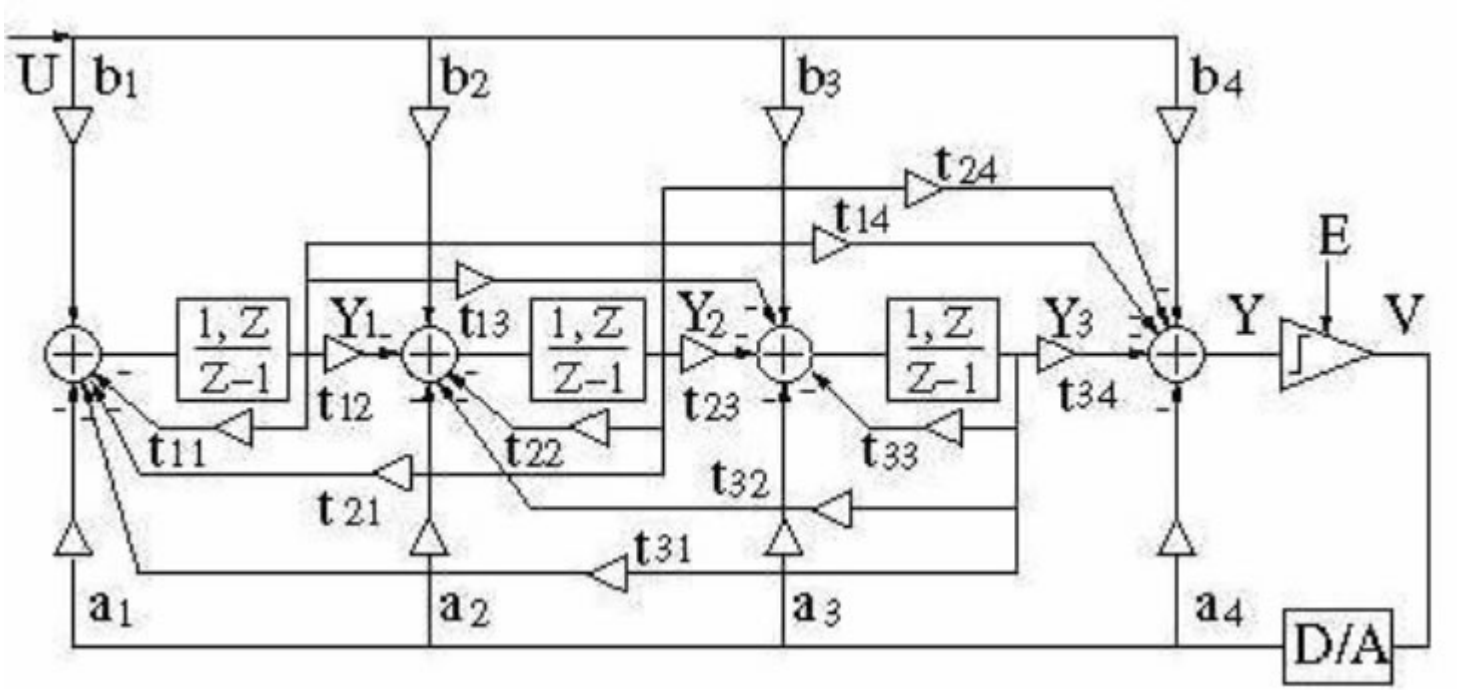
Proposed synthesis methodology



Advantages:

- Global optimal solution is guaranteed
- The methodology is scalable
- The methodology could be fully automated

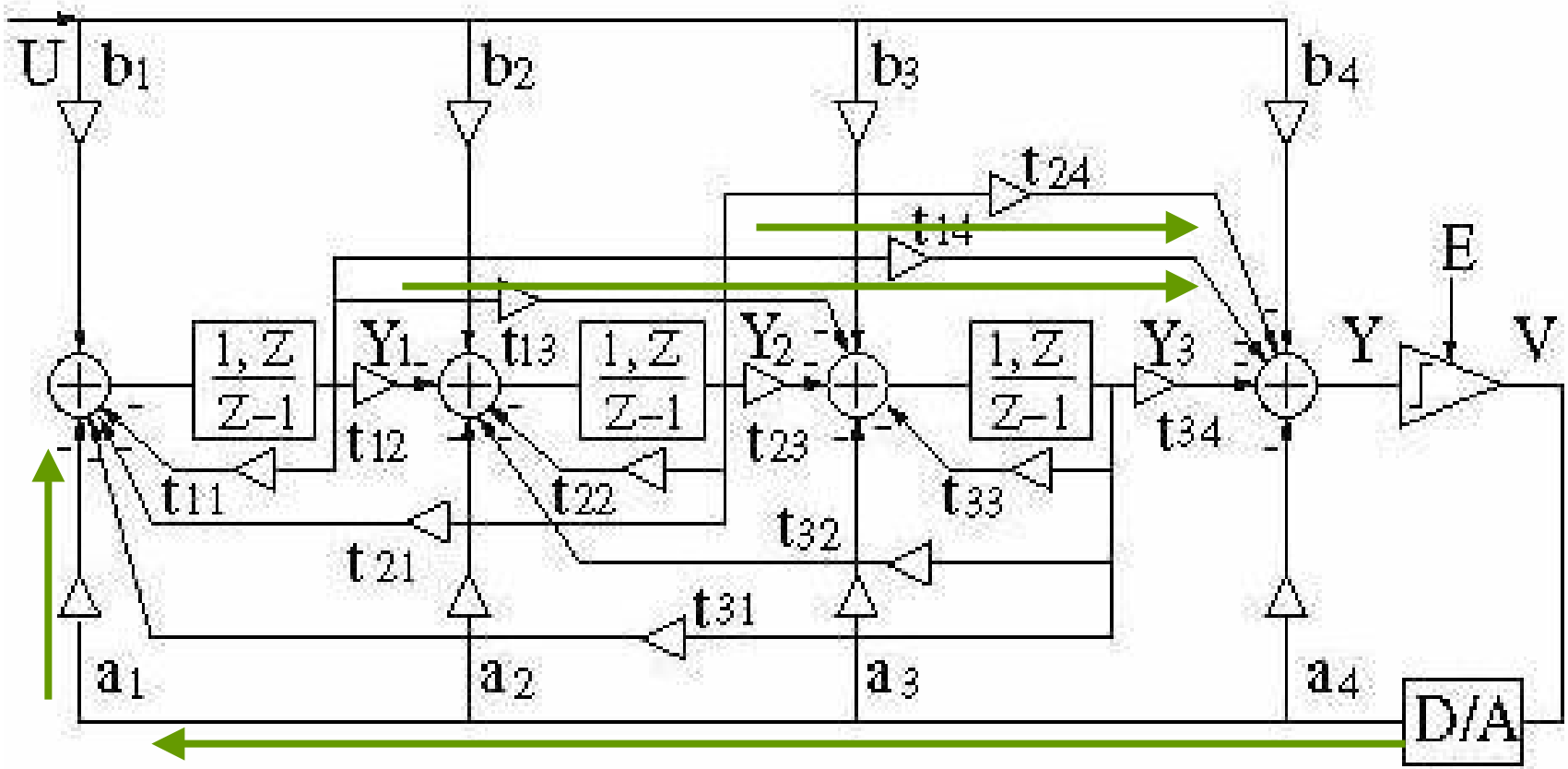
Generic topology for 3rd order modulator



Y_i : the output of the i^{th} integrator
Y : input to the quantizer
a_i : feedback coefficients from output to the i^{th} adder
b_i : feedforward coefficients from input to the i^{th} adder
t_{ji} : feedback and feedforward coefficients from Y_j to the i^{th} adder

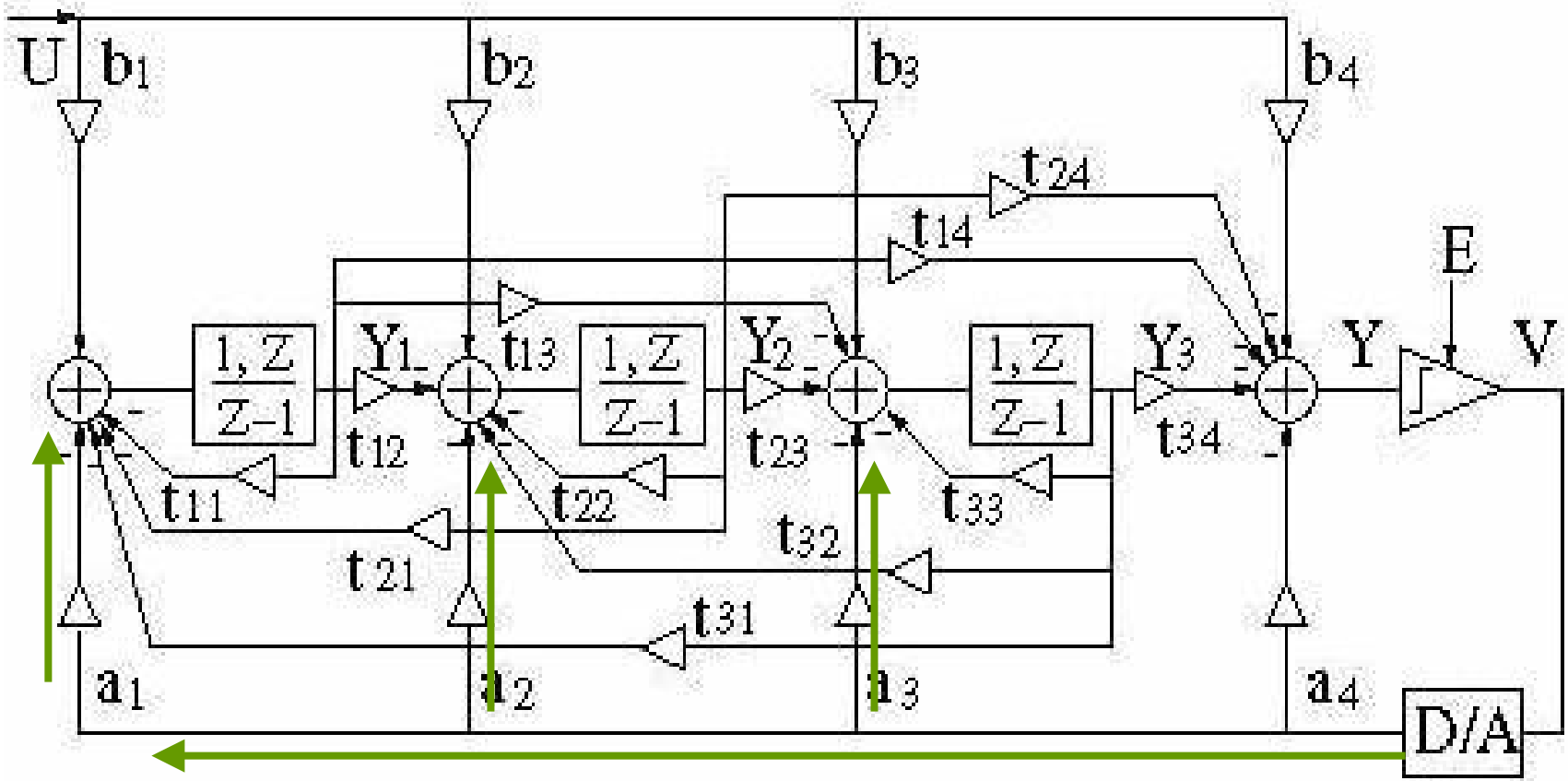
Generic topology for 3rd order modulator

Chain of Integrators with Feedforward Summation



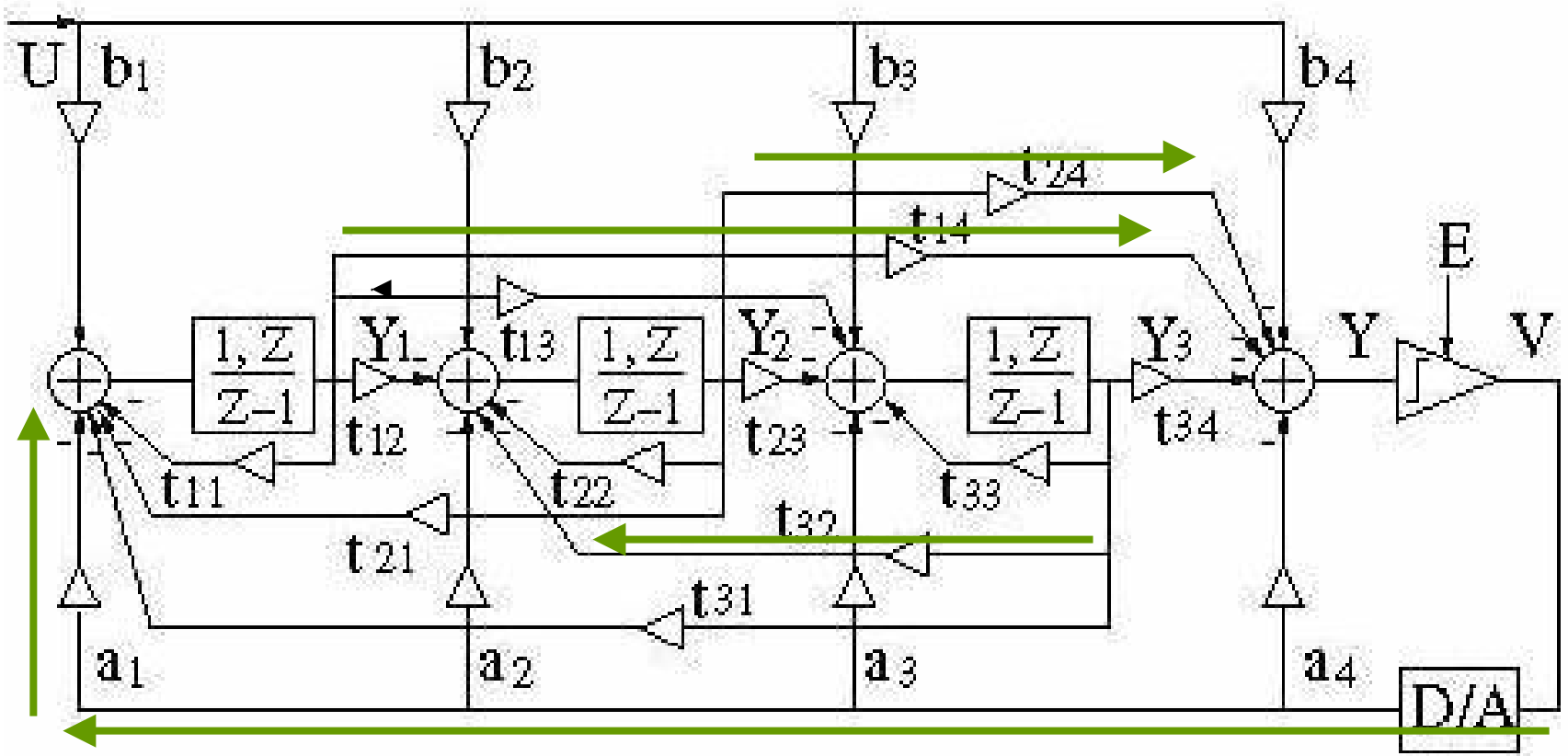
Generic topology for 3rd order modulator

Chain of Integrators with Distributed Feedback



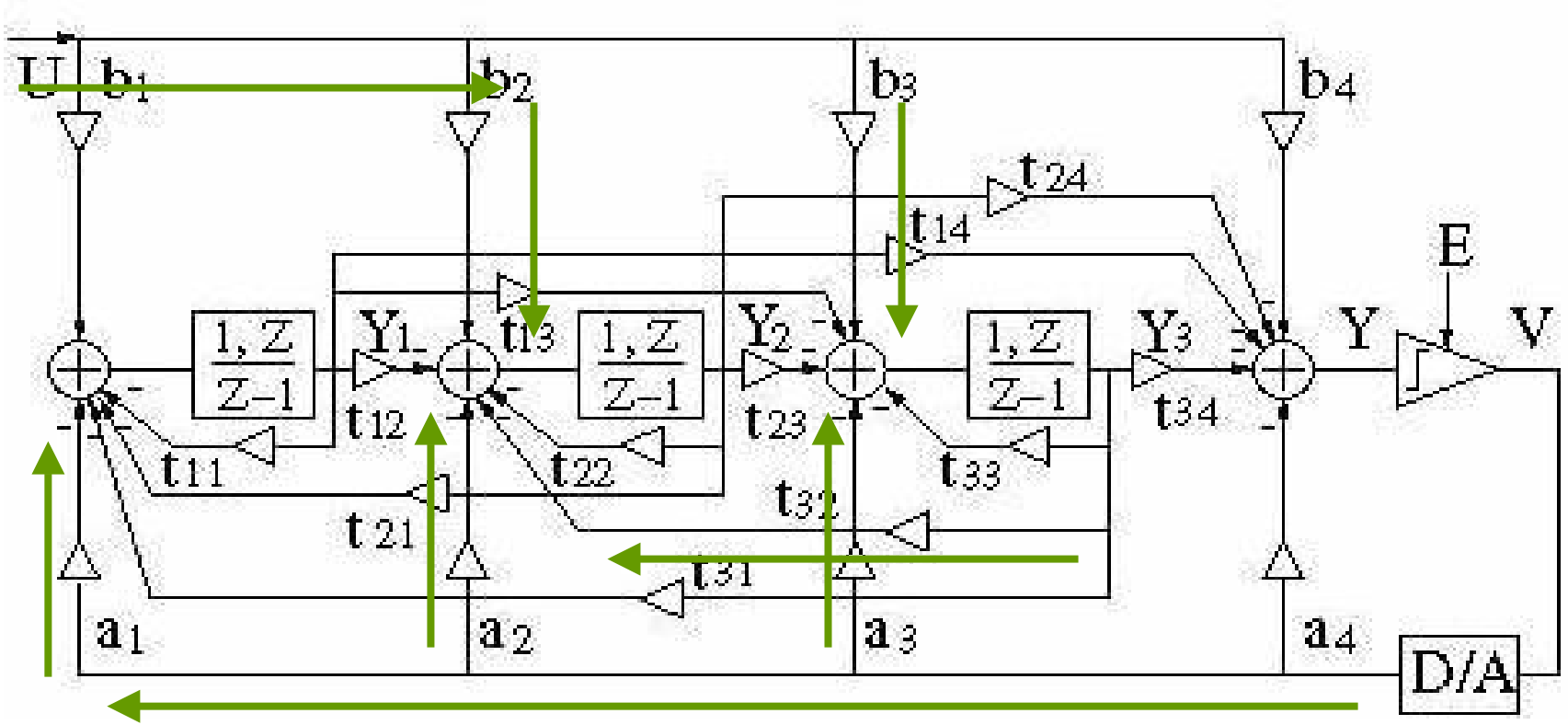
Generic topology for 3rd order modulator

Chain of Integrators with Feedforward Summation and Local Feedback



Generic topology for 3rd order modulator

**Chain of Integrators with Distributed Feedback,
Distributed Feedforward and
Local Feedback**



Generic topology

$$
\begin{aligned}
&t_{ji} \geq 0, \ \text{if} \ j \geq i, \ \ j = 1,\ldots,N, \ \ i = 1,\ldots,N+1 \\
&t_{ji} \leq 0, \ \text{if} \ j < i, \ \ j = 1,\ldots,N, \ \ i = 1,\ldots,N+1 \\
&a_i \geq 0, \ b_i \geq 0, \quad i = 1,\ldots,N+1 \qquad\qquad (1)
\end{aligned}
$$

$$
Y_1(z) = \frac{[b_1 \times u(z) - a_1 \times V(z) - t_{11} \times Y_1(z) - t_{21} \times Y_2(z) - t_{31} \times Y_3(z)]}{(z-1)}
$$

$$
Y_2(z) = \frac{[b_2 \times u(z) - a_2 \times V(z) - t_{12} \times Y_1(z) - t_{22} \times Y_2(z) - t_{32} \times Y_3(z)]}{(z-1)}
$$

$$
Y_3(z) = \frac{[b_3 \times u(z) - a_3 \times V(z) - t_{13} \times Y_1(z) - t_{23} \times Y_2(z) - t_{33} \times Y_3(z)]}{(z-1)}
$$

$$
V(z) = b_4 \times u(z) - a_4 \times V(z) - t_{14} \times Y_1(z) - t_{24} \times Y_2(z) - t_{34} \times Y_3(z) + E(z)
$$

Symbolic TF for generic topology

- **Solve the above equation using MATHEMATICA to obtain** $NTF = \frac{V(z)}{E(z)}$ **and** $STF = \frac{V(z)}{U(z)}$

- **Generalize the symbolic expressions for Delta-Sigma modulator of any order** N

- **For example, the numerator** NTF_n **and denominator of** NTF_d **of Delta-Sigma modulator of order** N **are:**

$$NTF_n = \sum_{K=0}^{N}(-1)^{K+1}(C_N^K - C_{N-1}^{K-1}\sum_{i=1}^{N} t_{ii} + \ldots$$

$$+ (-1)^K C_{N-K}^{K-K} \sum_{i_1\neq}\sum_{i_2\neq}\ldots\sum_{i_K} t_{i_1(i_1,i_2,\ldots,i_K)} t_{i_2(i_1,i_2,\ldots,i_K)} \ldots t_{i_K(i_1,i_2,\ldots,i_K)}) z^{N-K}$$

$$NTF_d =$$

$$\sum_{K=0}^{N}(-1)^{K+1}((C_N^K - C_{N-1}^{K-1}\sum_{i=1}^{N} t_{ii} + \ldots + (-1)^K C_{N-K}^{K-K} \sum_{i_1\neq}\sum_{i_2\neq}\ldots\sum_{i_K} t_{i_1(i_1,i_2,\ldots,i_K)} t_{i_2(i_1,i_2,\ldots,i_K)} \ldots t_{i_K(i_1,i_2,\ldots,i_K)}) + \ldots$$

$$+ (-1)^{K+1}(C_{N-1}^{K-1}\sum_{i=1}^{N} a_i t_{i,N+1} + C_{N-2}^{K-2}\sum_{i=1}^{N} a_i \sum_{j_1\neq}\sum_{j_2}^{N} t_{j_1(N+1,j_2)} t_{j_2(N+1,j_2)} + \ldots +$$

$$+ C_{N-K}^{K-K}\sum_{i=1}^{N} a_i \sum_{j_1\neq}\sum_{j_2\neq}\ldots\sum_{j_K} t_{j_1(j_1,j_2,\ldots,j_K)} t_{j_2(j_1,j_2,\ldots,j_K)} \ldots t_{j_K(j_1,j_2,\ldots,j_K)}) a_{N+1}(-1)^{K+1}(C_N^K - C_{N-1}^{K-1}\sum_{i=1}^{N} t_{ii} + \ldots$$

$$+ (-1)^K C_{N-K}^{K-K} \sum_{i_1\neq}\sum_{i_2\neq}\ldots\sum_{i_K} t_{i_1(i_1,i_2,\ldots,i_K)} t_{i_2(i_1,i_2,\ldots,i_K)} \ldots t_{i_K(i_1,i_2,\ldots,i_K)})) z^{N-K}$$

Symbolic NTF and STF

- **Complexity of growth of terms is roughly $4\times N$!**
- **Generally, modulator order is kept below 6~8, the symbolic expressions scale reasonably well**
- **MINLP is able to handle large number of constraints of different complexity**
- **Symbolic expressions for other combination of integrator types can be readily obtained via variable substitution**

MINLP problem formulation

- **By equating the symbolic TF to the desired TF, $3\times(N+1)$ equations are obtained with $(N+1)\times(N+2)$ unknowns**
- **Properties for the symbolic TF:**
  - All terms are nonlinear expressions of the defined coefficient variables
  - No quadratic terms
- **This mild nonlinear formulation is suitable to be solved by NLP**
- **To select the signal paths, binary variables are defined, so MINLP**

MINLP formulation

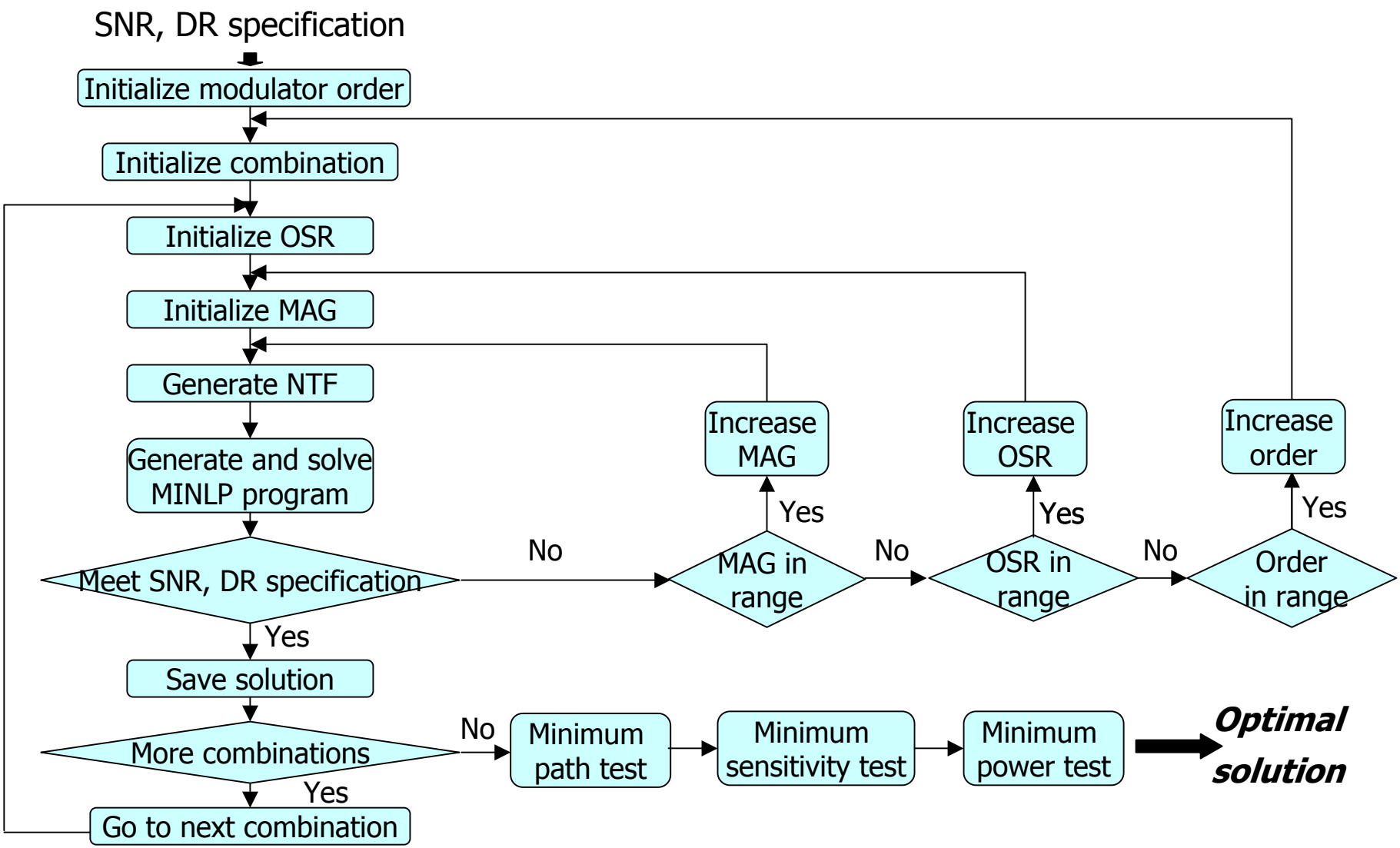
$$\text{minimize } f(x_i, wx_i)$$
$$subject\ \ to:\ \ g(x_i) = 0;$$
$$subject\ \ to:\ \ h(x_i, wx_i) \le 0;$$
$$subject\ \ to:\ \ x_i\ satisfy\ \ (1),\ \ wx_i \in \{0,1\};$$

Linear constraints *h* are added considering the complexity of nonlinear product term

Instead, we formulate *h* as: $x_i \times wx_i$

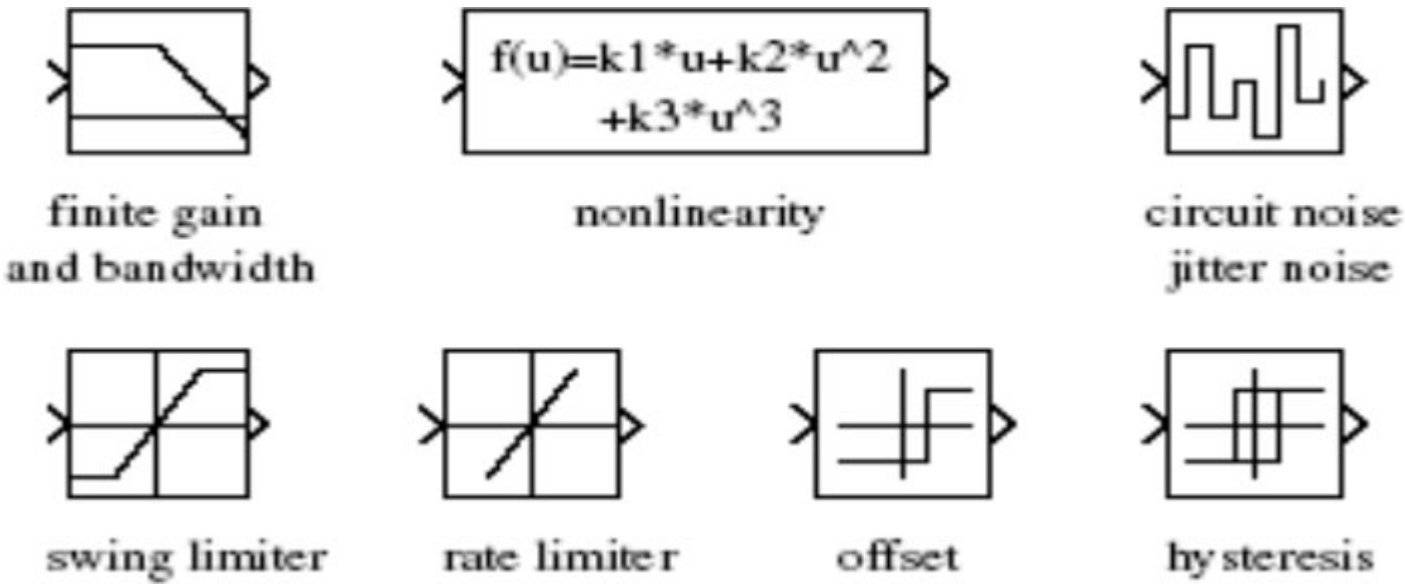
$wx_i = 1$ if $x_i \ge \varepsilon$ and $wx_i = 0$ otherwise, where ε is very small

Topology exploration flow



Topology refinement

- **Scaling => the voltage swings at the output of each integrator are within a certain range**
- **Nonideal blocks in Simulink**



Experiment: 3rd order modulator

- **3rd order Delta-Sigma modulator**
- **DR>70db**
- $N = 3,\ P = 1.5,\ U_{\max} = V_{ref}$,

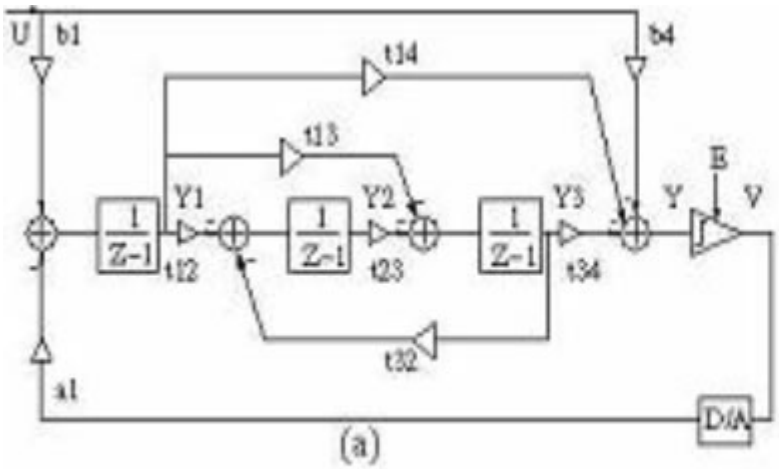
  $OSR = 32,\ MAG = 1.5$

$$NTF_1 = \frac{(z-1)(z^2 - 1.994z + 1)}{(z - 0.6685)(z^2 - 1.529z + 0.6629)}$$

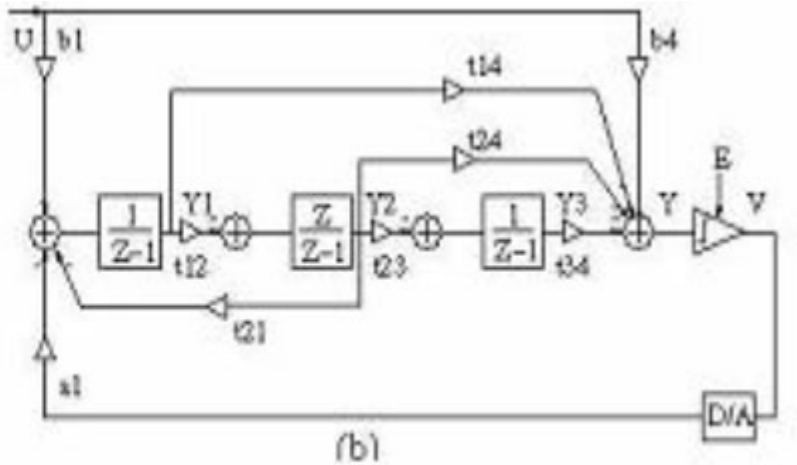
- **The topology is able to achieve DR=72db and SNR=67db**

Optimal topology

A. Minimum signal path (topology not unique)



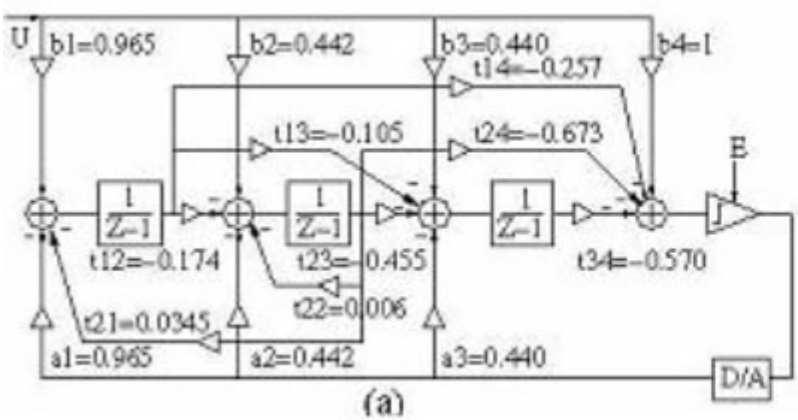
9 signal paths

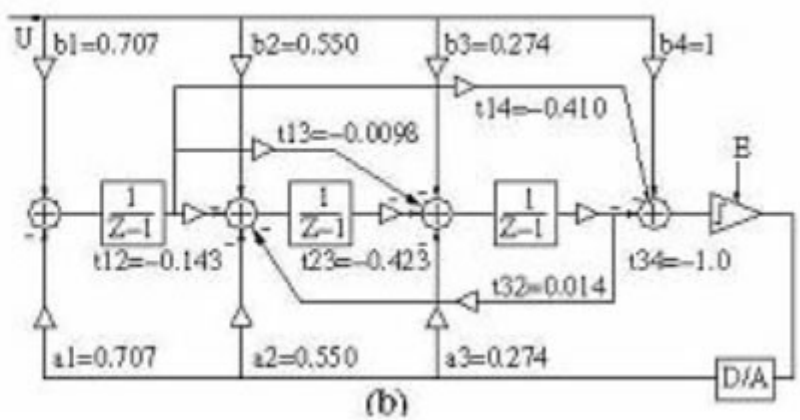


9 signal paths

Optimal topology

B. Minimum sensitivity

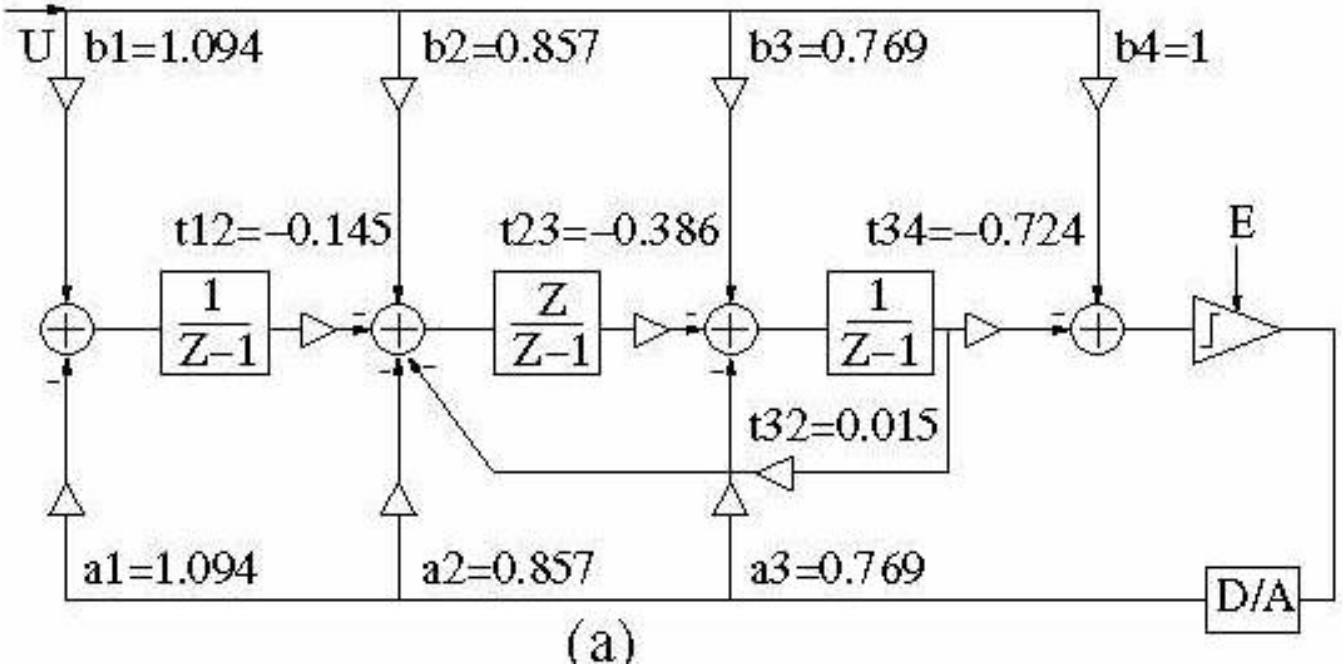




Sensitivity cost function values are 1.723 and 2.250 respectively, with all $S_{x_i}^{P_j}, S_{x_i}^{q_j} \leq 1.0$ (good case)

L. Huelsman, "Active and Passive Analog Filter Design", McGraw Hill, 1993

Topology from Toolbox



Sensitivity cost function values is 4.454, with some terms larger than 1.0, e.g.

$$S_{a_3}^{q_3}, S_{t_{34}}^{q_3} \geq 1.0$$

R. Schreier, “The Delta-Sigma Toolbox 6.0”, www.mathworks.com/matlabcentral/fileexchange, Nov 2003.

Triple-mode continuous-time ΔΣ modulator

Design Specifications

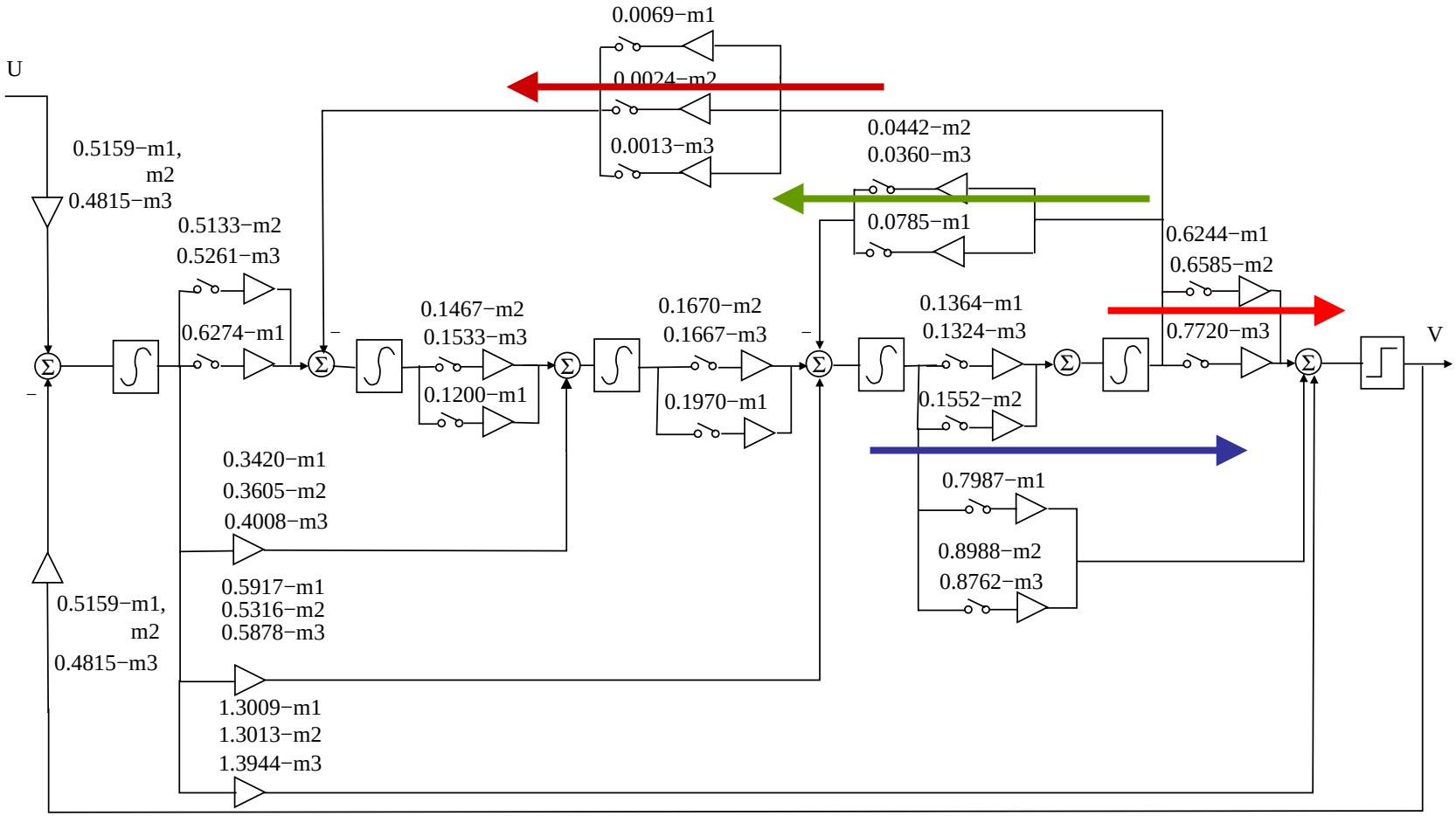
Mode	DR (bits/dB)	Bandwidth
UMTS	11.5/70	1.92MHz
CDMA2000	13/80	615kHz
GSM	15/90	190kHz
EDGE	14.5/87	270kHz

Design parameters for possible candidates

Order	OSR		
	UMTS	CDMA2000	GSM-EDGE
2	96	128	--
3	48	64	96
4	40	48	64
5	28, 32	40	48

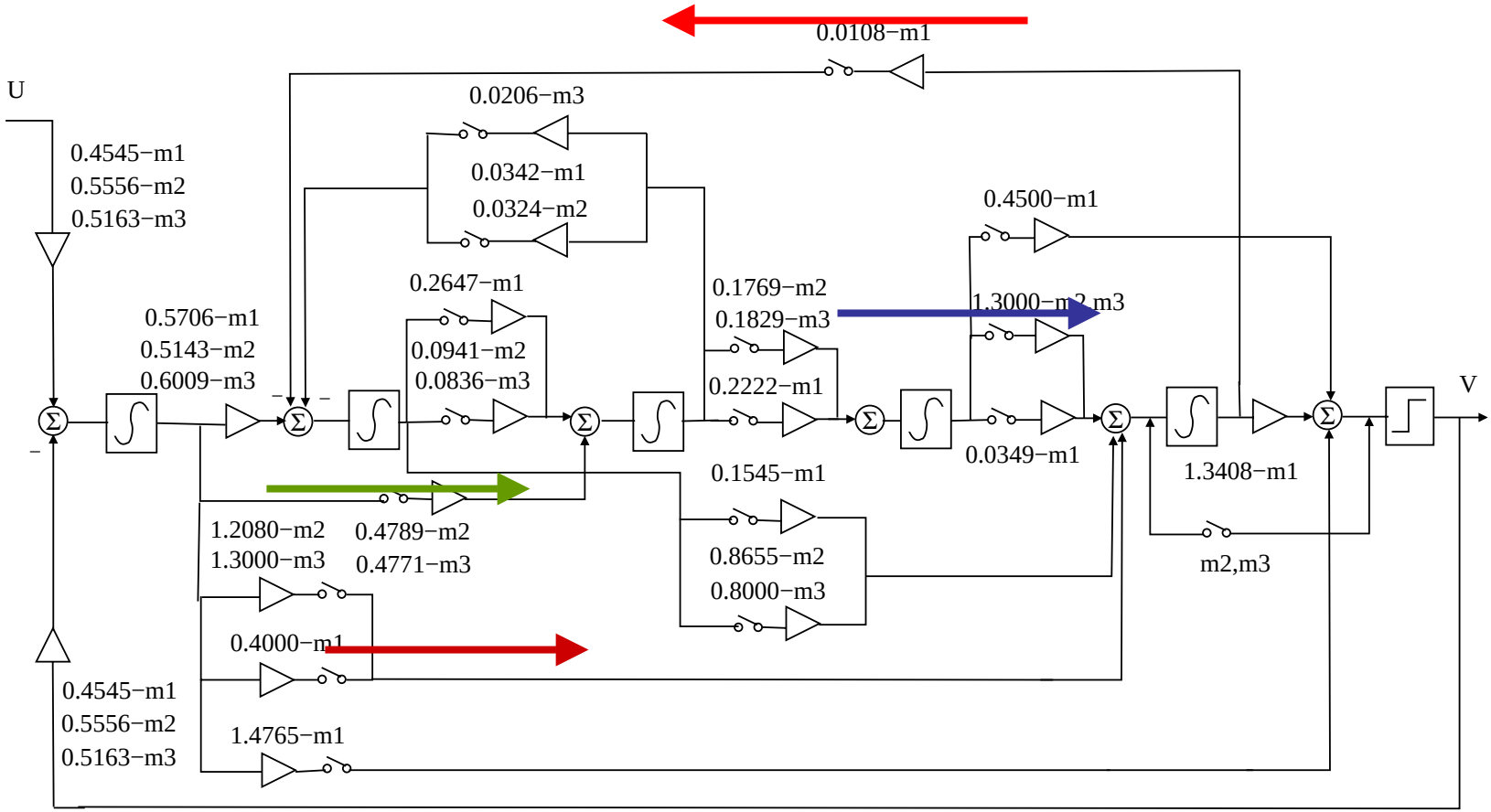
[1] R. Veldhoven, "A Triple-Mode Continuous-Time ΔΣ Modulator With Switched-Capacitor Feedback DAC for a GSM/EDGE/CDMA2000/UMTS Receiver", *JSSC*, Dec 2003.

Reconfigurable ΔΣ modulator topologies (1)



Topology *opt1*

Generated topologies



Topology *opt2*

Design complexity

complexity	3 single modes	[1]	*opt1* (5-5-5)	*opt2* (5-4-4)	*opt3* (5-4-3)
N_p	39	17	22	20	21
$N_{p,r}$	–	6	10	11	14
$N_{c,r}$	–	11	12	9	7
$N_{c,r2}$	–	0	9	6	4
$N_{c,r3}$	–	11	3	3	3
$N_{p,a}$	39	39	39	33	31
η_d	–	28.2%	24.4%	33.3%	33.3%
η_p	–	0%	0%	15.4%	20.5%

Np : # of signal paths

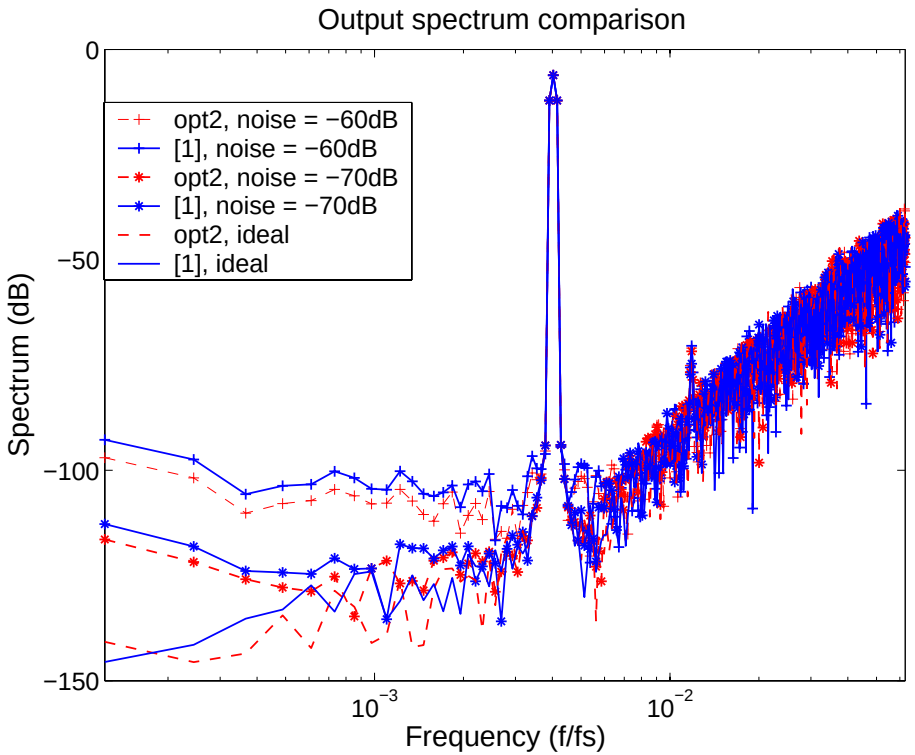
Np,r : # of non-reconfigurable cells

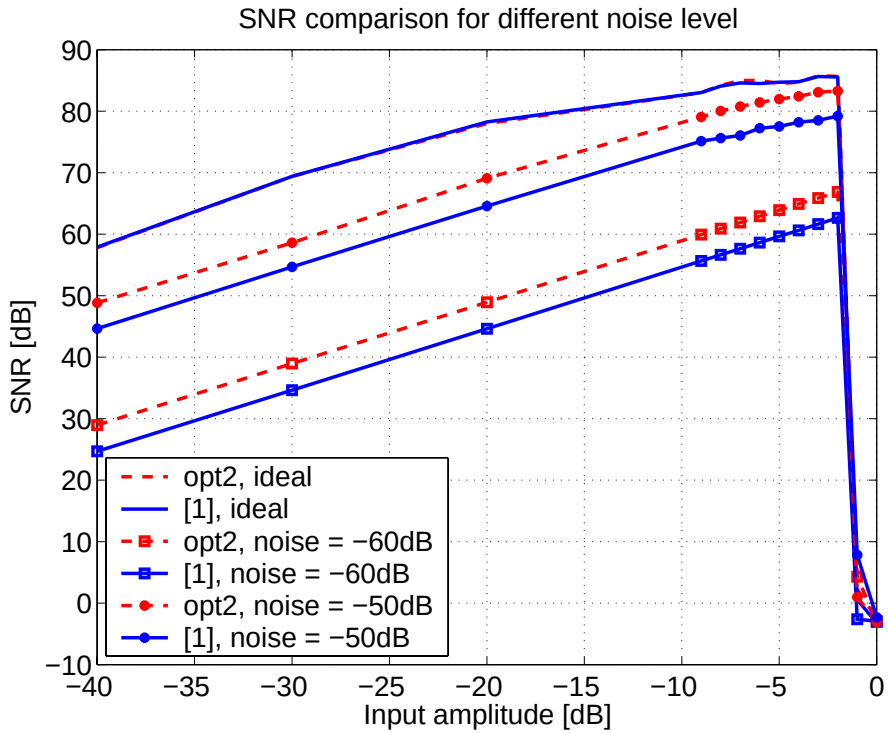
Nc,r : # of reconfigurable cells

ηd : estimated design effort

ηp : estimated power consumption reduction

SNR degradation due to circuit noise





Improvement as compared to the state-of-art design:

3dB for the case of -60dB noise level

5dB for the case of -50dB noise level

Experiments

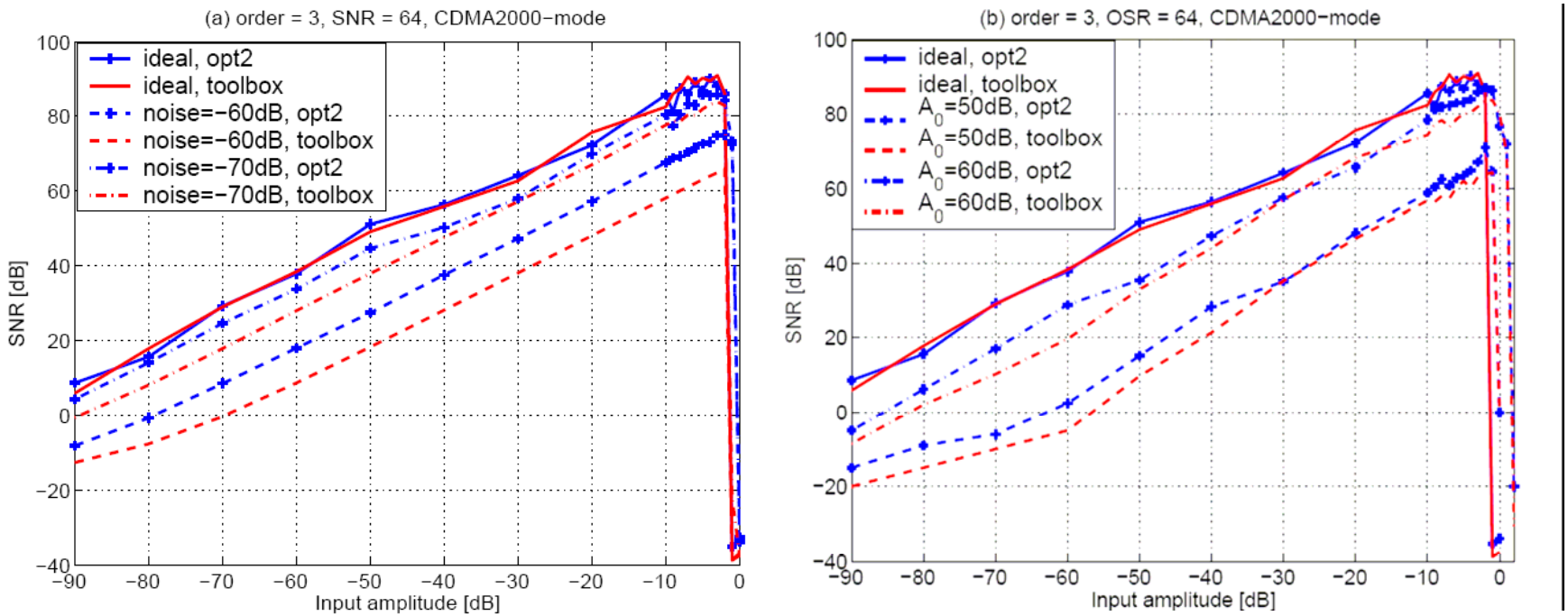


Fig. 3. SNR degradation by circuit nonidealities for topology *opt2* (mode 2)

Experiments

- Compare the triple-mode modulator with three single-mode modulators obtained with $\Delta\Sigma$ toolbox
  - **Design effort** can be less than 1/3
  - **Complexity** can be as less as 40%
  - **Power saving** can be as large as 24.2%
  - **More robust** to circuit nonidealities

Experiments using PSoC

- **Implementation of a reconfigurable Delta-Sigma modulator using PSoC mixed-signal SoC**

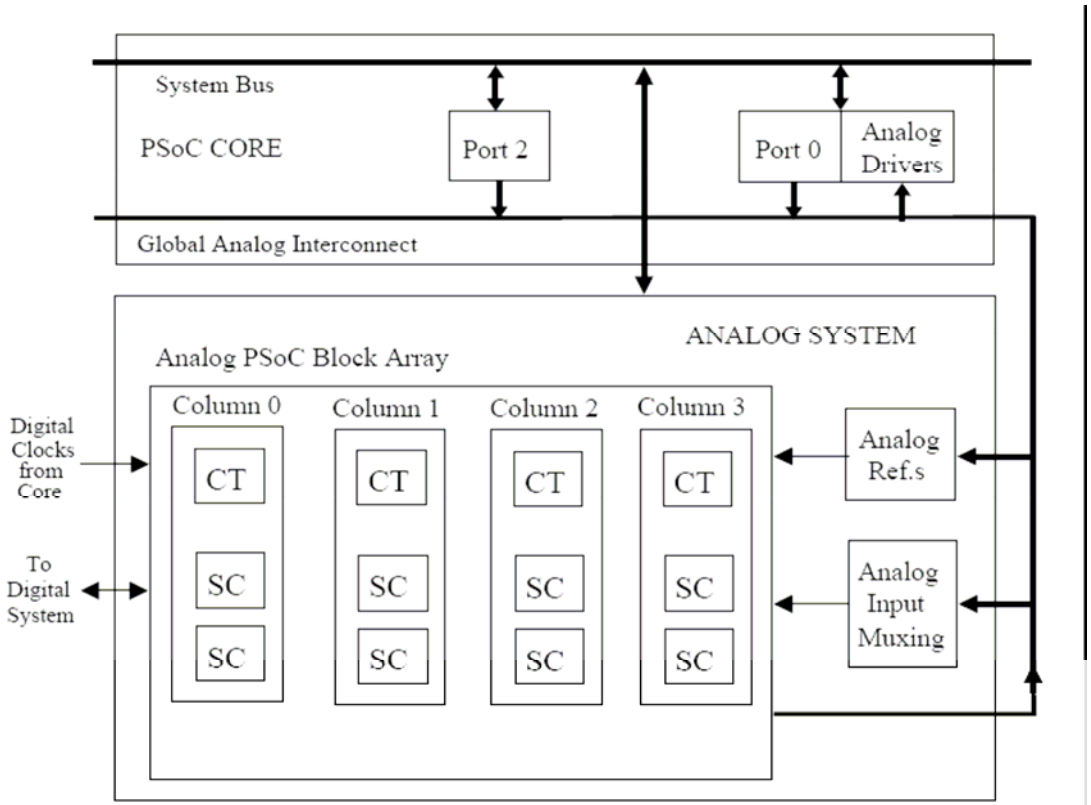


Fig. 4. PSoC analog system [11]

Experiments using PSoC

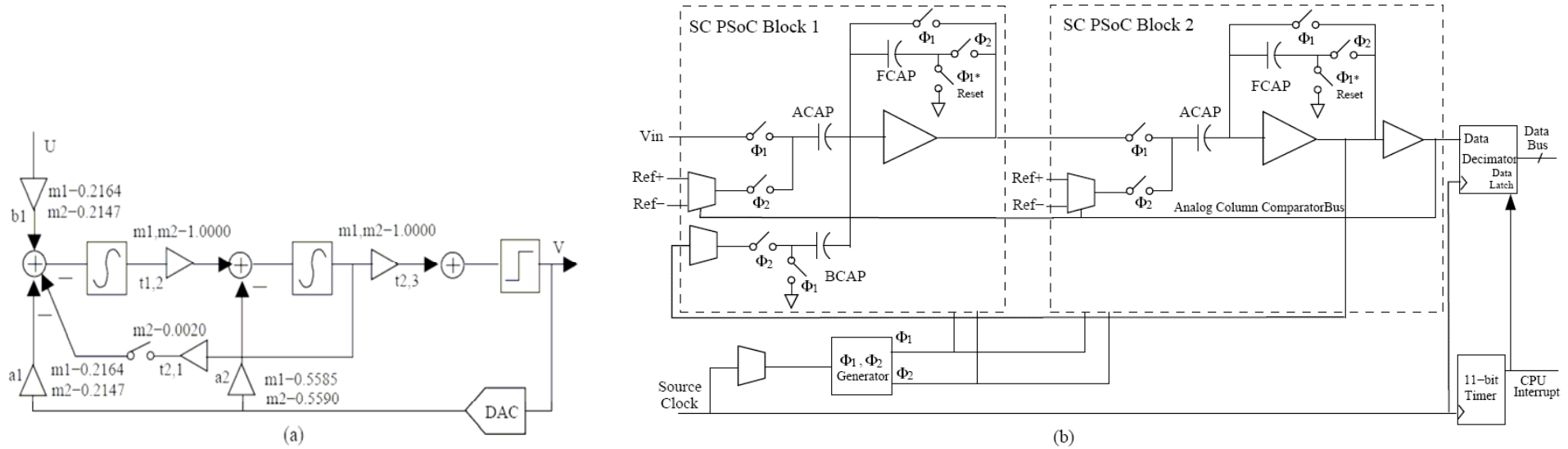


Fig. 5. Dual-mode second-order modulator (a) topology (b) PSoC implementation

Mode	SC block 1			SC block 2		
	ACAP	BCAP	FCAP	ACAP	BCAP	FCAP
1	4C	–	16C	8C	–	16C
2	8C	1C	32C	16C	–	32C

TABLE II

VALUES FOR THE CAPACITOR ARRAYS

Experiments using PSoC

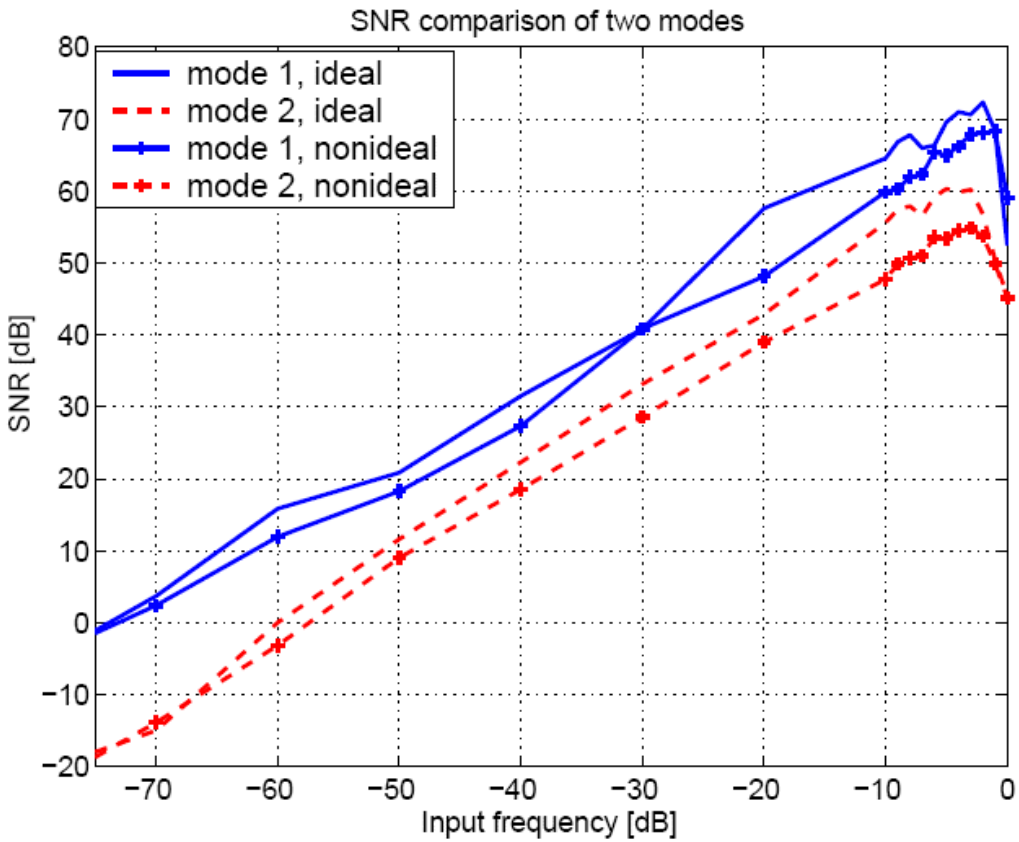


Fig. 6. SNR comparison of the dual-mode second-order modulator

Experiments using PSoC

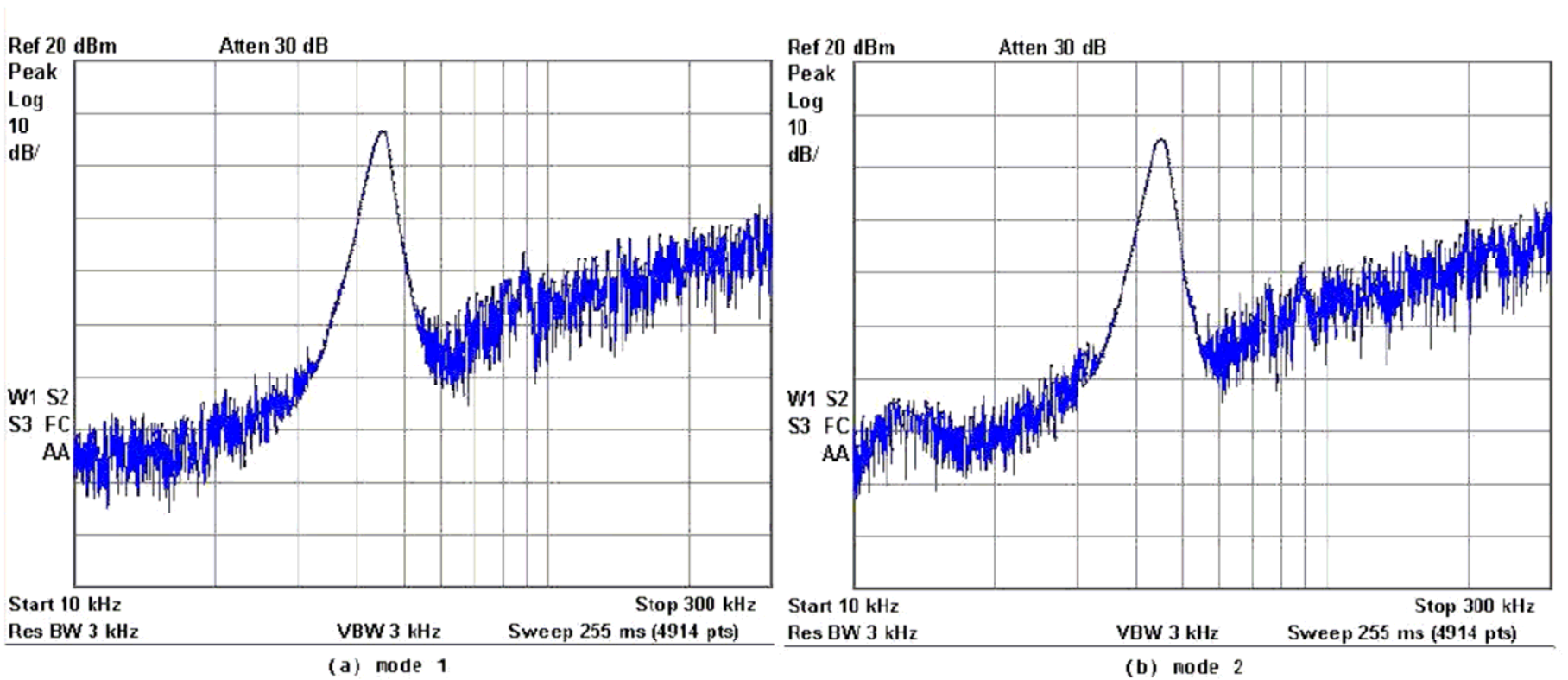


Fig. 7. Measurement result

Education & Training

- Hugo De Man, "System-on-Chip Design: Impact on Education and Research", IEEE Design & Test of Computers, July-Sept. 1999.

- System architects/designers:
  - Cross-disciplinary background: EE/CE/CS
  - EE: signals, conversion techniques, impact of circuit nonidealities, and know how to tackle these
  - CE: how HW & SW work together, abstraction levels, successive refinement, trade-off analysis
  - CS: high-level description languages for systems, system and circuit modeling techniques, formal verification

Education & Training

Curricula, textbooks, projects, lab material, exercises?

A. Doboli and E. Currie

"Embedded Mixed-Signal Systems: A Designer's Perspective", due to be published in 2007.

Conclusions

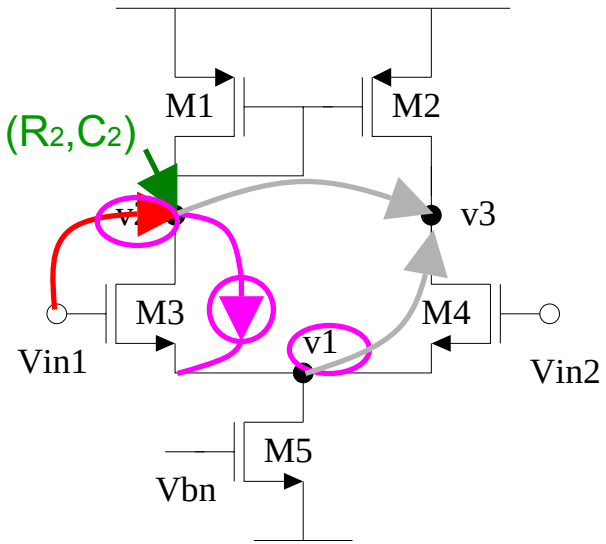
- PSoC: embedded mixed-signal architecture
- Related research at Stony Brook
- Systematic methodology for $\Delta\Sigma$ ADC design
- Automated circuit modeling
- Education & training

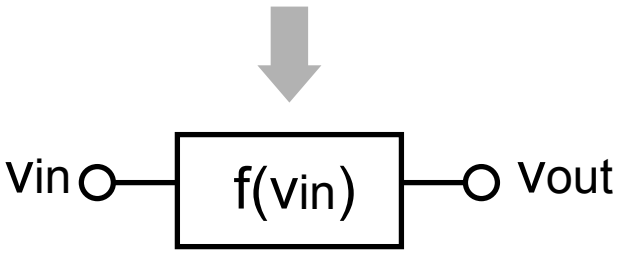
Automated Macromodeling

- **Produced macromodels:**
  - **Structural**
  - **No feedback dependencies (decoupled)**
  - **Symbolically characterized nonlinear current sources**
  - **Extensible, accuracy is controllable**
  - **Insight into circuit**
  - **Reusable**

Automated Macromodeling

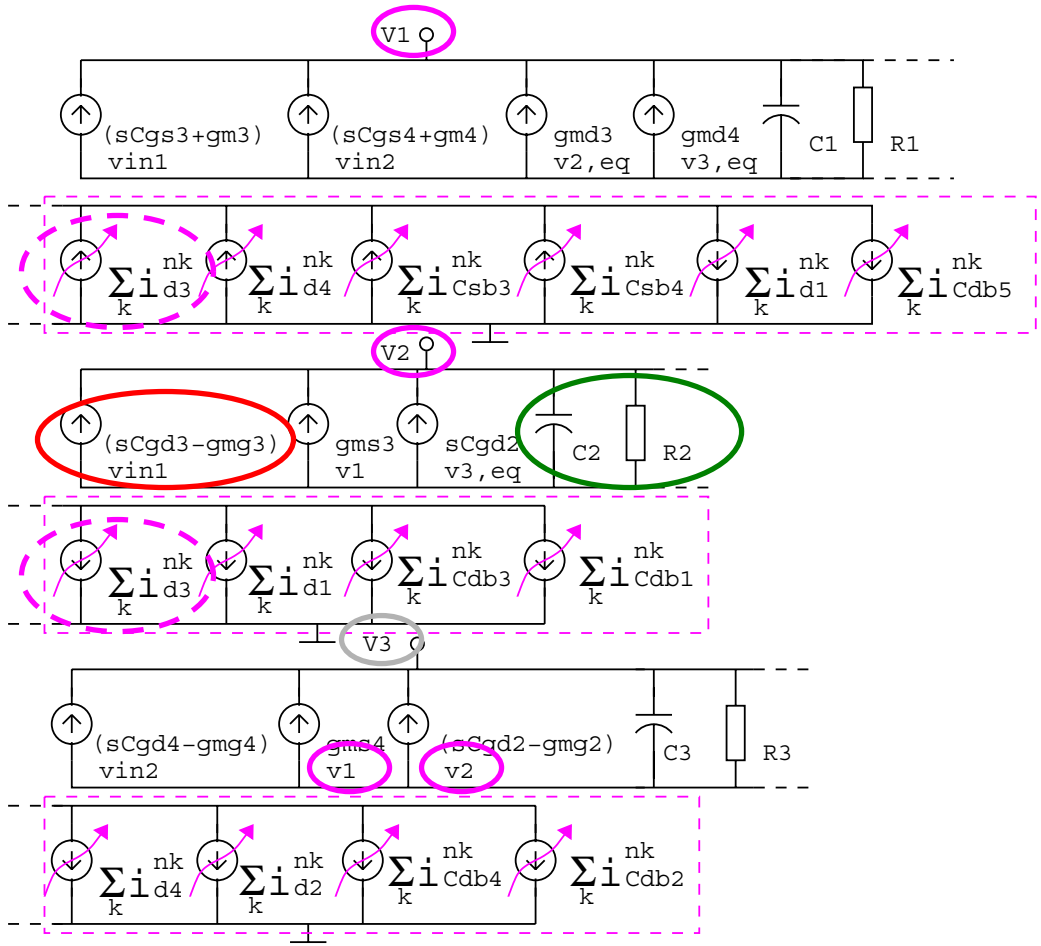
Circuit netlist





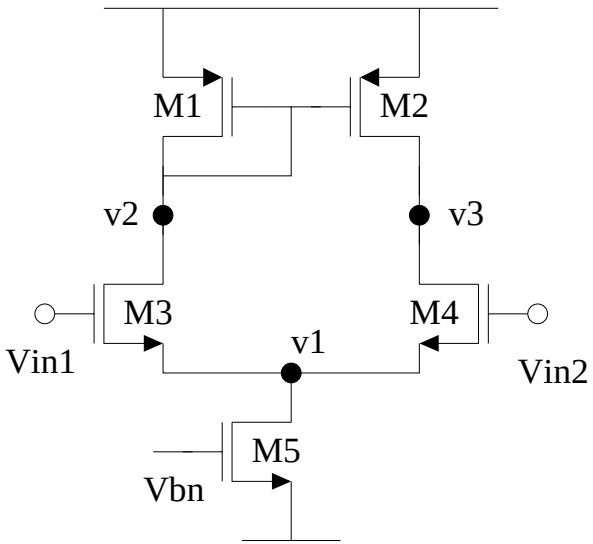
Black-box macromodel

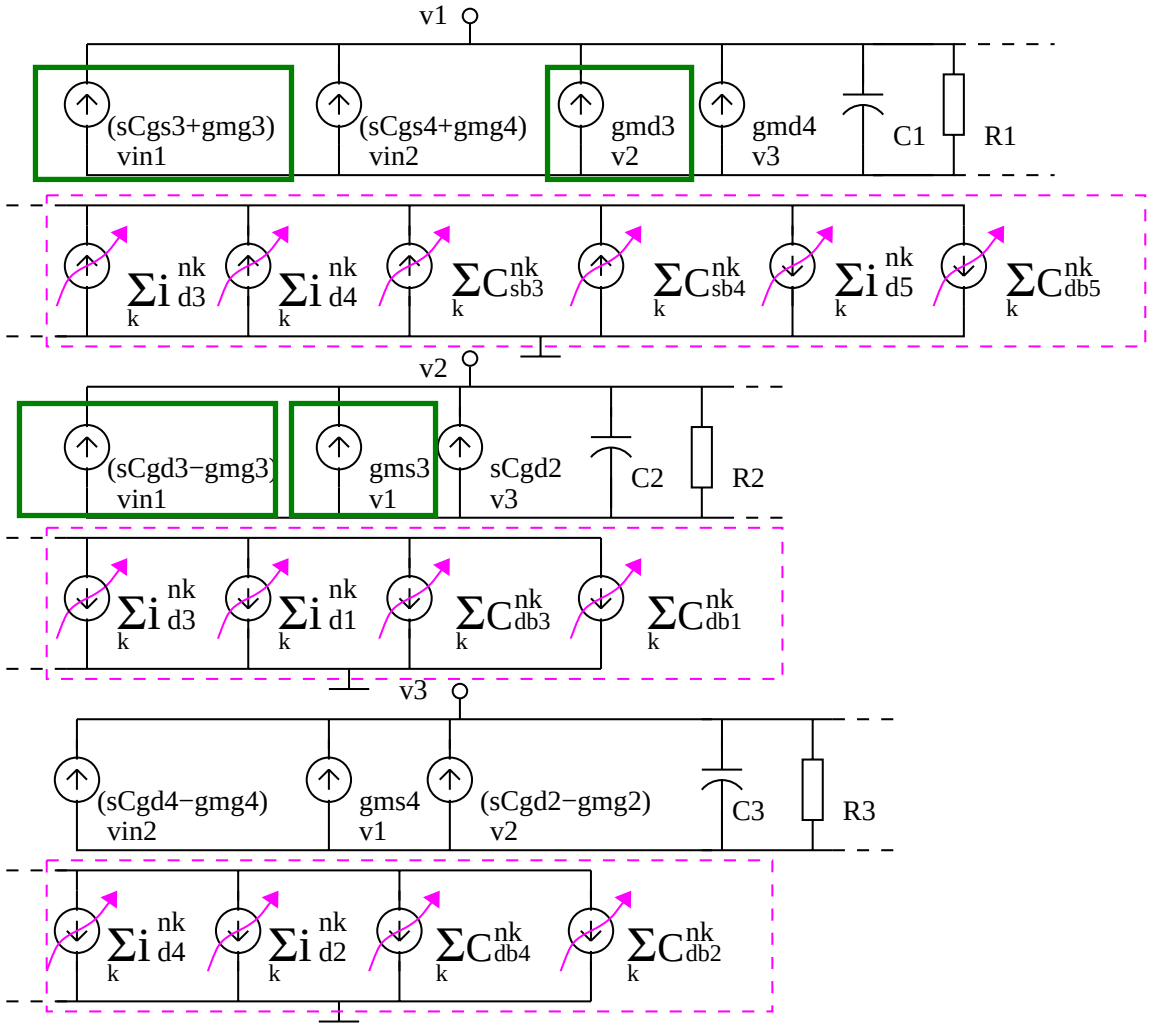
Structural nonlinear macromodel



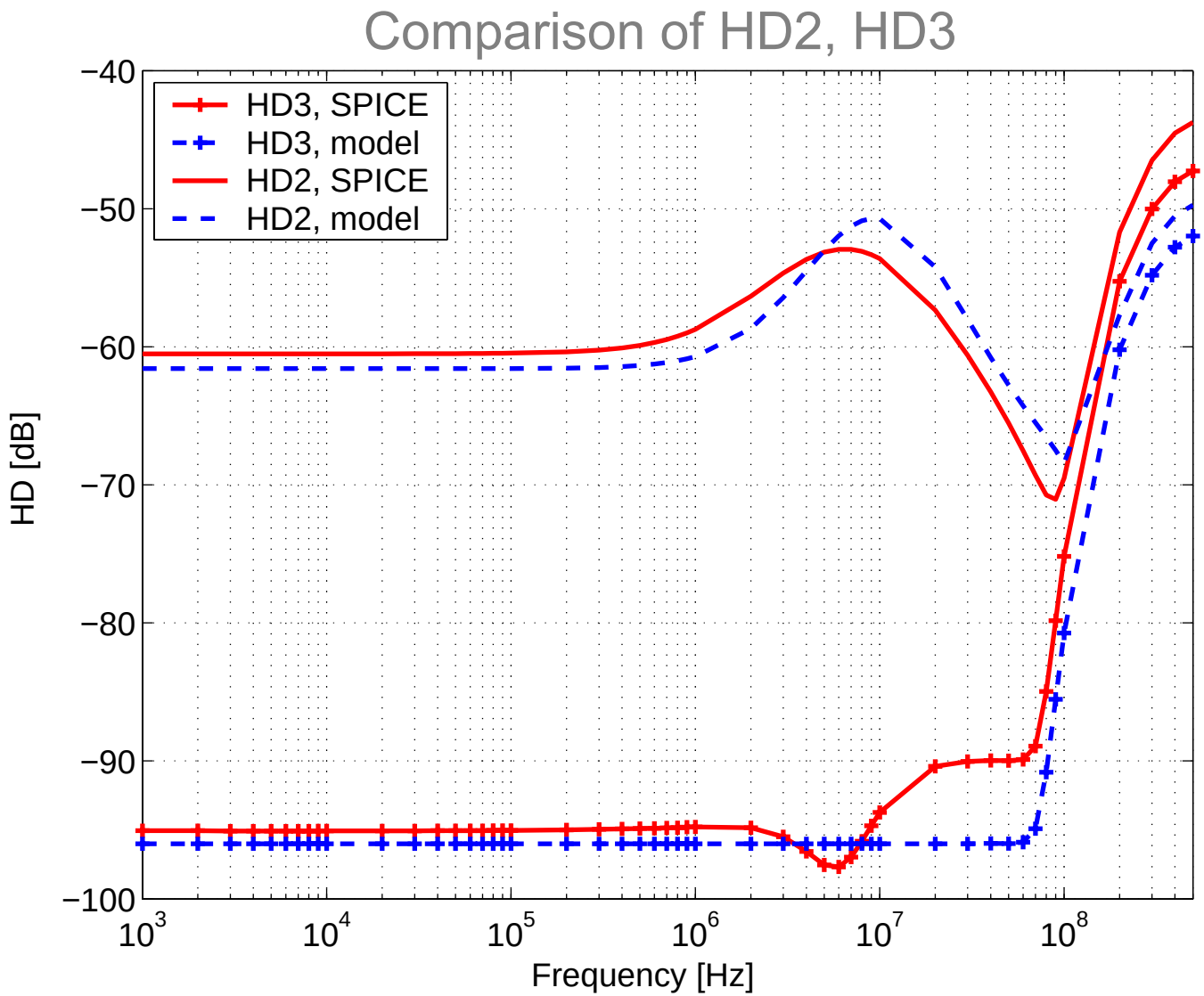
Automated Macromodeling

Circuit netlist

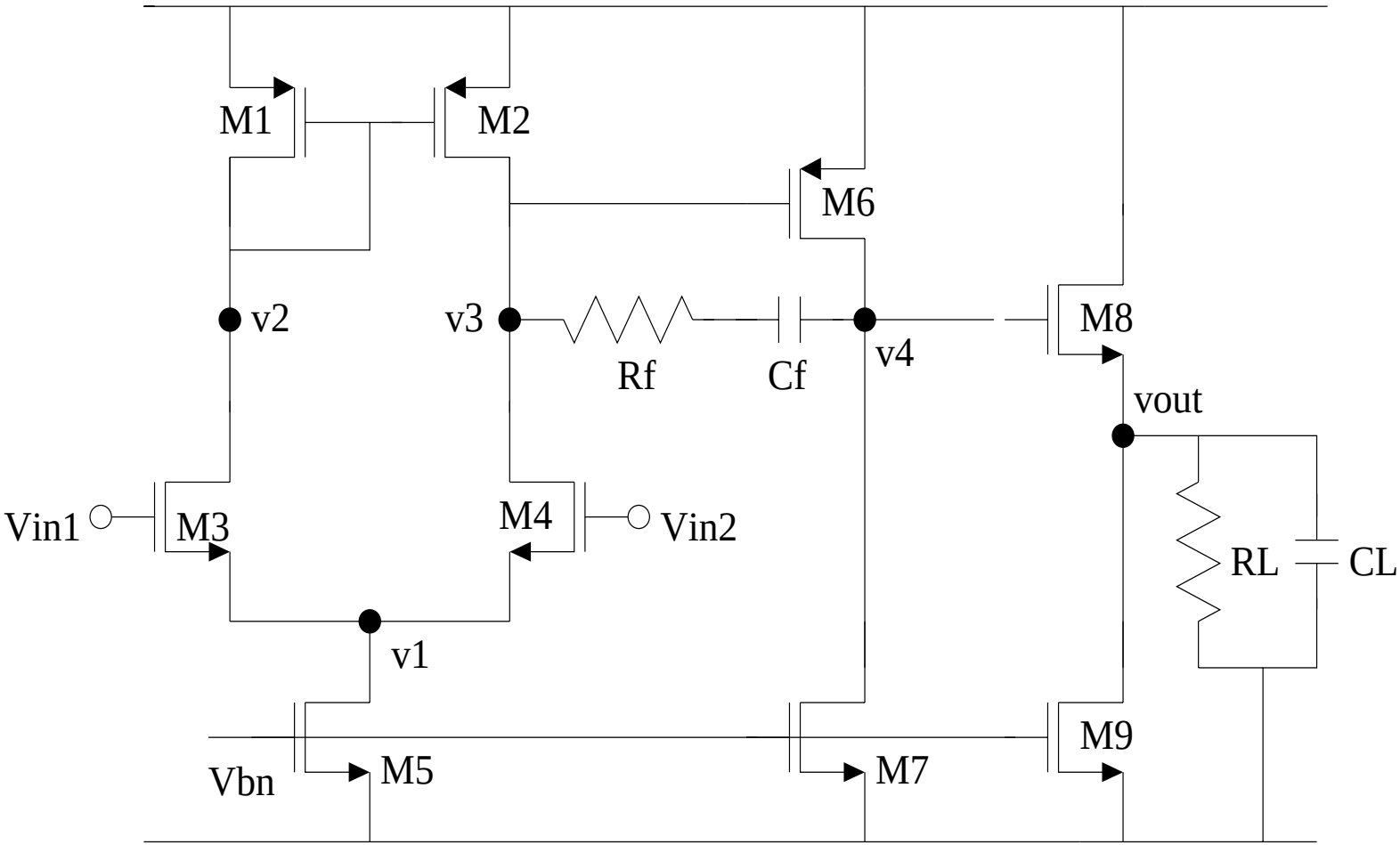




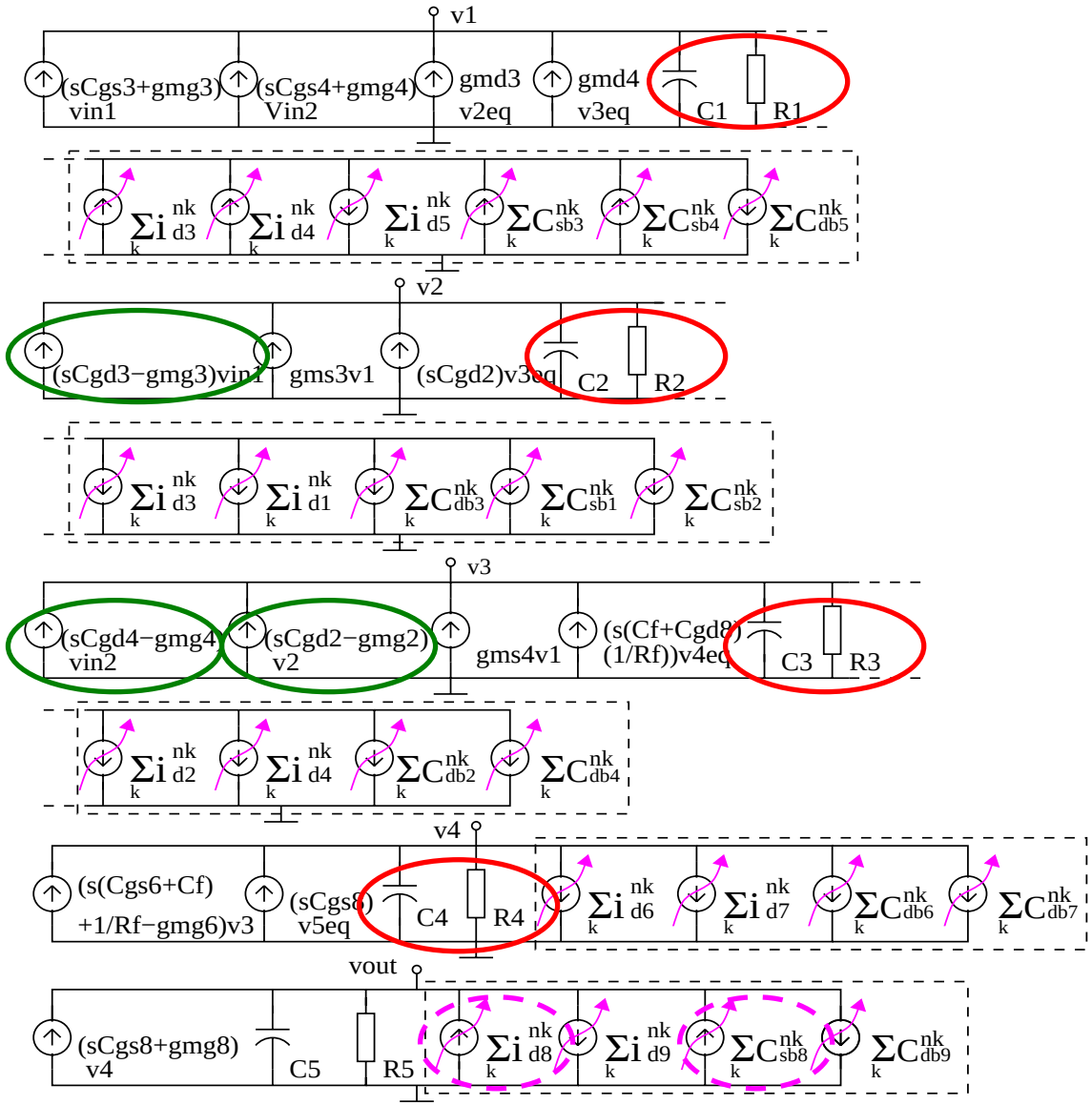
Automated Macromodeling



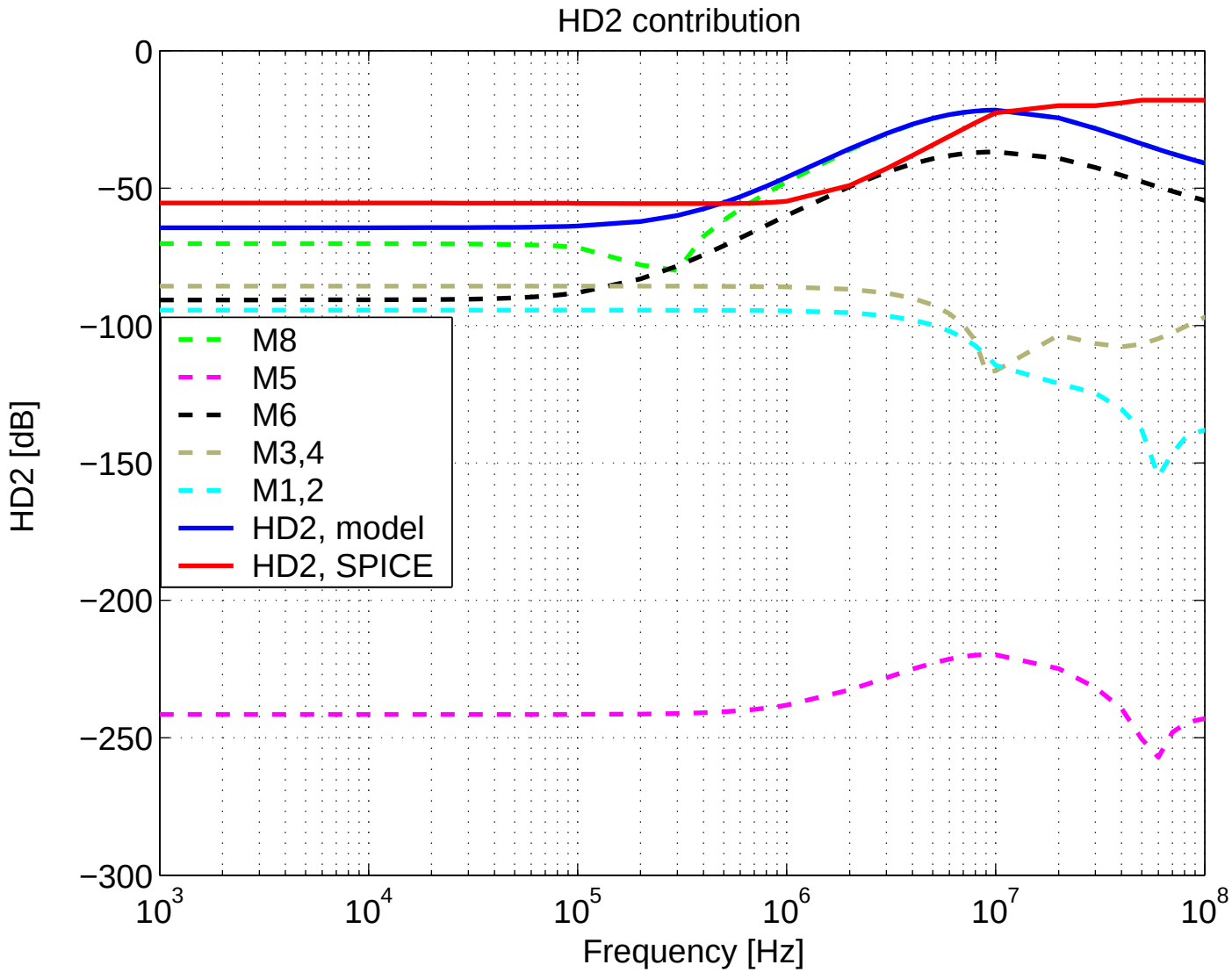
Automated Macromodeling



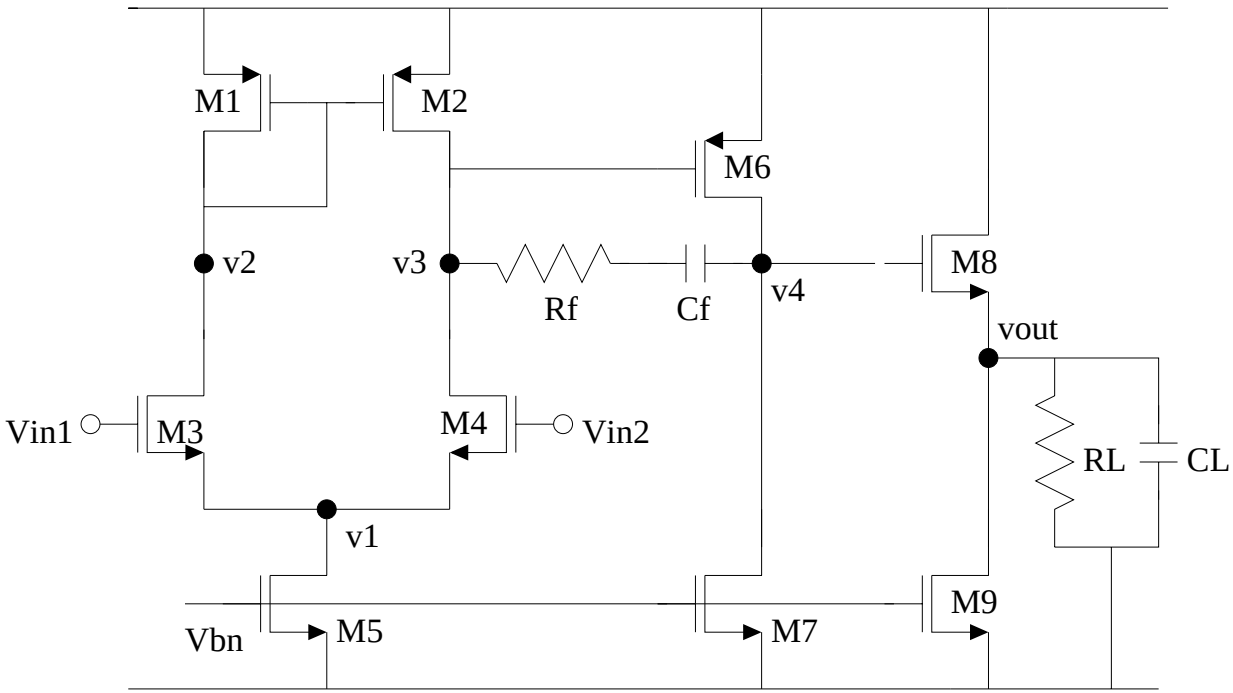
Automated Macromodeling



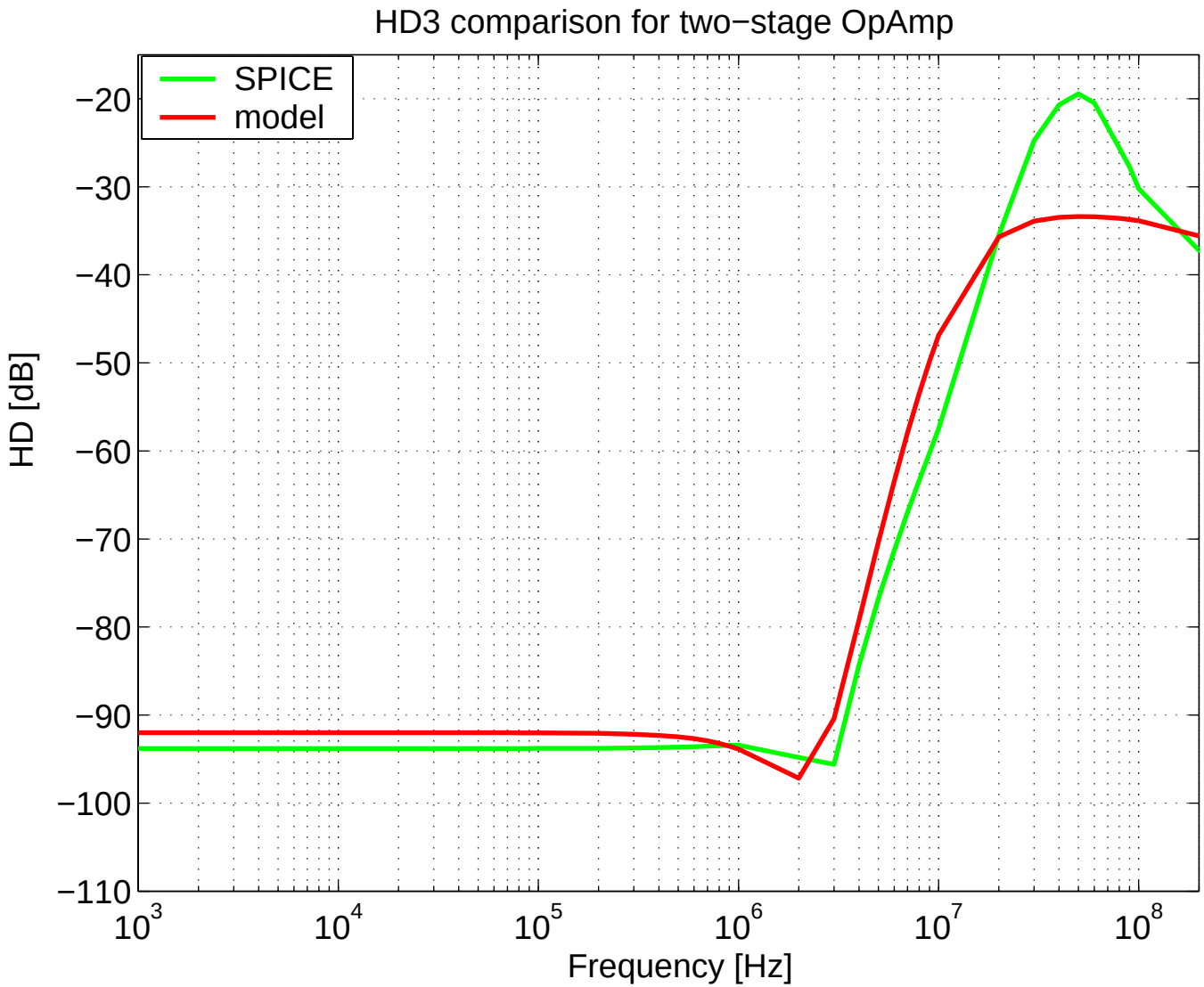
Automated Macromodeling



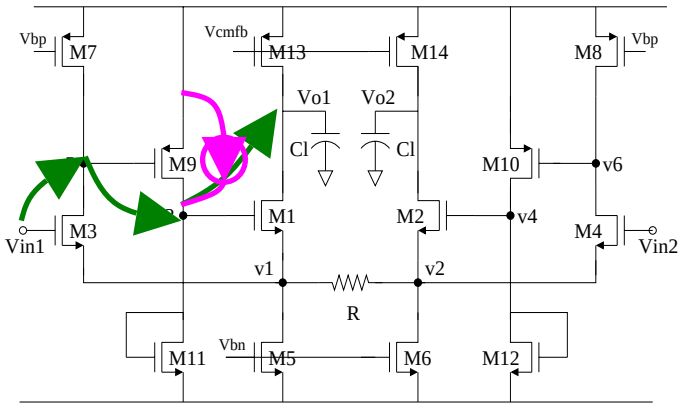
Automated Macromodeling

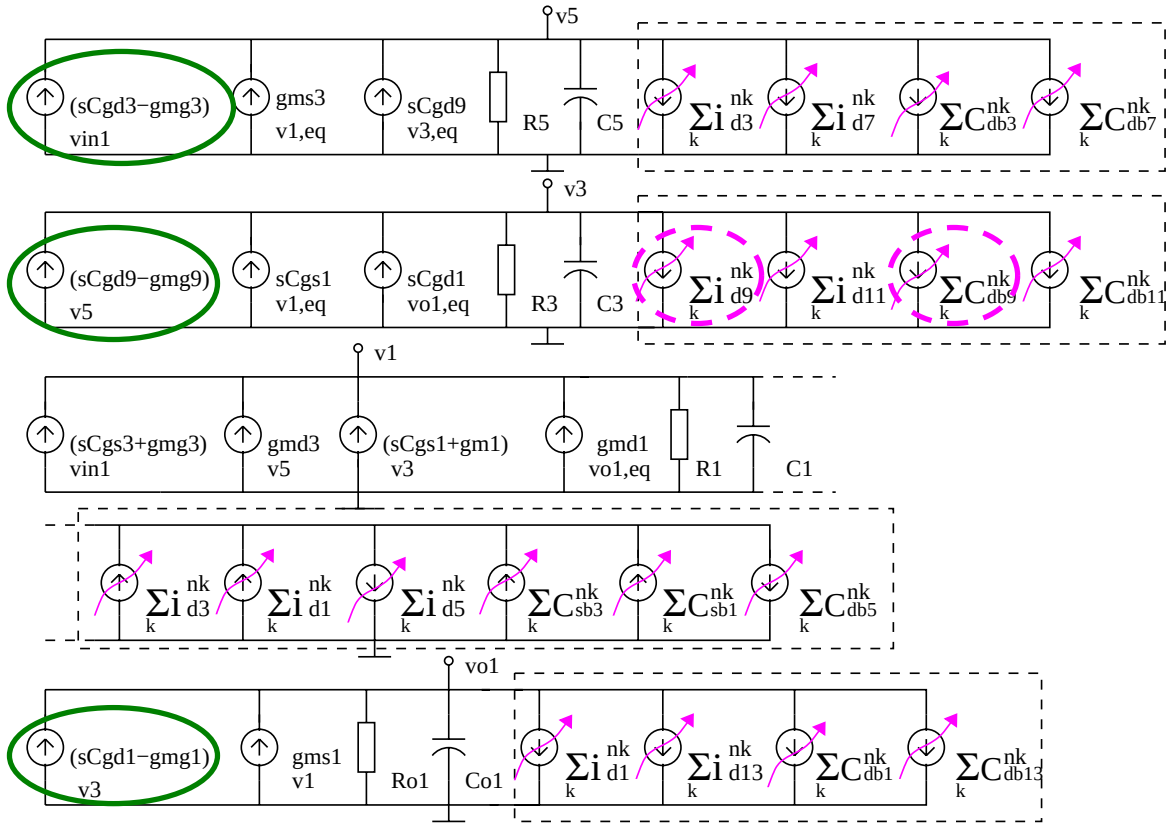


Automated Macromodeling

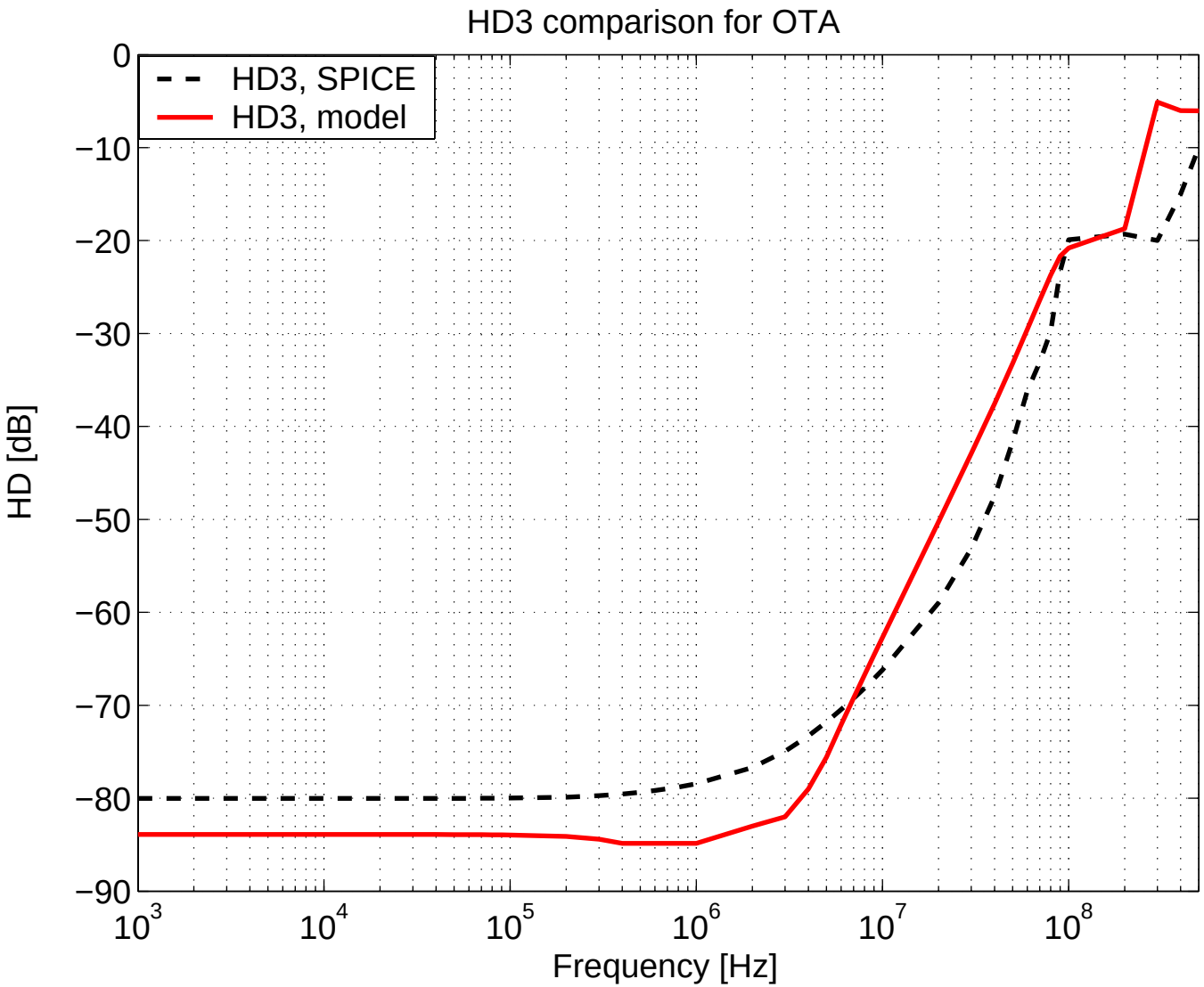


Automated Macromodeling





Automated Macromodeling



Automated Macromodeling