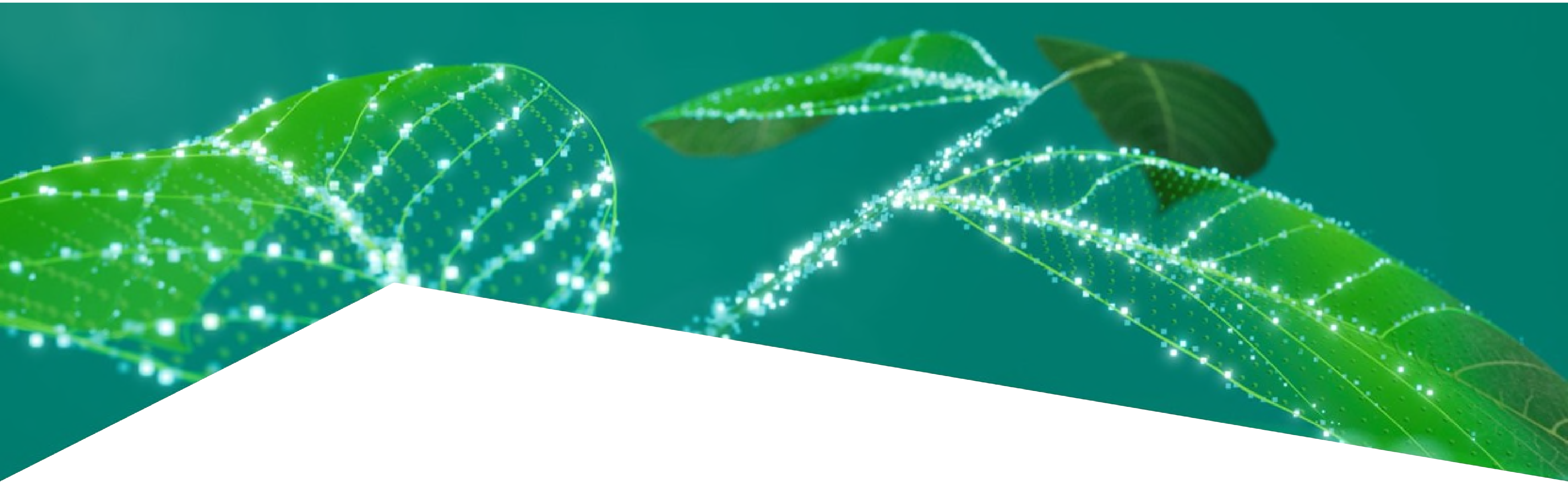

Exploring the benefits of the HSC topology in high performance AI power systems

C. R. Swartz; Senior Member IEEE, Lead Principal Engineer – Infineon Technologies
IEEE PELS Symposium 2025 Long Island, NY November 7th 2025

Infineon Technologies
November 7th 2025

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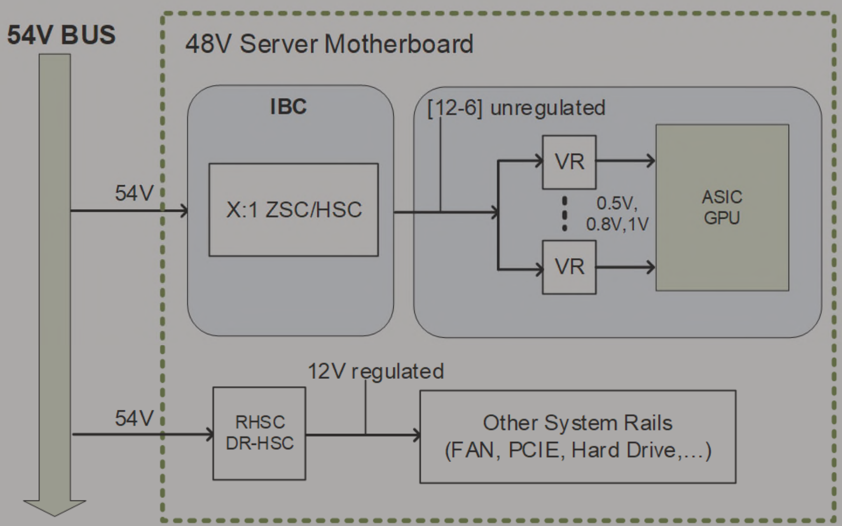
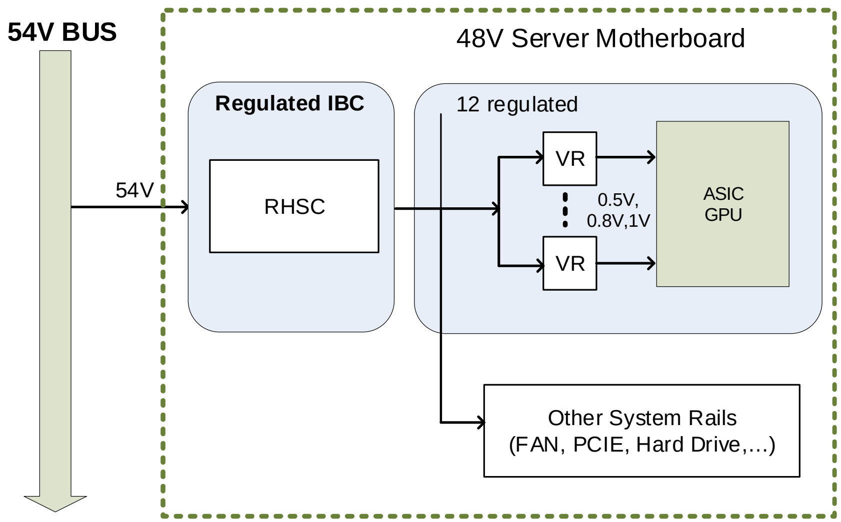
48 V to PoL application landscape

Unregulated IBC approach



- Most of the solution are not processing energy through physical inductor
- ZVS and/or ZCS can be easily achieved
- Suffers at low input voltage

Regulated IBC approach



- Required all/part of the energy to be processed by inductor
- Soft switching difficult to achieved (DC current component)
- Suffers at high input voltage

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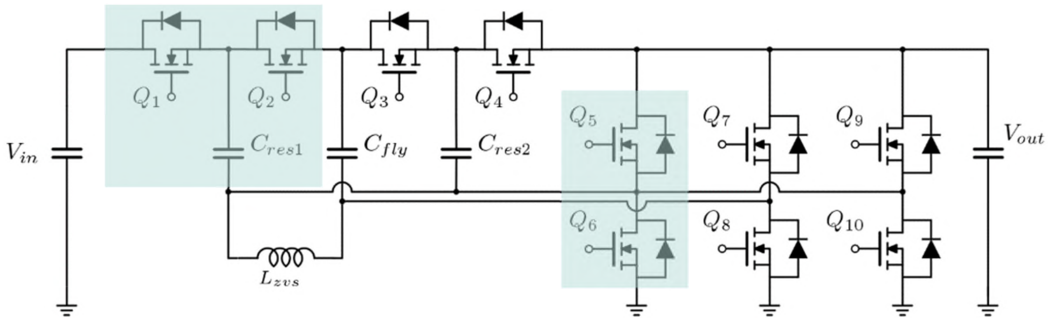
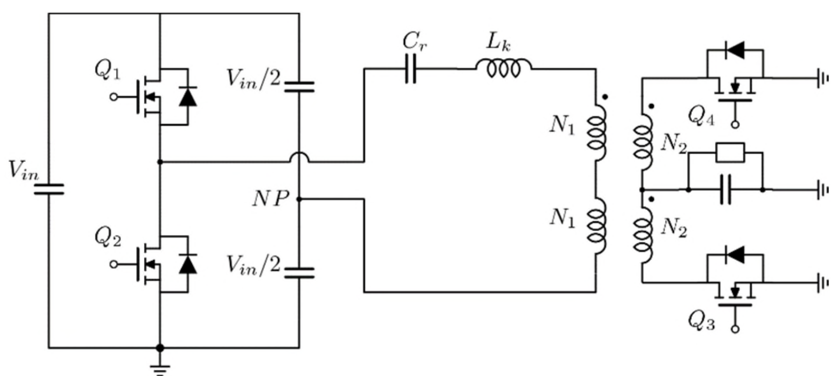
From Switched Capacitor to Hybrid Switched capacitor converters

Zero-Voltage switching switched capacitor converter

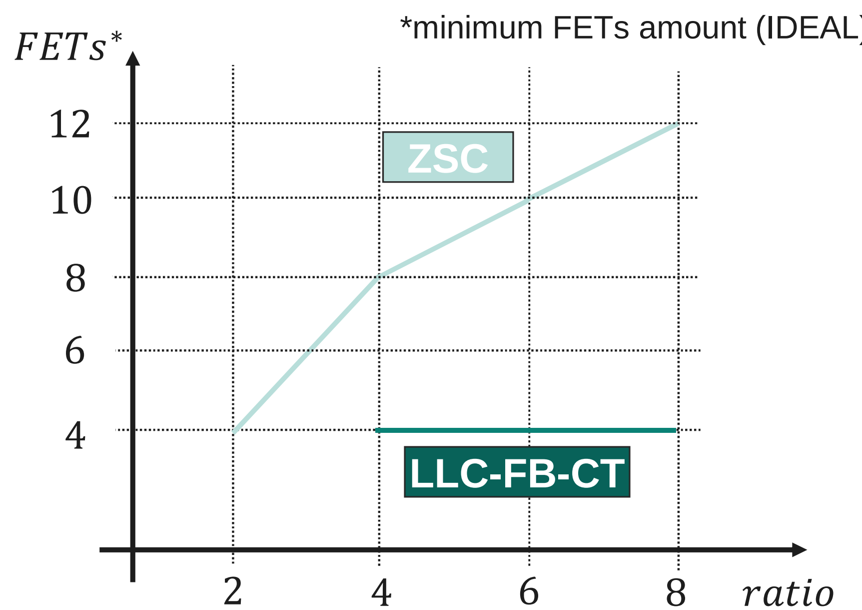


- SC based topology, ratio given from SC cells

LLC HB-CT



Transformer based topology, ratio given by transformer ratio



Hybrid Switched capacitor is combining SC cells with magnetic device

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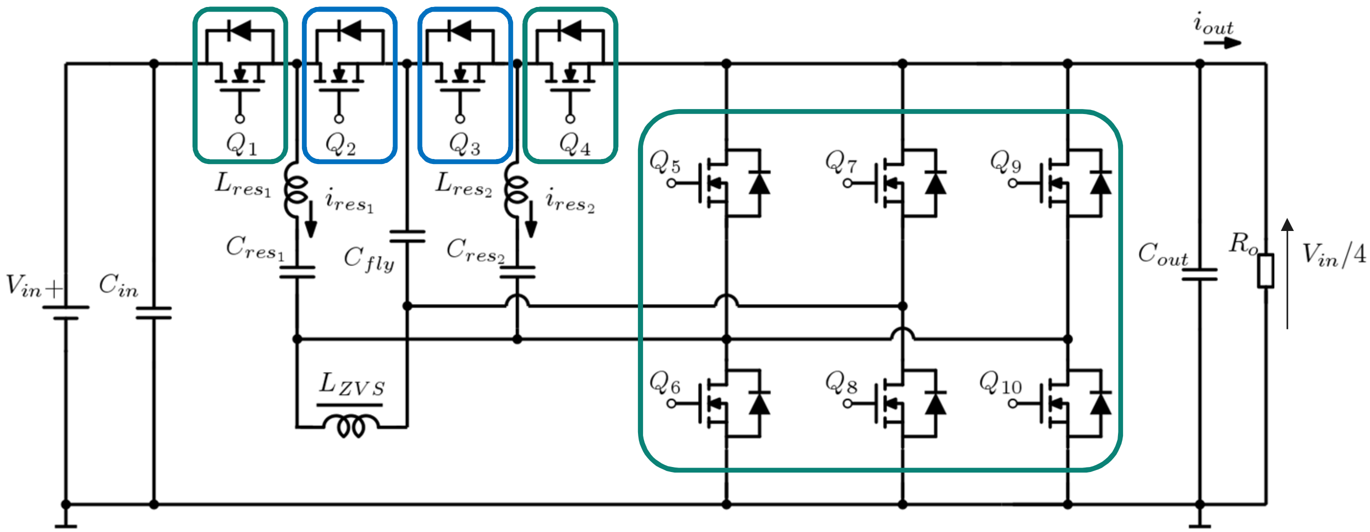
Zero-voltage-switching Switched Capacitor (ZSC) Converter



4 : 1 ZSC Stage

ϕ_α … Q_1, Q_3, Q_5, Q_8, Q_9

ϕ_β … $Q_2, Q_4, Q_6, Q_7, Q_{10}$

If V_{in} = 40 V - 60 V:

25 V *MOSFET*

40 V *MOSFET*

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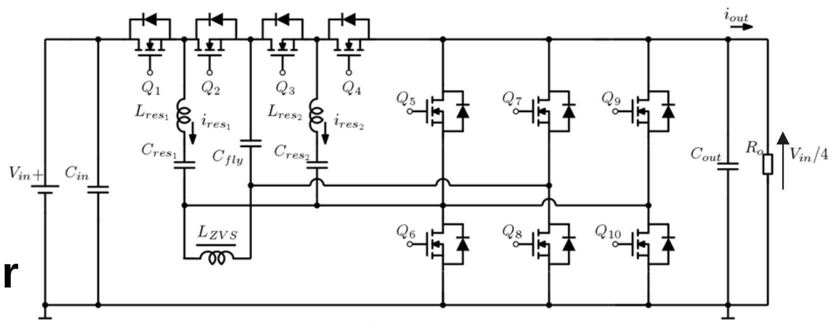
Zero-voltage-switching Switched Capacitor (ZSC) Converter

<u>Technical Features</u>



4 : 1 ZSC Stage

- Very **high efficiency** and **density** reachable
- Low voltage FETs with **better FOM (V_{out} , 2 x V_{out})**
- **Soft-switching** operation regardless of tolerance of components and input voltage variation (L_{ZVS} provides soft-switching capability)
- No power magnetic components in the main current path → **high power capability**
- **High switching frequency** operation possible due to ZVS switching
- Inherent **droop current sharing** for parallel operation

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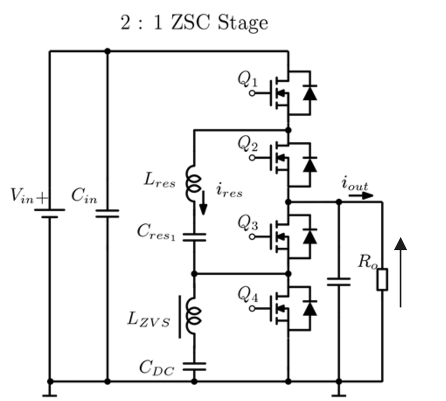
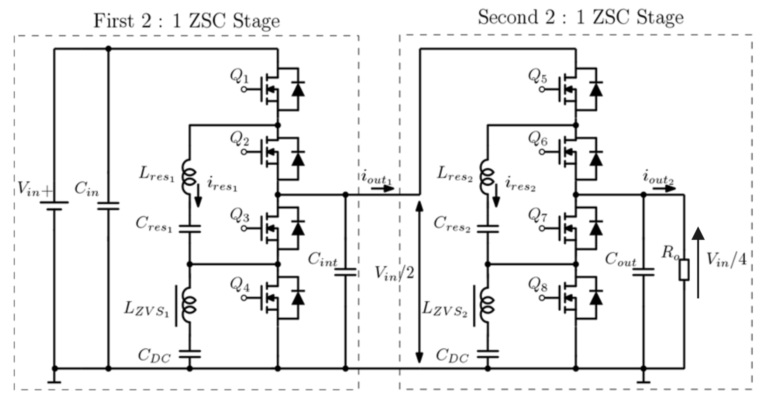
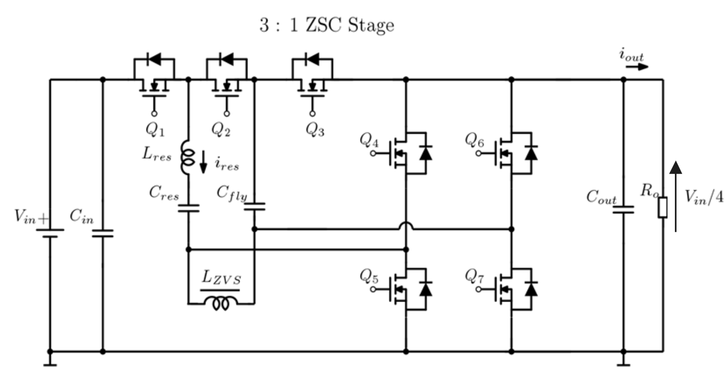
ZSC Implementation Flexibility



2:1 ZSC



Cascaded two 2:1 ZSC (4:1)



3:1 ZSC

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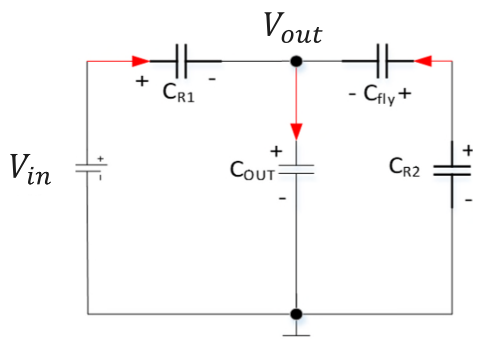
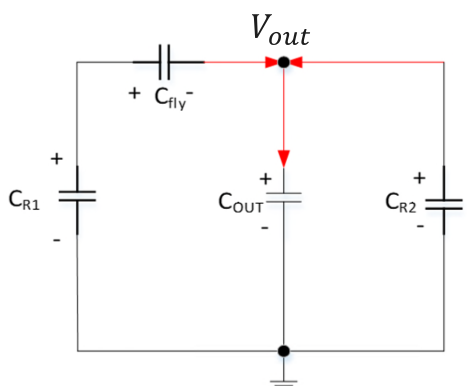
Calculation of Voltage Conversion Ratio in Steady-State

The average voltage of each capacitor can be calculated by combining the equivalent circuit in charging and discharging modes.





Charging Mode

$$V_{in} = VCR_1 + Vo_{ut}$$
$$V_{CR2} = Vout + VCfly$$

Discharging Mode

$$V_{CR1} = V_{Cfly} + Vout$$
$$V_{CR2} = Vout$$

$$V_{CR2} = Vout$$
$$V_{fly} = 2\,V_{out}$$
$$V_{CR1} = 3\,V_{out}$$
$$V_{in} = 4\,V_{out}$$

$$\boldsymbol{V_{out} = \tfrac{1}{4}\,Vin}$$

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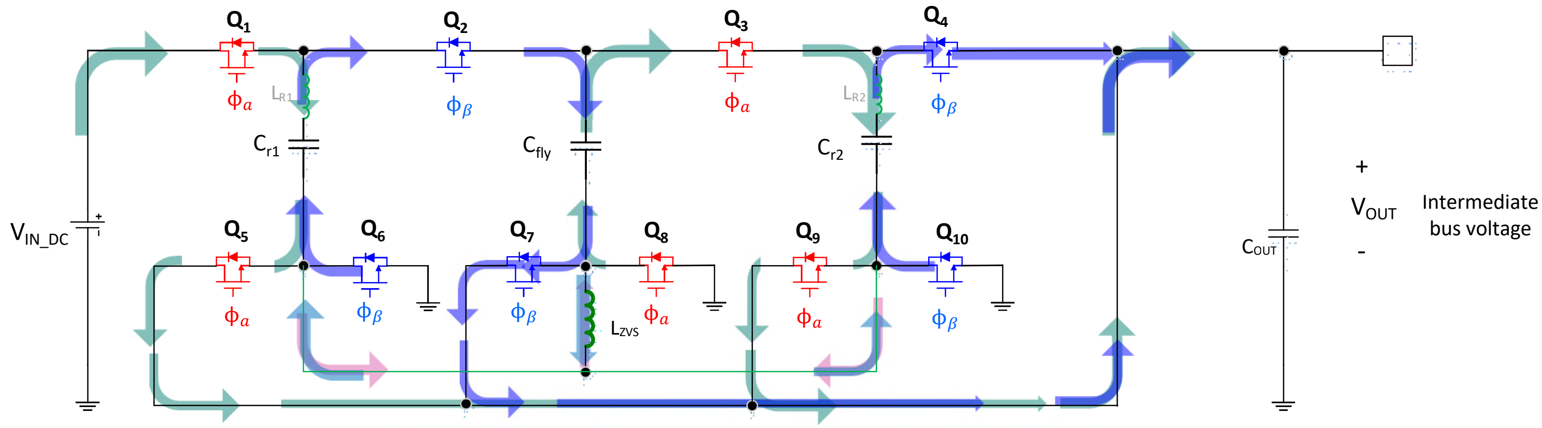
ZSC Topology in Action



Charging Cycle

- Energy flows from V_{in}, and energy flows out of cap C_{fly}
- Energy continues to flow and is charging the output
- At the same time energy flows out Lzvs

Discharging Cycle

- Energy flows out of cap C_{r1} and C_{r2}
- Energy continues to flow and is charging the output
- At the same time energy flows into Lzvs

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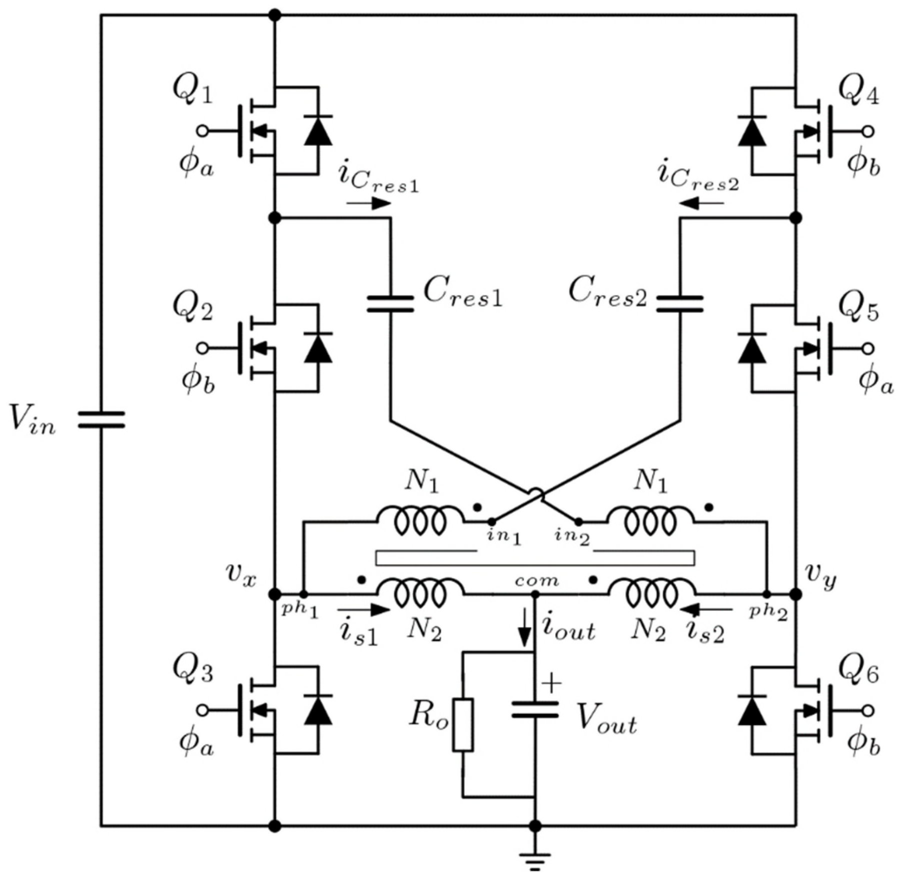
Hybrid Switched Capacitor HSC



- **Different ratios** are possible maintaining the same number of FETs 5:1 6:1 8:1 as optimized conversion ratio.
- **Soft-switching** operation regardless tolerance components and input voltage variation (L_m of the **Multi-Tapped Autotransformer** provides soft-switching capability)
- L_k of the **Multi-Tapped Autotransformer** ensure **soft-charging** of the C_{res1}, C_{res2} and C_{out}
- **Simplified driving system** (no need charge pump)
- **Symmetric operation** (less input current ripple)
- Q_2 and Q_5 have to block V_{in} in their off state
- Q_1 and Q_4 have to block $\frac{V_{in}}{2} + V_{out}\frac{N_1}{N_2}$
- Q_3 and Q_6 have to block $2V_{out}$voltage in their off state

$$\boxed{V_{out} = \frac{V_{in}}{4 + 2\frac{N_1}{N_2}}}$$

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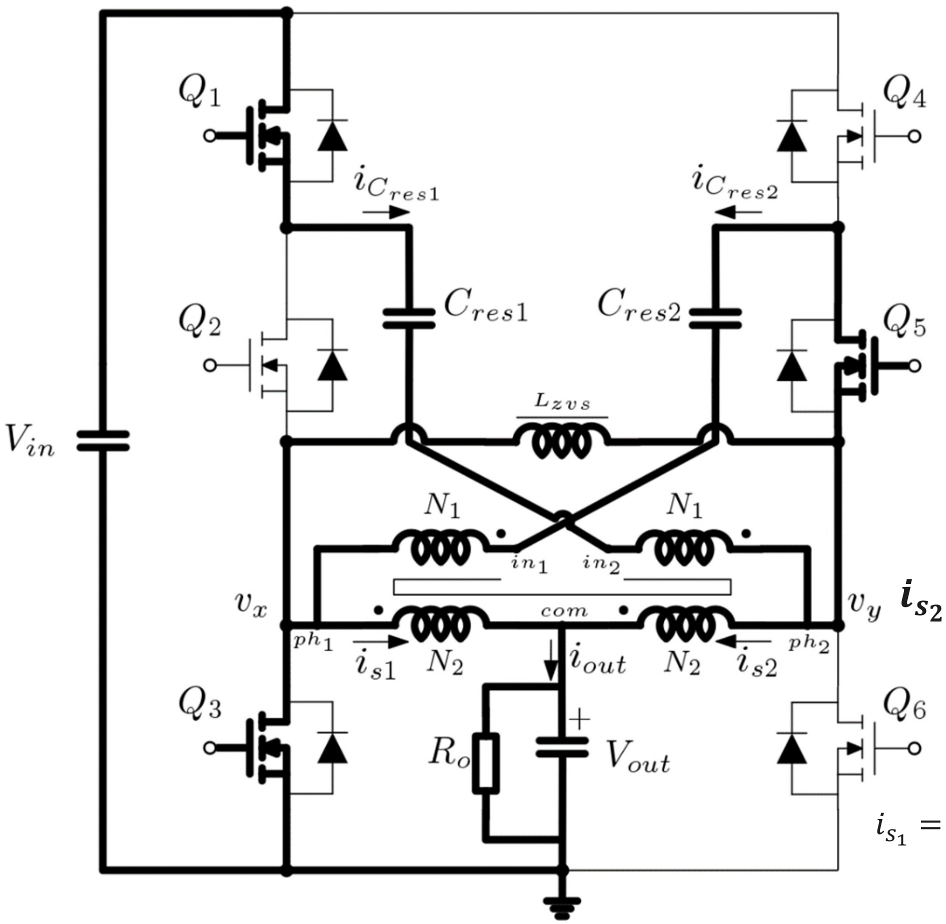
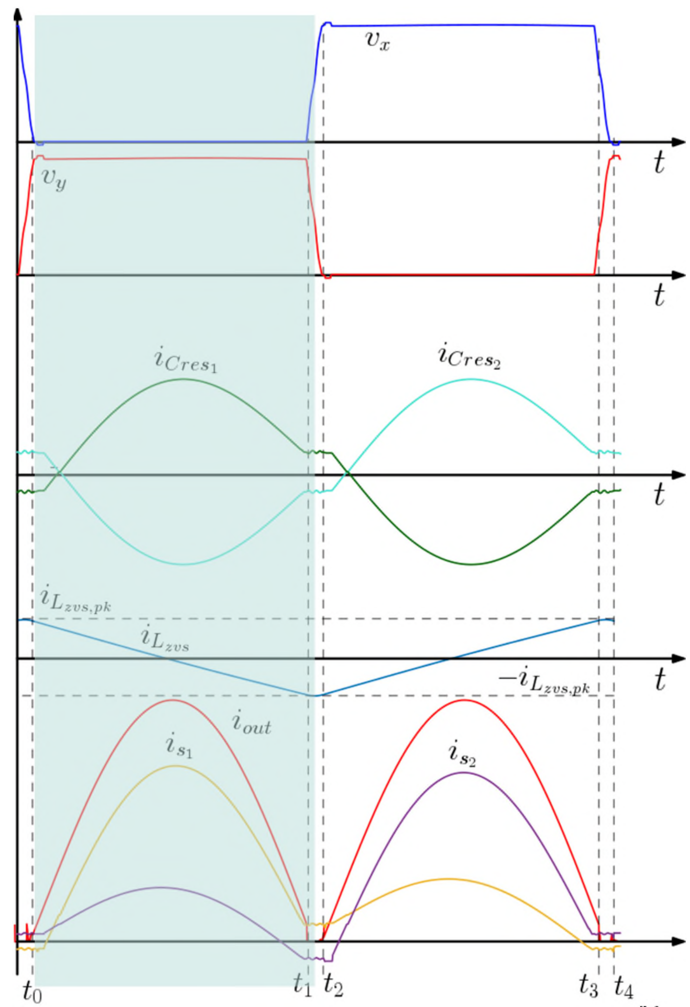
Phase Φ_A



$$i_{s_2} = i_{Cres_1} - i_{Cres_2} = 2i_{res}$$

$$i_{s_1} = \left(\frac{N_1}{N_2} + 1\right) i_{s_2} = \left(\frac{N_1}{N_2} + 1\right)(2i_{res})$$



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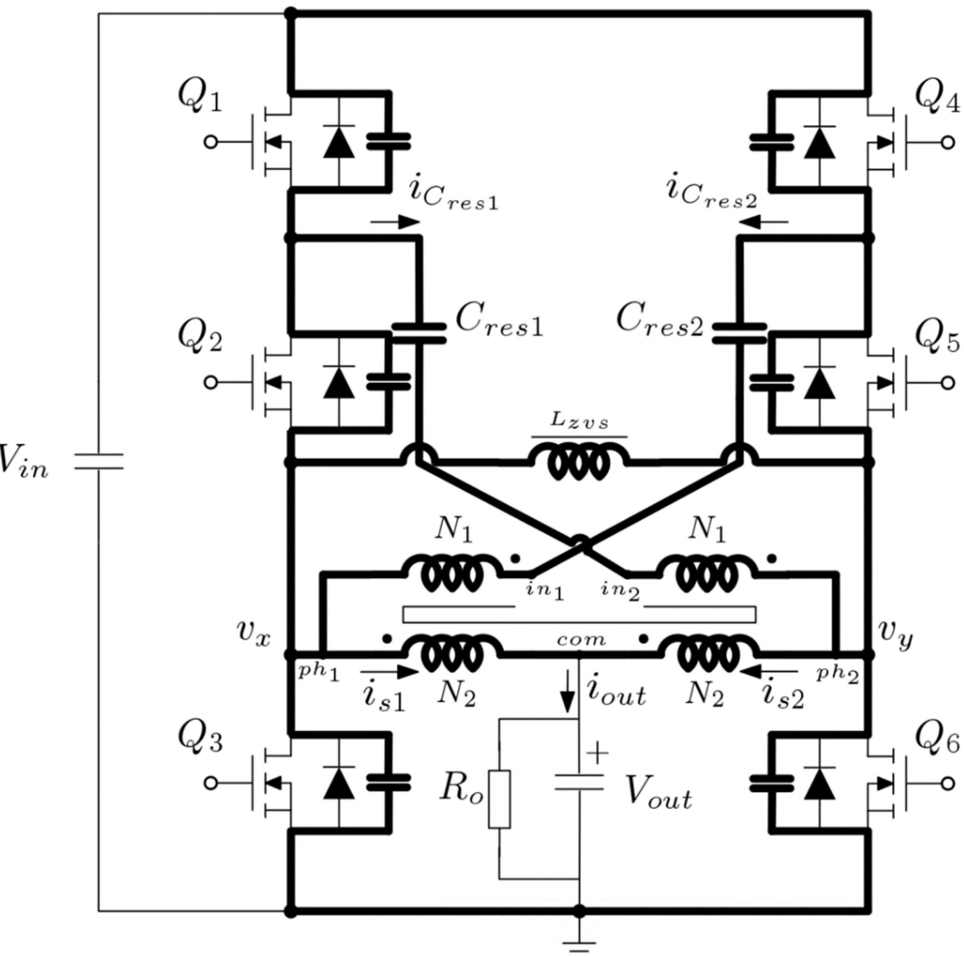
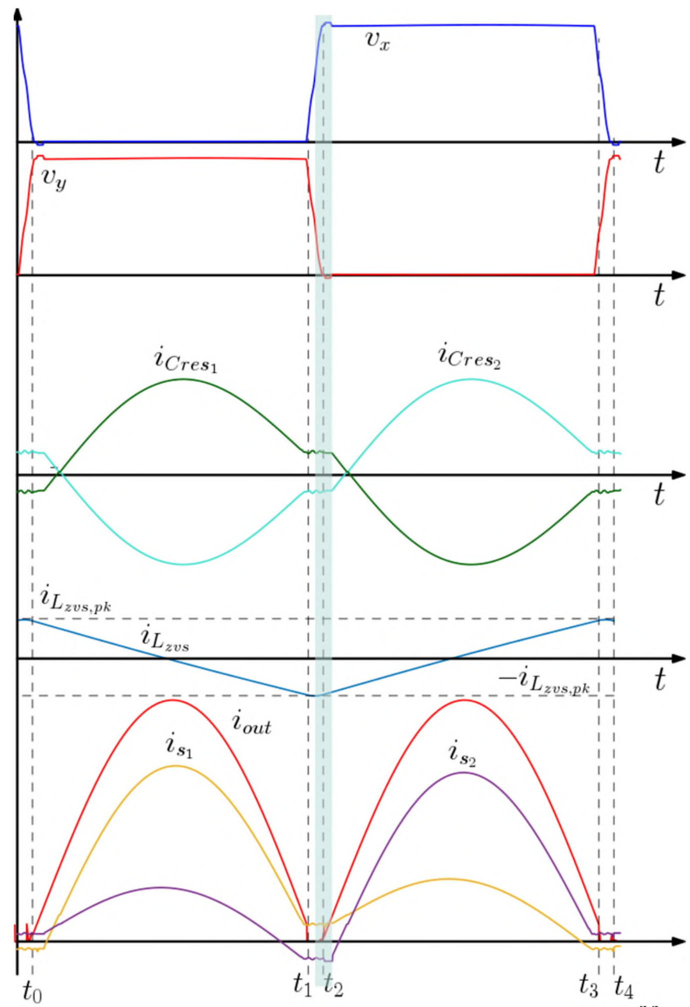
Dead time



- Symmetric ZVS operation for all FETs



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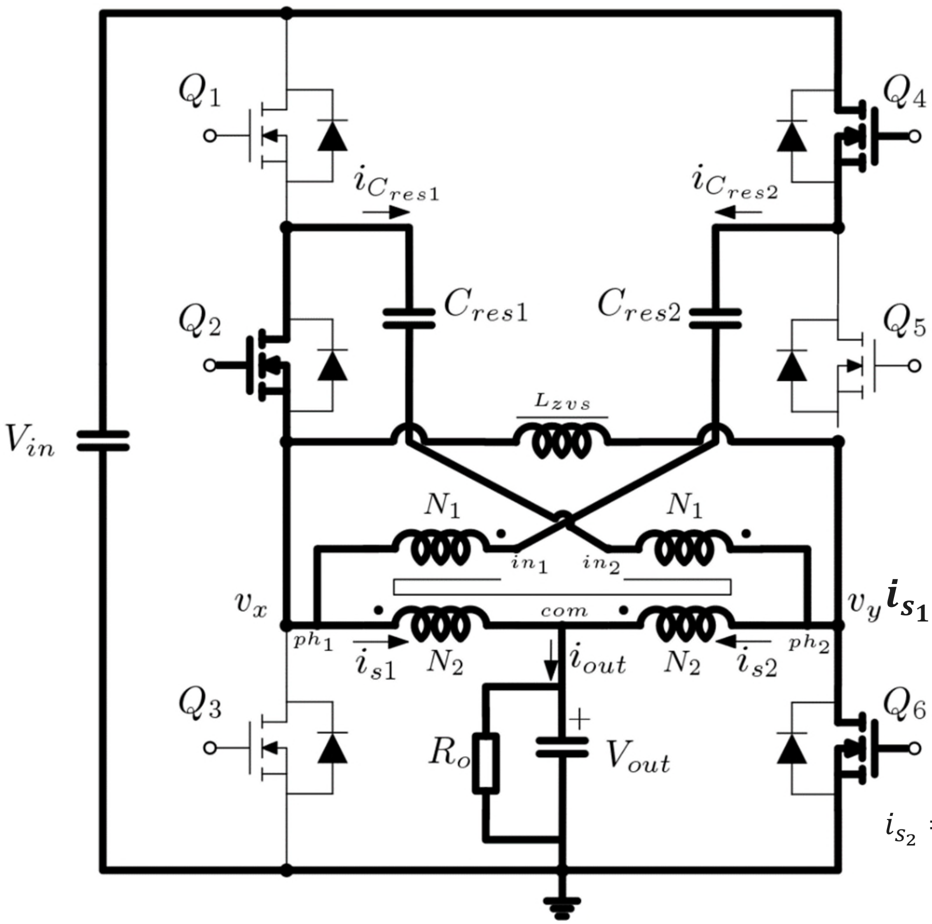
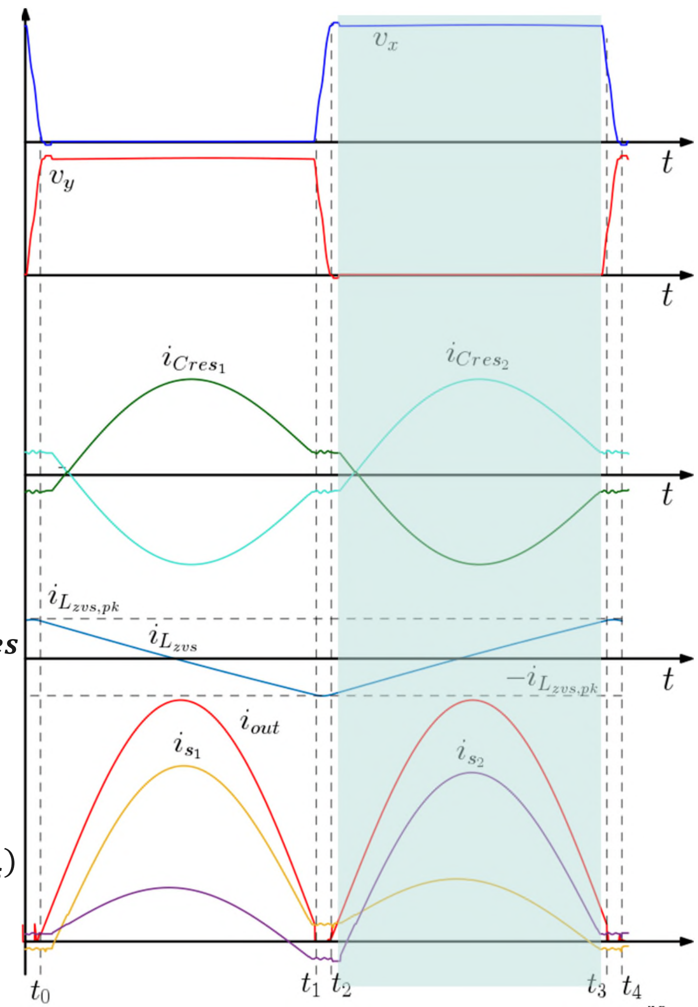
Phase Φ_B



$$i_{s_1} = -i_{Cres_1} + i_{Cres_2} = 2i_{res}$$

$$i_{s_2} = \left(\frac{N_1}{N_2} + 1\right) i_{s_1} = \left(\frac{N_1}{N_2} + 1\right)(2i_{res})$$



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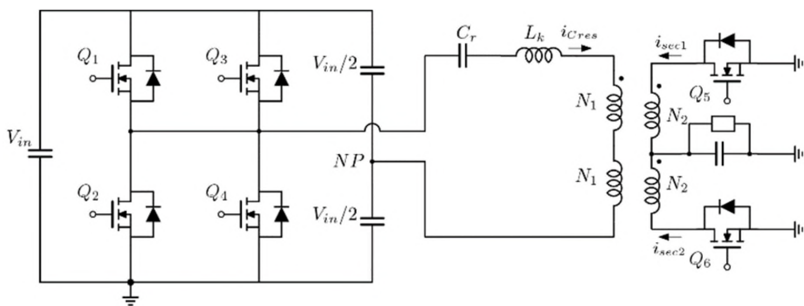
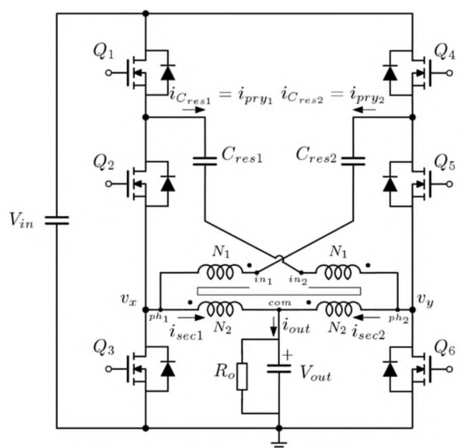
Comparison HSC with LLC-HB-CT converter

LLC HB-CT



Hybrid Switched capacitor



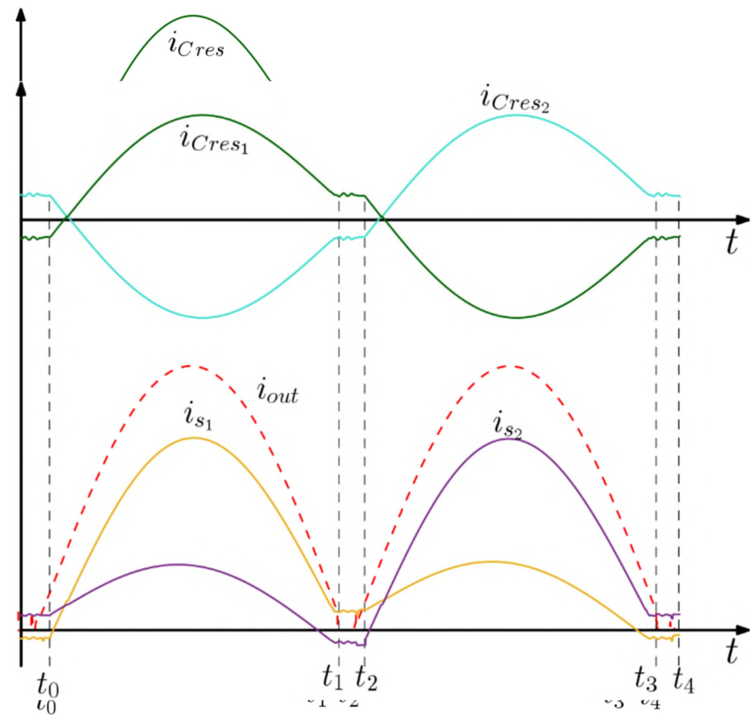
Both converter running at the **resonant frequency $f_{sw} \simeq f_{res}$**

High Q factor -> ZCS

Comparison with the same amount of FETs

ZVS ensures by the **magnetizing** inductance in **HSC** and **LLC**

Hybrid Switched capacitor waveforms



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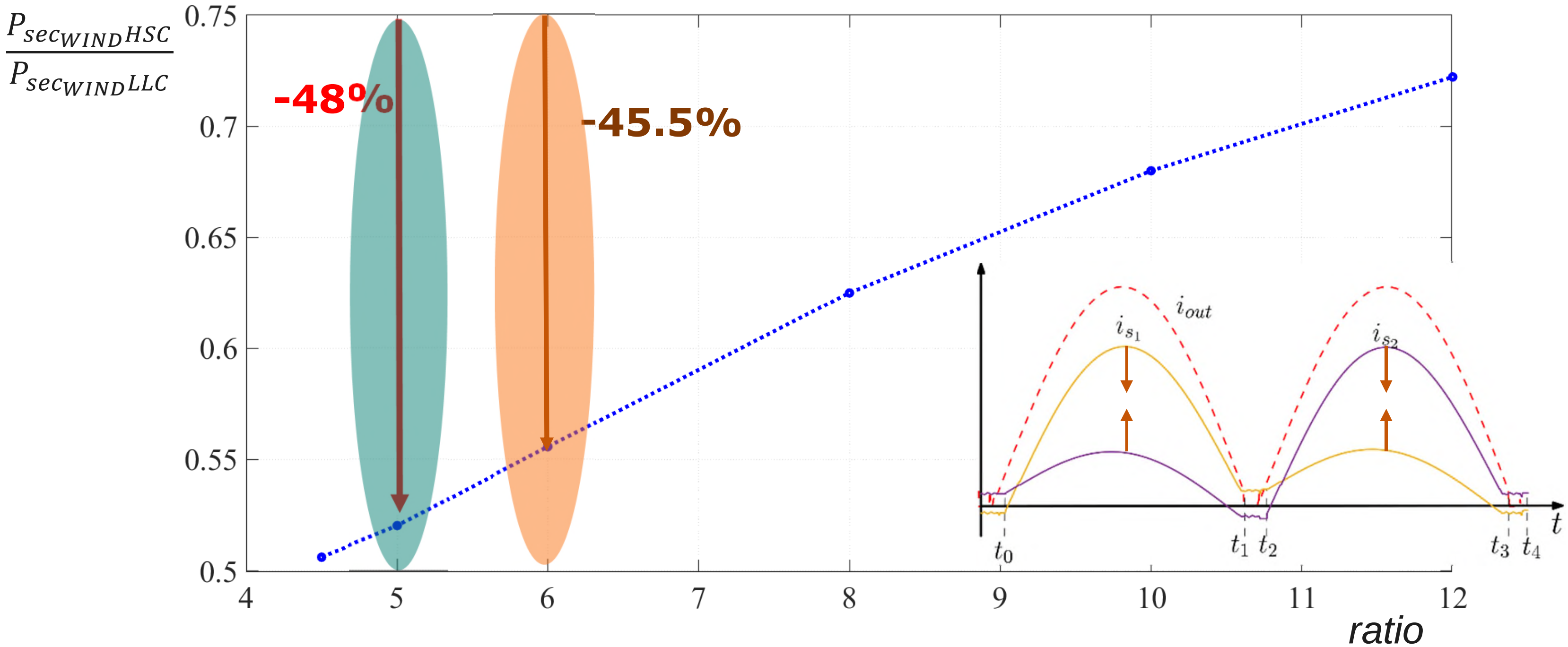
Theoretical comparison between LLC and HSC
Secondary windings losses

Comparison conduction losses on secondary winding



In **5:1 HSC**, considering $\boldsymbol{R_{sec_{HSC}}} = \boldsymbol{R_{sec_{LLC}}}$, the **conduction losses** on secondary windings are **reduced** by **48%.**

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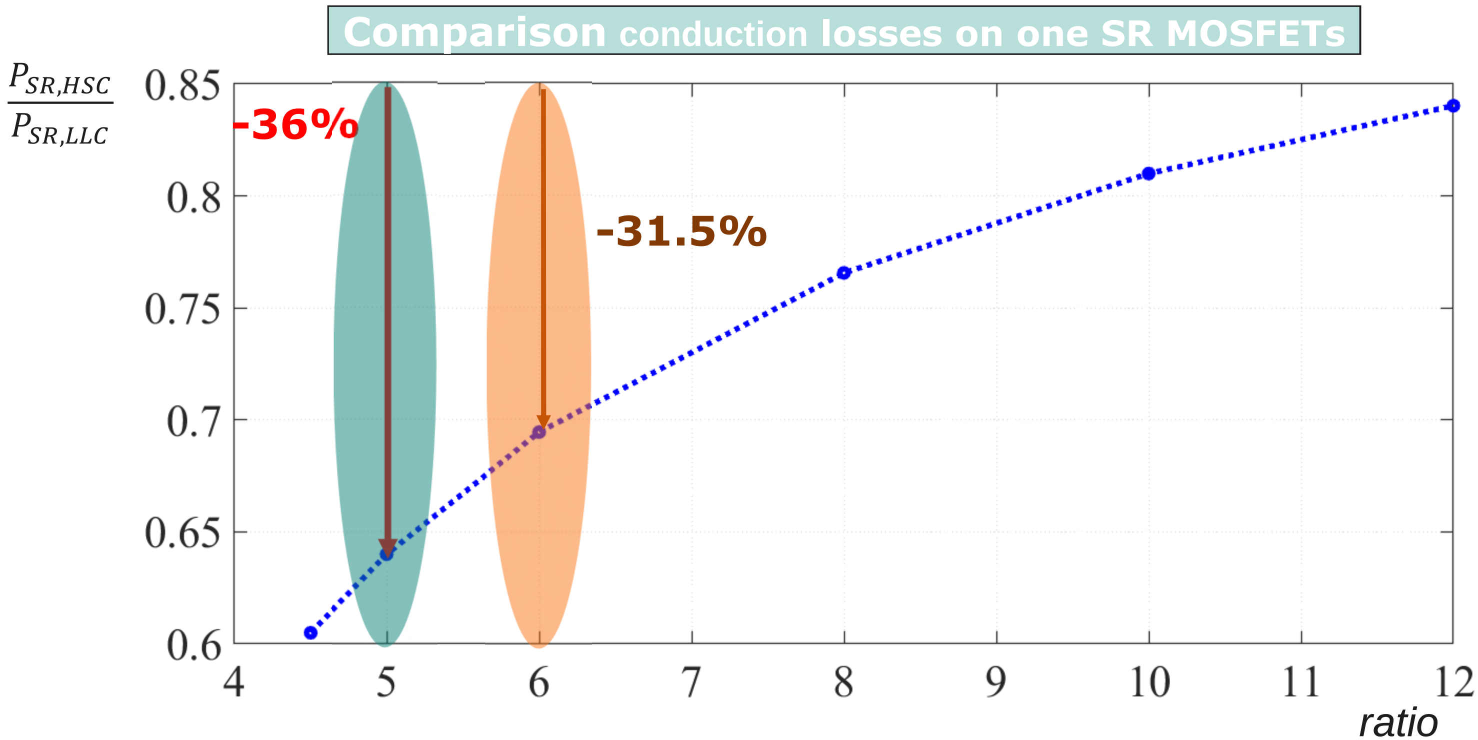
Theoretical comparison between LLC and HSC
SR MOS losses



In **5:1 HSC**, considering $\boldsymbol{R_{on,SR_{HSC}} = R_{on,SR_{LLC}}}$, the **conduction losses** on SR FETs are **reduced** by **36%.**

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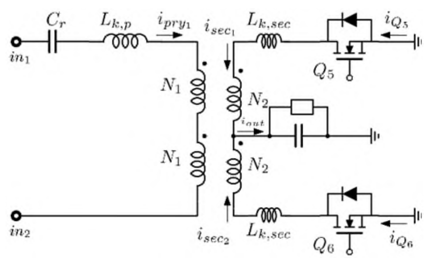
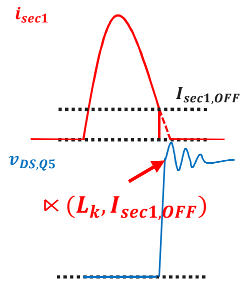
Robustness of HSC comparing with LLC

LLC

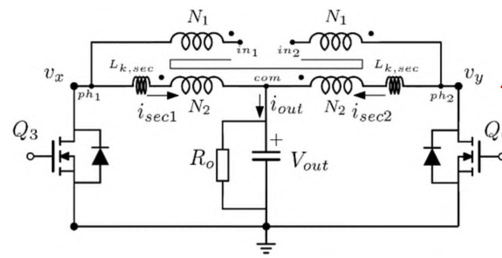
No ZCS

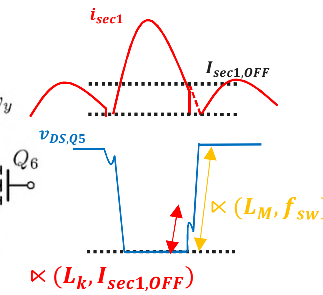




- If LLC is not in **ZCS** there are **additional losses** proportional with the leakage inductance of secondary windings and the turn-off secondary current

HSC

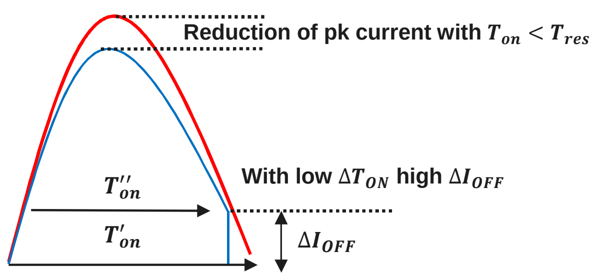




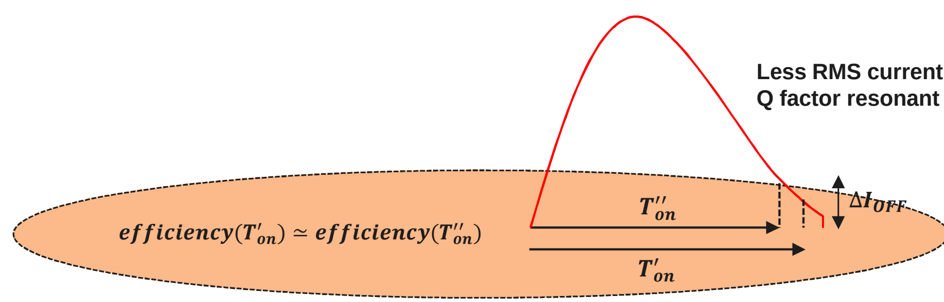
- If HSC is not in **ZCS** there is **not anymore** a dependence with the turn off current in terms of **losses** because of **ZVS** operation in all FETs.

Resonant tank Q factor

With high Q factor resonant tank



With low Q factor resonant tank



HSC magnetic can guarantee low leakage inductance, so as low energy impacting ZVS perfomance and chance to run over resonant frequency improving efficiency and realibaility in mass production

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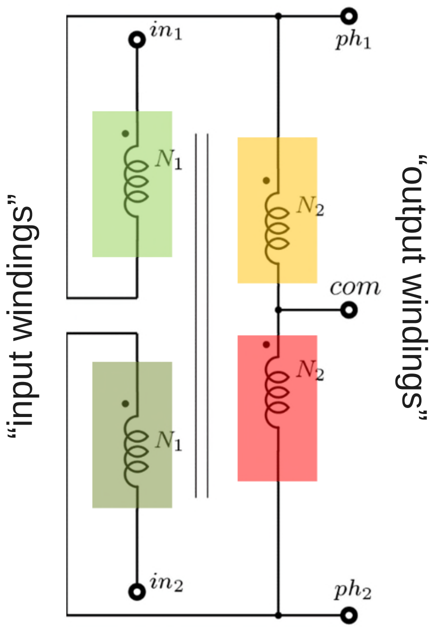
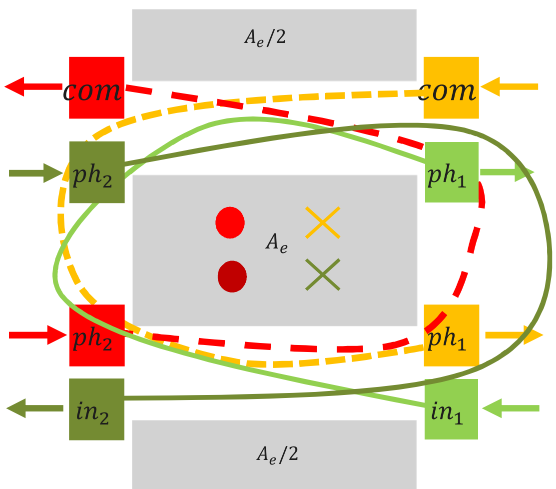
Multi-tapped autotransformer

Multi-tapped



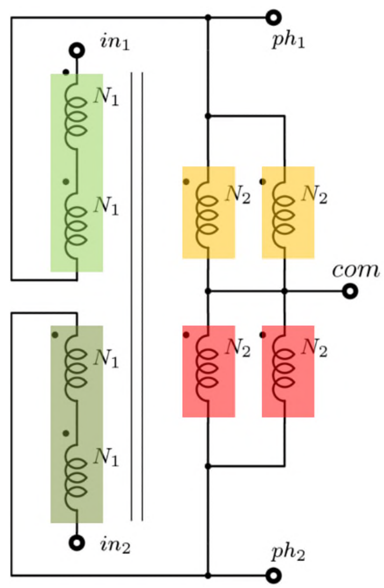
MTA

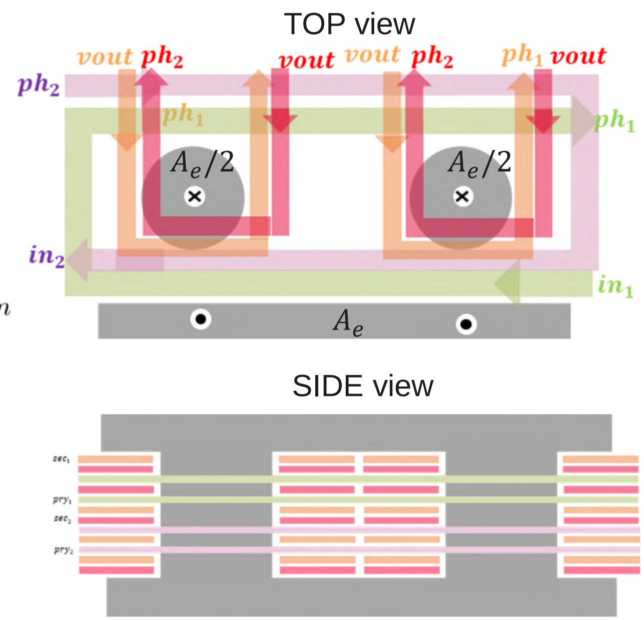


MTA Core and windings structure

- Core volume optimization
- Optimal for <500W 8:1 IBC

Matrix Multi-tapped





- Conduction losses optimization
- Optimal for >500W 8:1 IBC

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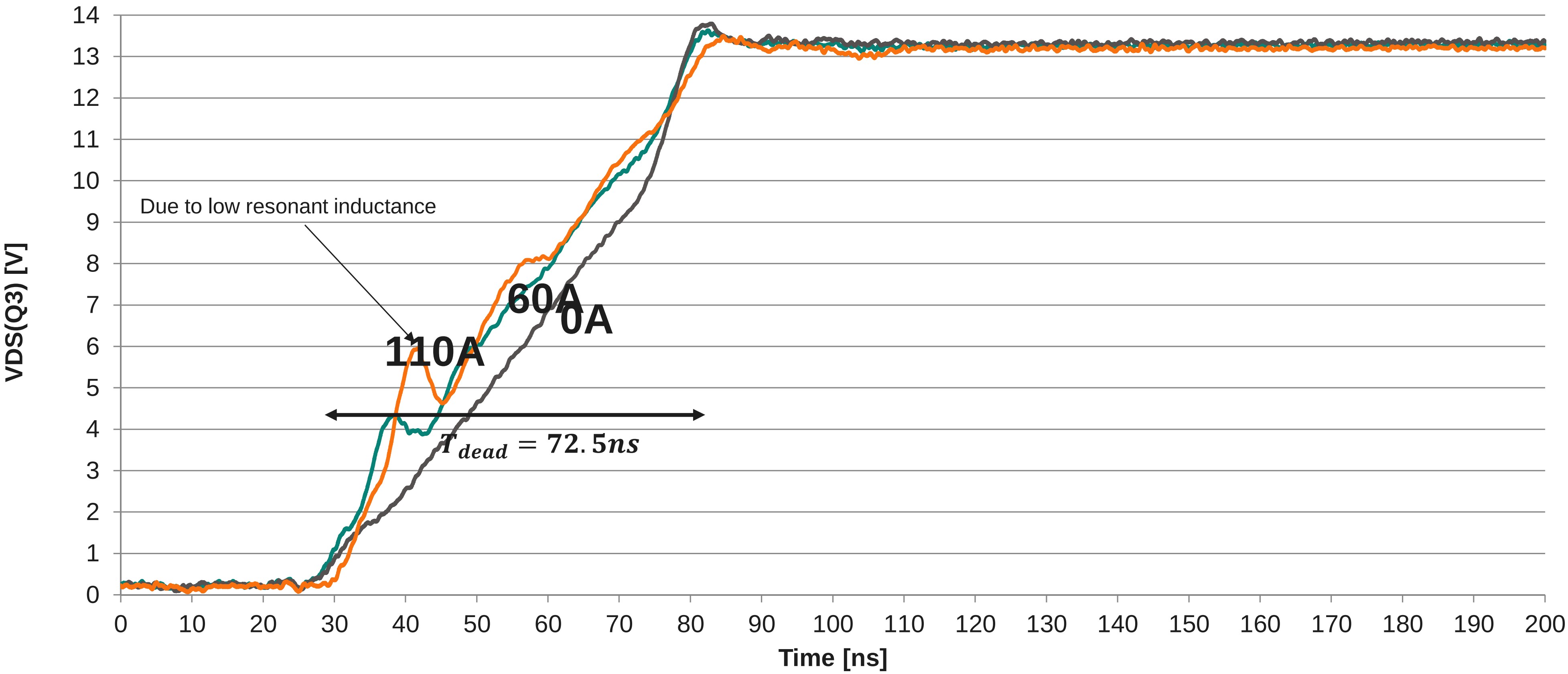
ZVS behaviour over load – Experimental waveforms



– HSC can run above resonant frequency (to reduce RMS current) without compromise ZVS capability when low Q factor can be implemented (i.e. in a module solution)

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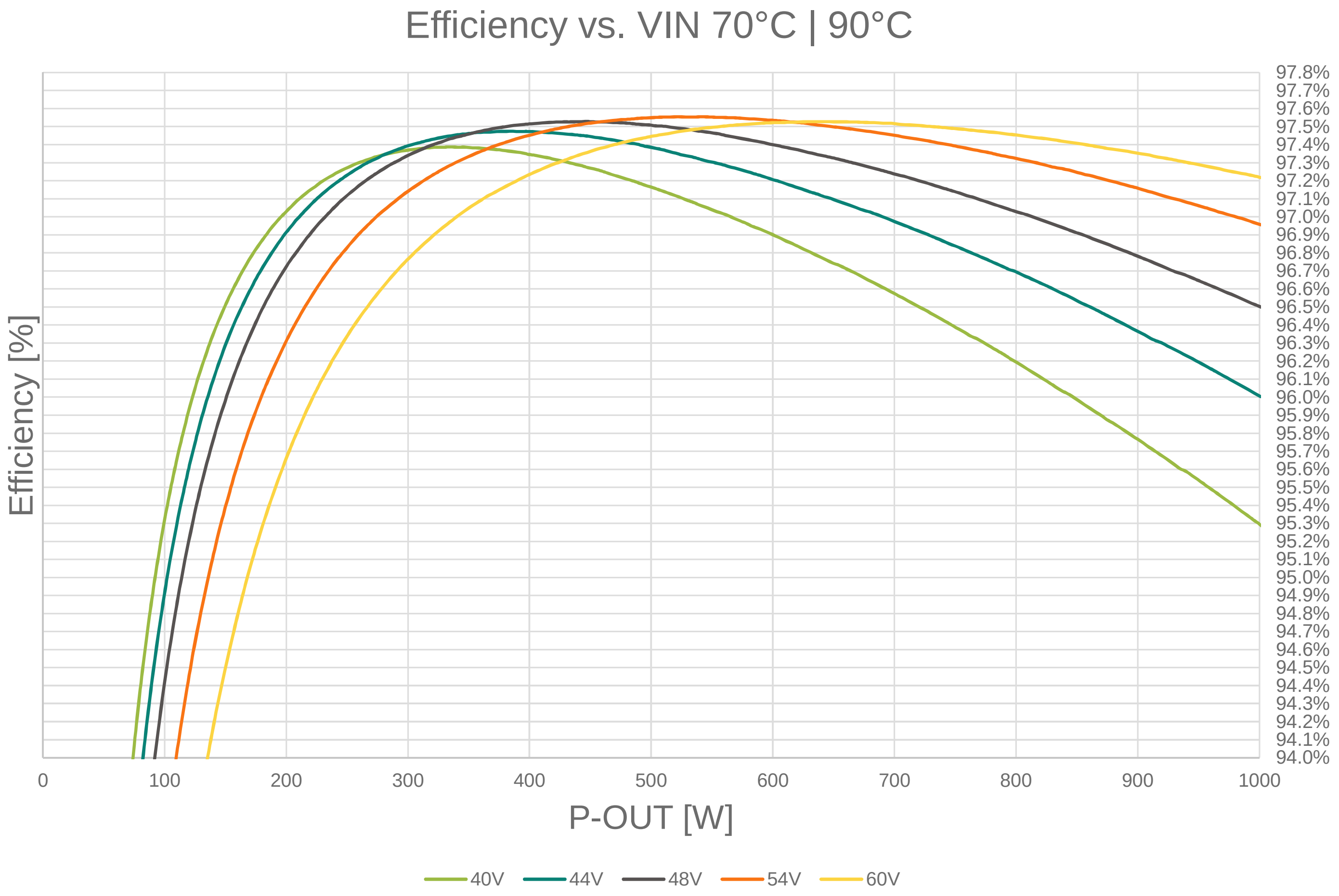
Measured HSC efficiency in challenging thermal environment



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Abstract:

The requirements for power systems that support high-performance AI computing infrastructure with 40 V to 60 V inputs are becoming increasingly challenging. Higher efficiency and power-density requirements are changing rapidly, and the thermal environment is becoming more difficult to manage. To manage PDN losses, power must be delivered closer to the point of load, and intermediate bus voltages require flexibility to achieve the best overall efficiency and transient response. Chris R. Swartz will discuss how adding a multi-tapped autotransformer to the super-efficient ZVS switched-capacitor topology creates the Hybrid Switched-Capacitor (HSC) topology and enables additional flexibility in conversion ratios without increasing the number of cells or the number of power switches. The benefits of the HSC topology as a means of providing over 1 kW of intermediate power, with transient capability of 2× TDP and high conversion efficiency in thermally challenging environments, will be discussed. Additional system benefits — such as a novel startup scheme, simple droop current sharing, and the ability to synchronize multiple stages — will be shown.

Seminar Presenter:

Chris R. Swartz is a Senior Member of the IEEE with more than 36 years of experience in power electronics design. He began his career at Motorola Inc., where he worked on both digital and power electronics during a ten-year tenure there. Chris then spent 14 years at Emerson Network Power (formerly Artesyn Technologies), designing both fully custom and standard AC–DC and DC–DC products. Chris subsequently worked for two years at Transim Technology, focusing on advanced power electronics and thermal simulation, before embarking on a 16-year career with Vicor Corporation as a Senior Principal Engineer. Last February, Chris joined Infineon as a Lead Principal Engineer, what he calls his most exciting role yet!