High Efficiency and Density Using New Generation Semiconductor Packaging

IEEE Long Island Power Symposium

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OUTLINE

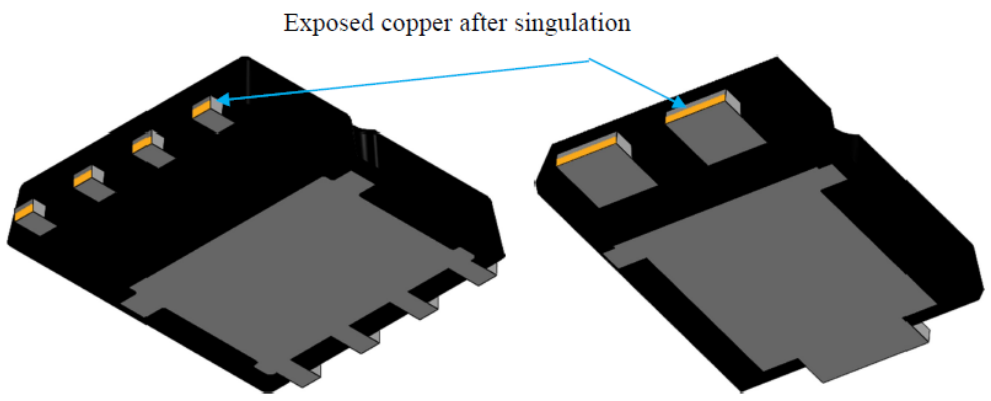
- What is a Wettable Flank Package?

Normally PDFN56 and SMPC4.6 package pins of lead frame generated by the singulation process from the strip during package assembly. The singulation process will make pin surface exposed copper and there lacks plating in the exposed surface. The exposed copper will easily suffer oxidation which prevents it from being solder wettable and a solder fillet does not typically develop (Figure on the left).

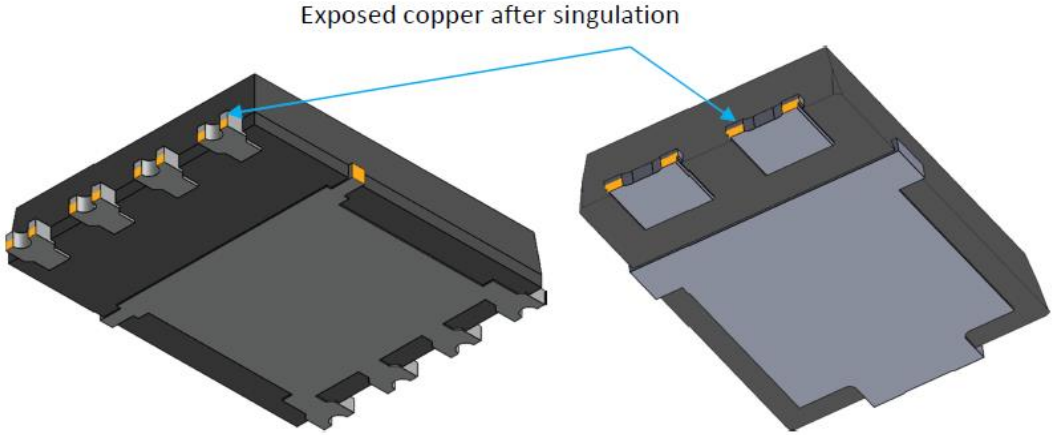
How do we lower the pin surface exposed copper area after the singulation process to avoid pin oxidation?

This kind of improving package lead frame is called a ***"Wettable Flank"*** packages of PDFN56**U** and SMPC4.6**U**. These packages are designed with more lead frame to gain more plating area after singulation process. This provides good adhesion between the Tin solder and lead frame pin after reflow process (Figure on the right). The solder tin amount combine with extended lead frame help pass a higher yield rate of device solder reliability.

- PDFN56, SMPC4.6 Package:

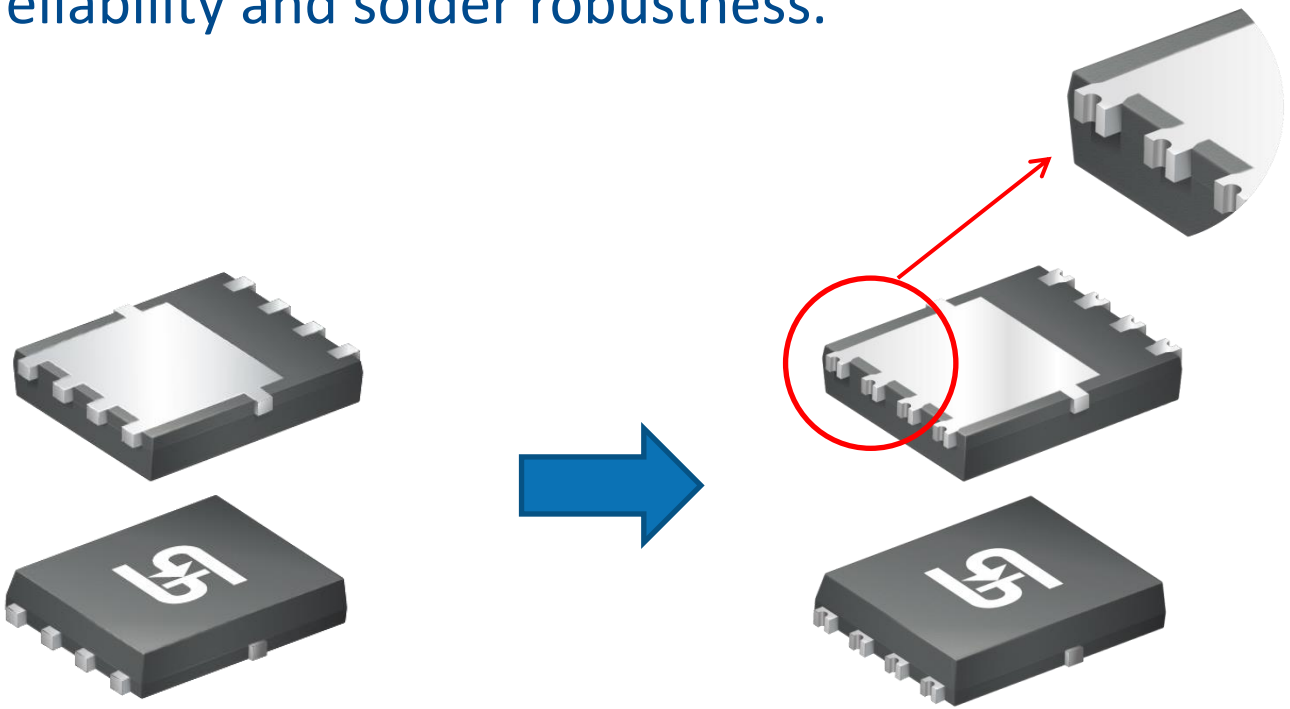


PDFN56**U**, SMPC4.6**U** Package:



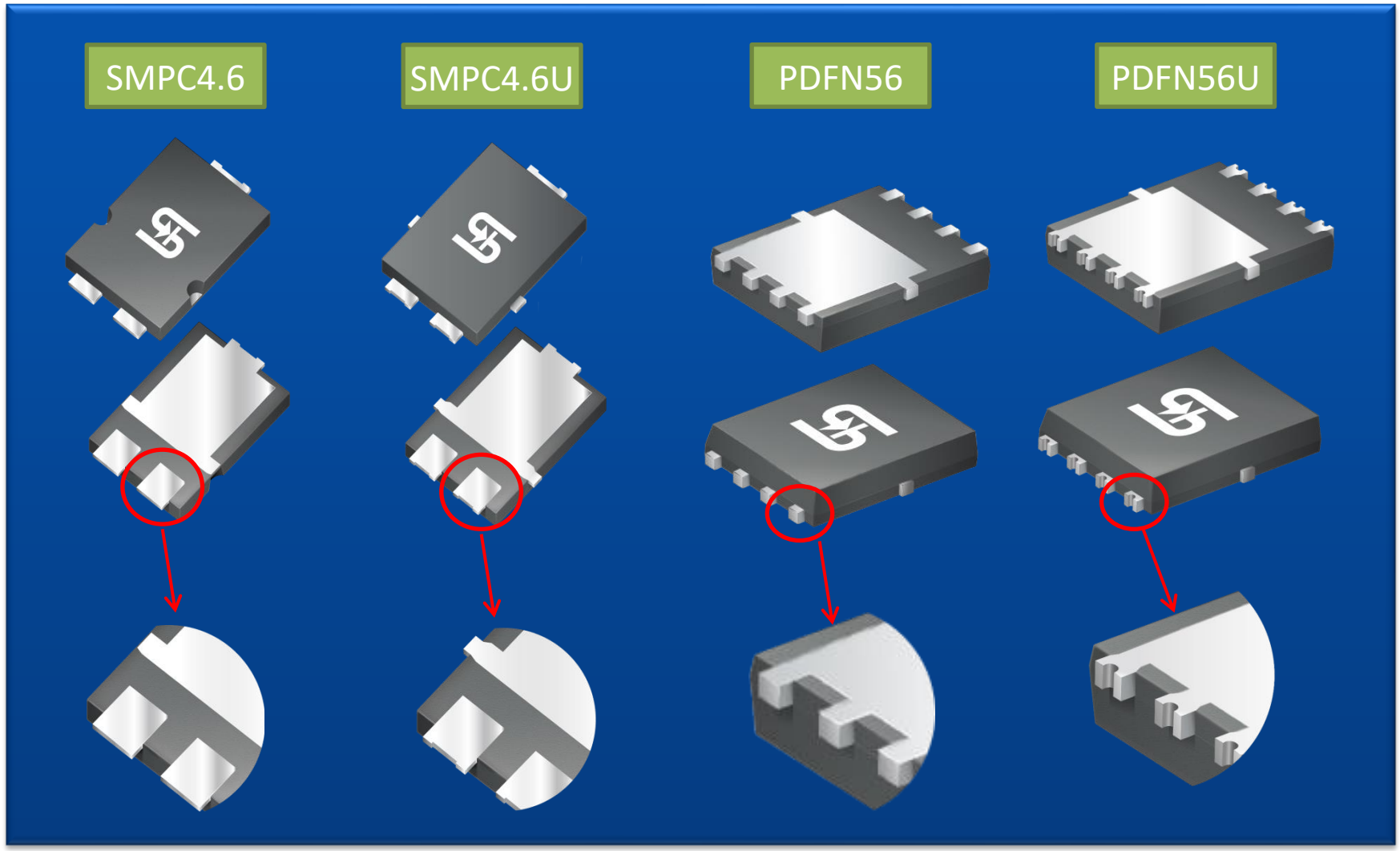
ABSTRACT

Considering PDFN56 (SMPC4.6) SMT onto PCB, there is an idea to improve the solder robustness by applying an U-shape lead-tip. Using a PDFN56 (SMPC4.6) package with a wettable flank enables optical inspection of soldering. Which can increase product reliability and solder robustness.



WETTABLE FLANK

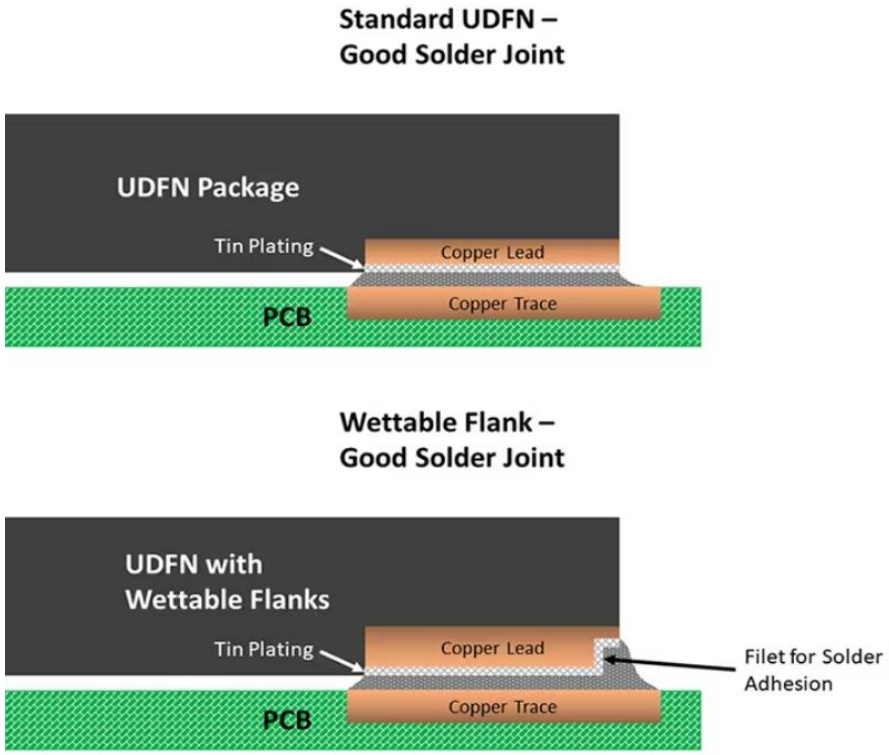
- Differences In Pin Type:

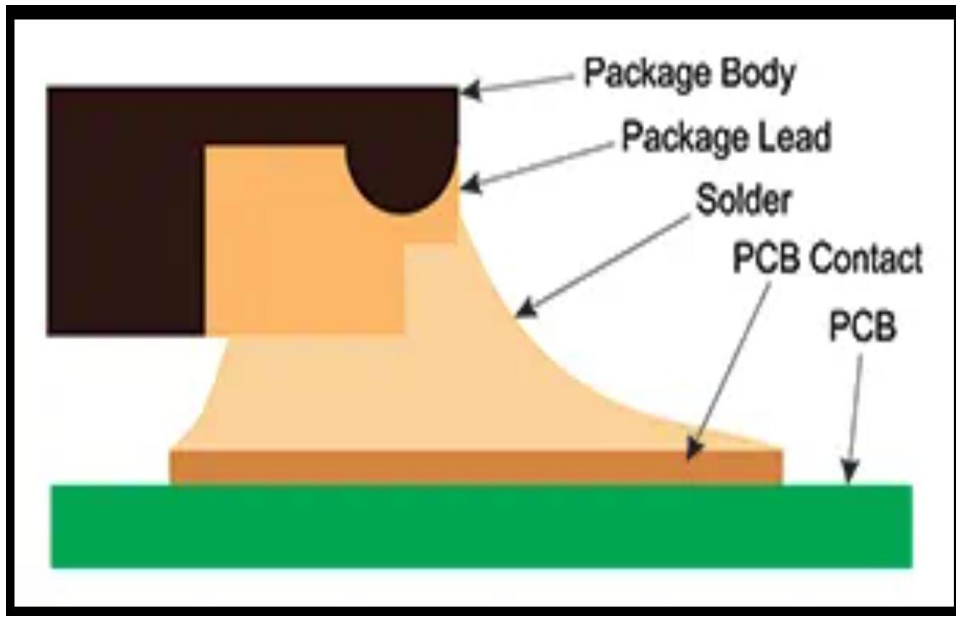


OUTLINE

- What is a “Wettable Flank” Package?

In surface-mount semiconductor package terminology, particularly for QFN (Quad Flat No-lead) or DFN (Dual Flat No-lead) packages, a *wettable flank* refers to a modification of the package termination geometry and plating so that solder can visibly wet (flow up) the side flanks (edges) of the terminations after reflow. This offers a visible solder fillet at the side of the part, which allows for optical inspection of solder joints on the side of the package.





OUTLINE

- How did we get here?
  - Evolution. Thru Hole, surface mount gull wing, surface mount flat package, QFN
  - Each generation solves a new problem and creates trade offs
  - Wettable flank addresses the ability to test, inspect, and form more reliable solder joints
  - Why is it important for electronic power designs?

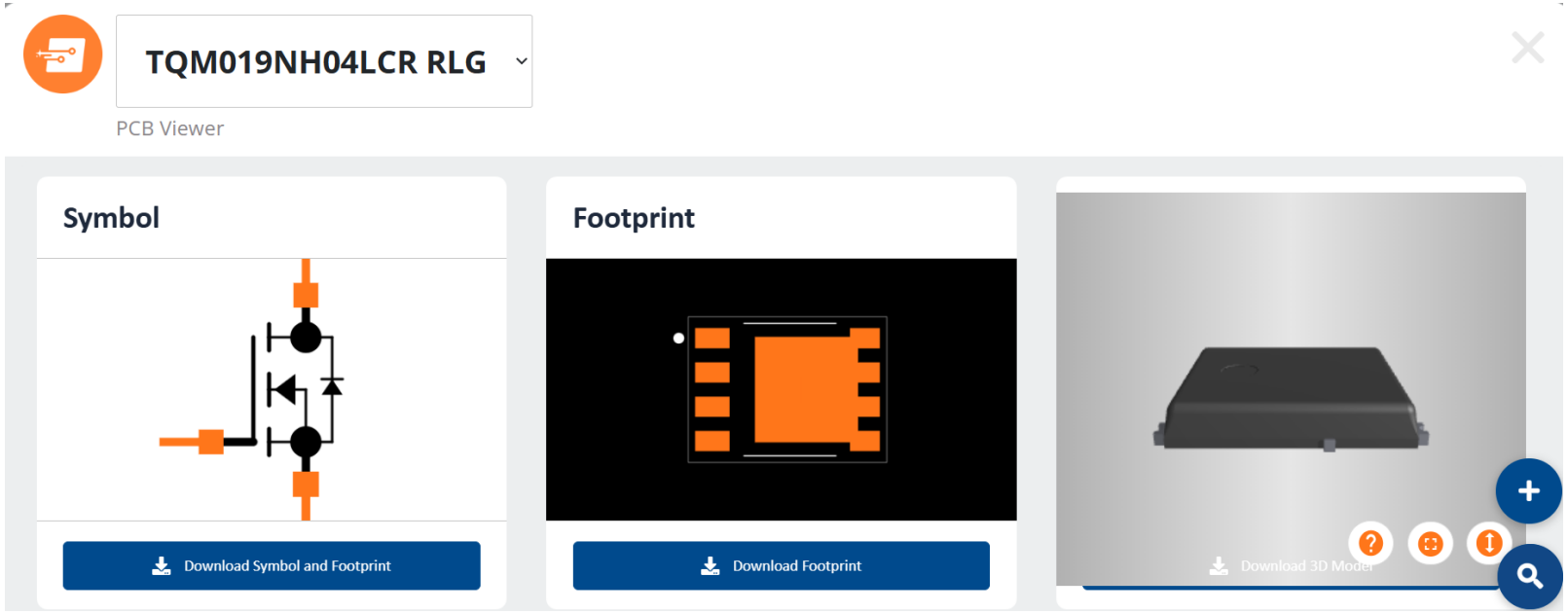
- Leveraging the expertise from Automotive for any design
  - The origins of the wettable flank stem from the Auto Manufacturers and Automotive Suppliers.
  - Wettable Flank Packaging has been around for years at this point and has only gained more traction
  - Automotive Manufacturers and Suppliers have made this the Standard for RFQ's in certain applications
- Something for everyone
  - Available for AEC-Q and commercial parts
  - Industry standard footprint allows for AVL flexibility
  - Improved manufacturability with AOI
  - Engineers power density, 55% greater surface area = lower parasitic contact resistance
  - Uses less board space than leaded packages
  - Improved reliability & durability
  - Less risk in the design
- Test methodology
  - Thermal Cycling, Thermal Shock, as well as Board Flex

THE NEED FOR WETTABLE FLANK

- Why was “Wettable Flank” Developed?
- Standard QFN/DFN packages are often singulated by sawing or punching, leaving exposed copper side-walls on the lead-frame terminations (because the plating covers the bottom termination surfaces, but the sides may expose bare Cu). These exposed copper side walls oxidize and do *not* reliably wet during reflow, meaning there is no visible solder fillet on the side of the package terminations.
- With after board assembly it can be difficult (or impossible) to visually verify good solder joints for those side terminations. Without visible fillets, inspection via optical means (AOI) is limited, and sometimes only electrical test or X-ray can verify the joint.
- In automotive, aerospace or other high-reliability manufacturing environments, visual inspection of solder joints (via AOI or optical microscopes) is often required or strongly preferred, to verify solder quality and fillet formation. The wettable flank modification was developed to enable side fillet visibility and simpler inspection.

MODIFICATIONS

- What Modifications are Involved with “Wettable Flank” Packages?
- After singulation (e.g., sawing), the side of the terminal is modified (for example a step or dimple is cut to expose more lead-frame metal on the flank).
- A full tin (or other solderable finish) plating is then applied such that the flank (sidewall of the termination) is plated, not just the bottom surface. This ensures solderability on the side.
- The PCB land/footprint is adjusted: the pad land may be extended (further length) so that solder paste can allow solder to flow and form a fillet up the sidewall. For example, the manufacturer will recommend extending pad lands (e.g., from 1.0 mm to 1.2 mm) to enable solder to flow to the flank.



BENEFITS

- What are the Benefits of a “Wettable Flank” Package?
- **Improved inspection visibility**: Because solder fillets are visible on the sides of the package terminations, automatic optical inspection (AOI) systems or human visual inspection can more easily verify proper soldering. This is especially important in automotive or functional-safety systems.
- **Better solder joint reliability (potentially)**: With a proper solder fillet forming on the side of the package termination, the mechanical robustness of the solder joint may improve (better fillet shape, increased solder volume on side). For example, one document states that wettable flank leads improve solder joint reliability and inspection accuracy.
- **Enables use of high-density QFN/DFN packages in high-reliability environments**: As package sizes shrink and lead-frames become finer pitch, it becomes harder to inspect underside solder joints. Wettable flank provides a way to maintain inspection capability.
- **Less need for X-ray or complex inspection for side terminations**: Standard QFN/DFN without wettable flanks often require X-ray or cross-sectioning to verify side termination solder because sidewalls don’t show solder fillets. With wettable flanks, visual inspection is viable.

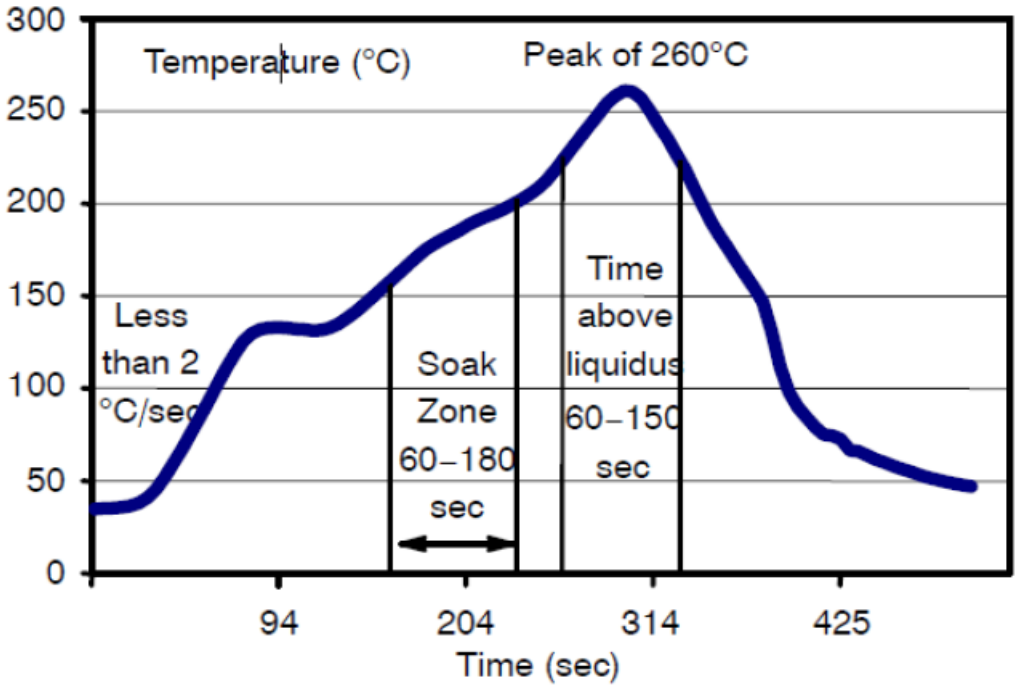
TRADE-OFFS

- What are the Trade-offs of a “Wettable Flank” Package?
- **Slightly increased manufacturing or cost complexity**: The process of cutting or shaping the lead-frame flank to expose the side, plus tin-plating the flank, is an additional manufacturing step. Some packages may cost more or be newer in the product lifecycle.
- **PCB footprint changes**: To fully benefit from the wettable flank, the PCB land pattern often needs adjustment (extended pad/land length, possibly stencil modifications) to allow solder paste and solder flow for side fillet formation. Designers must follow manufacturer guidance. For example, the Allegro article gives recommended land extensions.
- **Inspection of fillet height still matters**: While side fillets are present, the actual quality (height, continuity) of the fillet still must be inspected. For example, one standard mentions minimum toe-fillet height etc.
- **Higher risk if land/stencil is not adapted**: If you use a wettable flank package but use a standard land/stencil footprint, solder may not properly flow to the flank, reducing the benefit.
- **Need for updated assembly process**: Reflow parameters, solder paste choice, flux, board design, and inspection criteria may need tuning for wettable flank packages (e.g., longer land length, suitable solder volumes). For example, an IR reflow may peak at 245 °C.

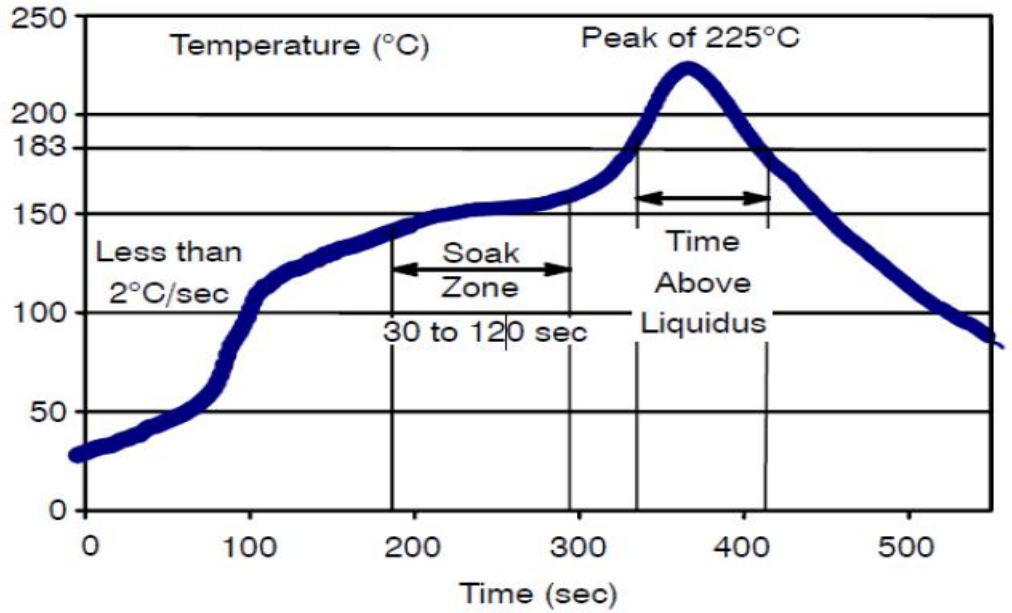
IR REFLOW PROFILES

- Not all packages leads contains the same metallurgy (i.e.-Tin, Copper, Lead, etc.)
- Lead Length as well as footprint sizing will affect the IR Reflow profile
- Wettable Flank IR profiles tend to peak slightly less, in between 225°C and 245°C, but extend further out in time
- Solder Content can also dictate over all reflow time

Typical Reflow Profile for Lead Free Solder:



Typical Reflow Profile for Eutectic Tin/ Lead Solder:



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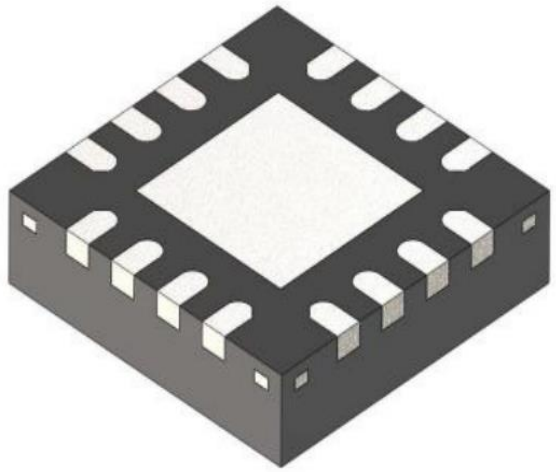
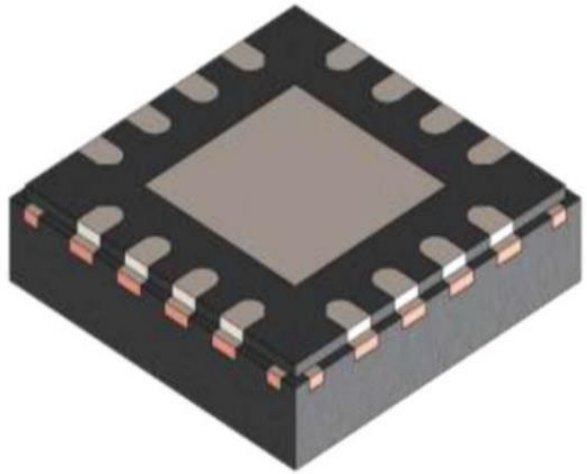
PACKAGING CONFIGURATIONS

- **Not all packages marketed as "Wettable Flank" are equal**: The term may cover various implementations (step-cut, dimple, different plating). Designers should review package drawings to ensure the feature is present and meets their inspection/assembly needs.

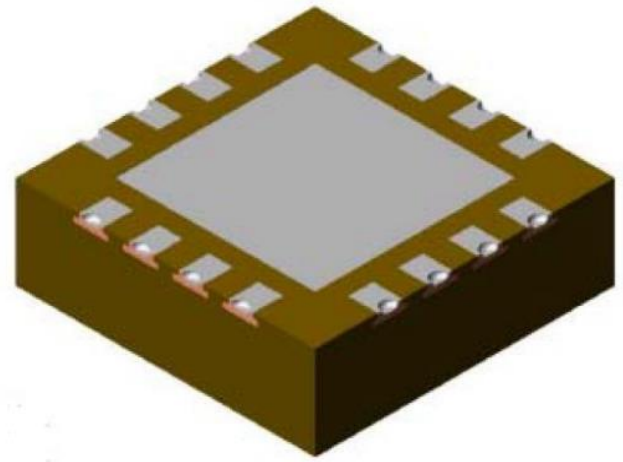
- Electro-less Plated Sn:



- Electro-Plated Sn Step-Cut:



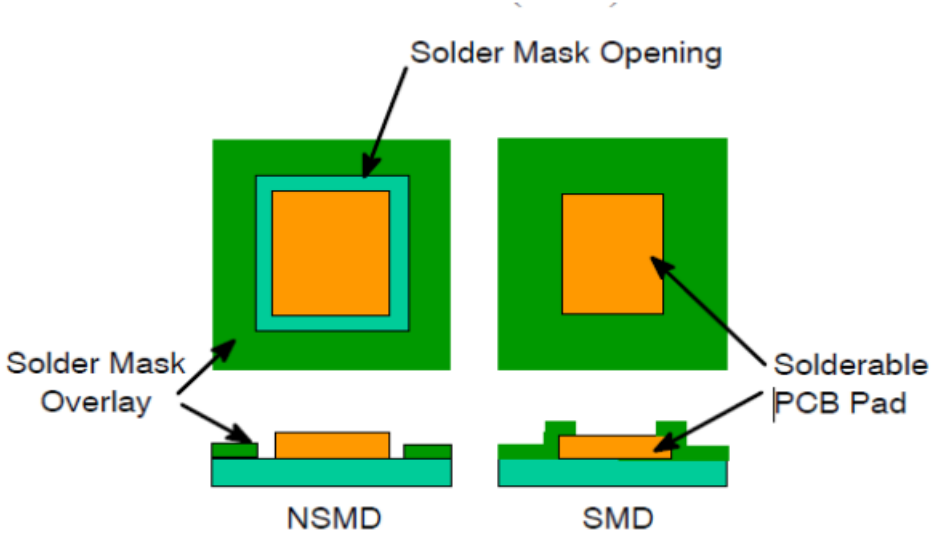
- Dimple Lead:



NSMD AND SMD PAD CONFIGURATIONS

- Two types of PCB solder mask opening commonly used for surface mount leadless style package are:
- 1. Non-Solder Masked Defined (NSMD)
  - Allows Solder Paste and Solder to Flow Around and on Top of Metallization
  - More Accurate Due to Tighter Tolerances of Copper Etching Process
- 2. Solder Masked Defined (SMD)
  - Restrict Solder Paste and Solder Flow
  - Harder to Control Tolerances
  - Less Visual Inspection
  - Creates a Concentration Point of Stress

    (Typically on Top of Metallization)

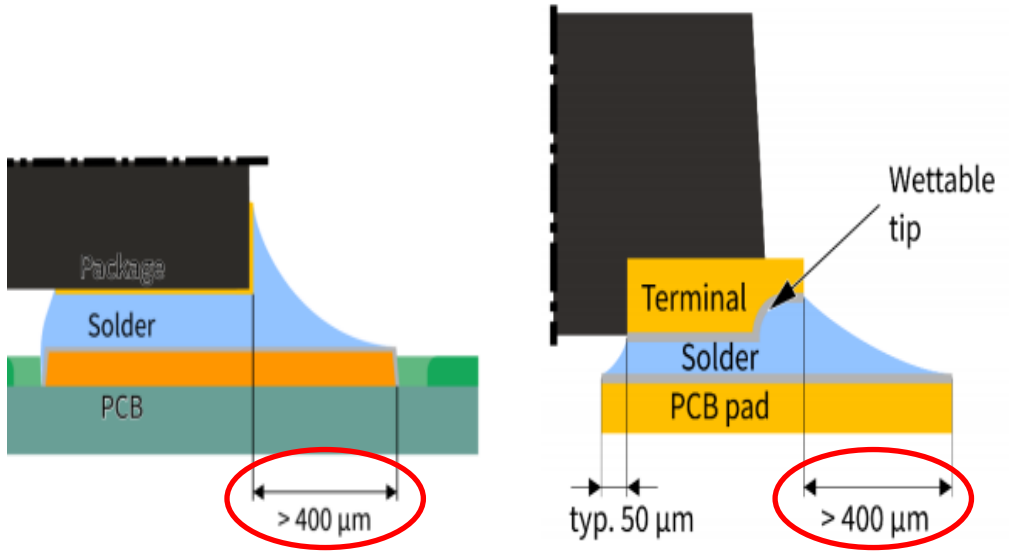


Summary: NSMD is the preferred Methodology when defining Footprints

LAYOUT PAD DESIGN

Pad Design for LTI Features

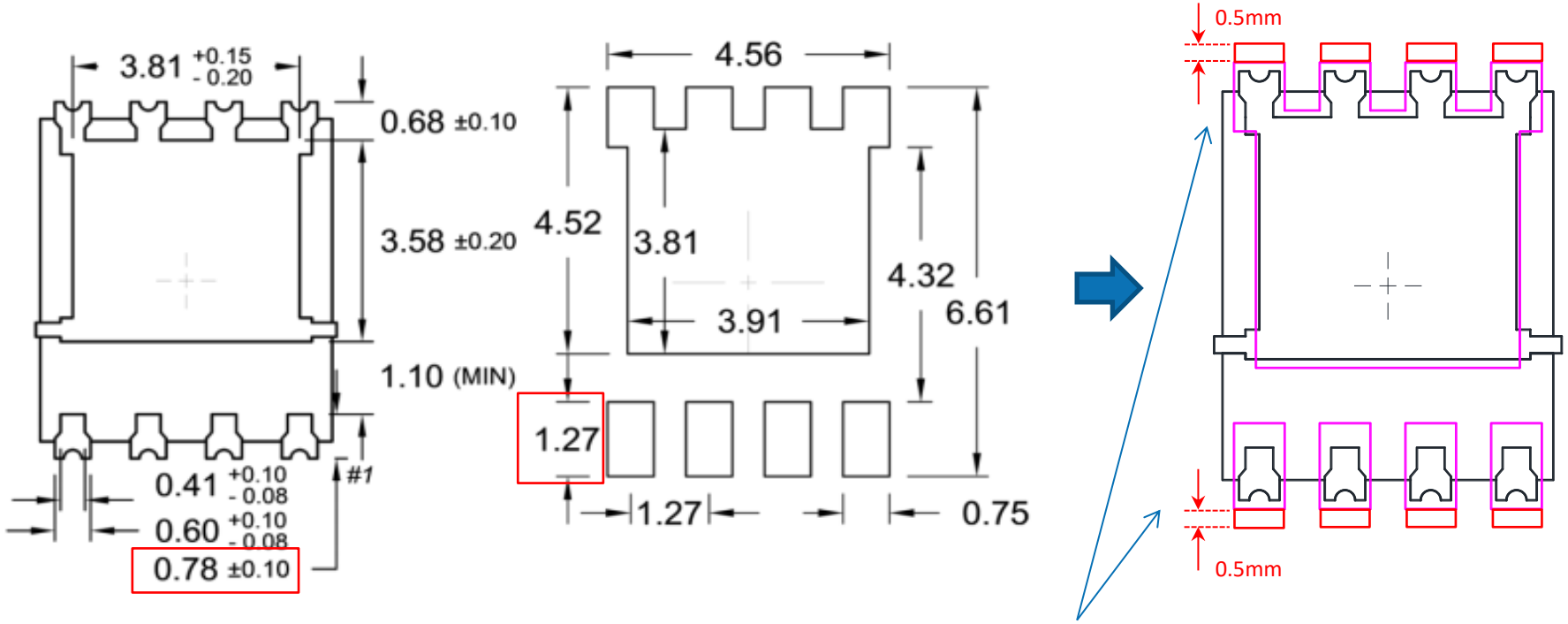
To ensure an optimal response during the AOI, the PCB pad should protrude the package outline by minimum 400µm. The solder paste volume should be accordingly increased by a sufficient amount to ensure a homogeneous and reproducible solder joint fillet formation at the termination tip.



Reference: Infineon, Recommendations for Board Assembly of Infineon Thin Small Discrete Packages without Leads

WETTABLE FLANK FOOTPRINT

- Layout footprint – PDFN56U



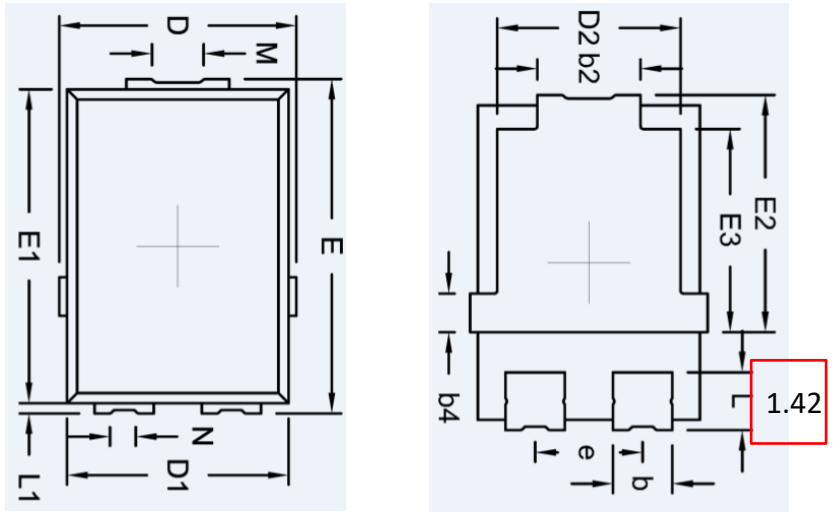
The footprint extend from 1.27mm to 1.77mm.

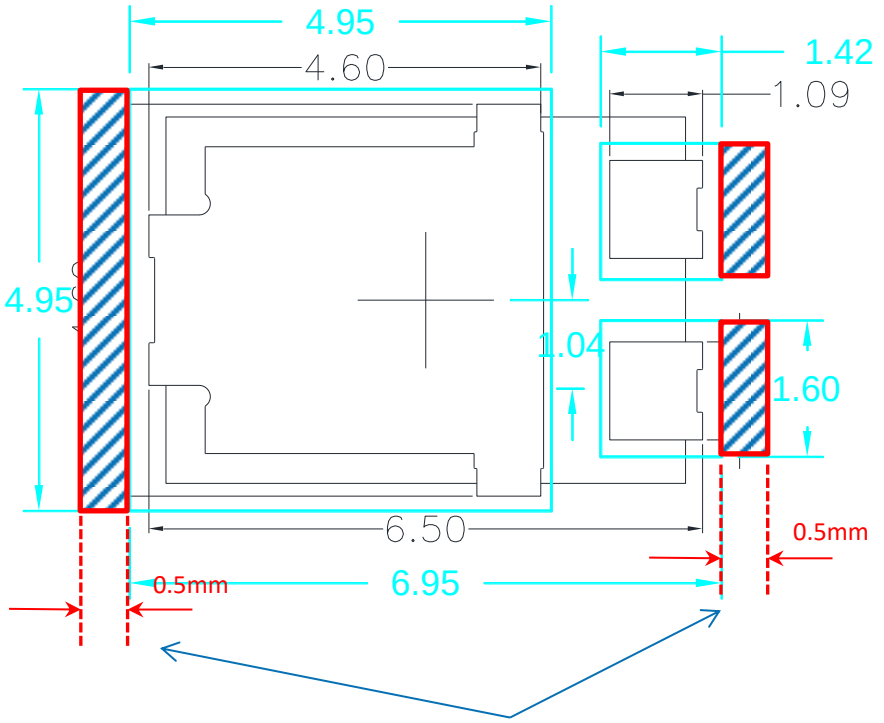
Footprint length condition

1. 1.27mm
2. 1.77mm

WETTABLE FLANK FOOTPRINT

- Layout footprint – SMPC4.6U





Footprint length condition

1. 1.42mm
2. 1.92mm

The footprint extend from 1.42mm to 1.92mm.

FOOTPRINT COMPATABILITY ON ALL CAD TOOLS

Footprint

Choose format to download:

- Altium
- Circuit Studio
- CR-8000/5000 (Beta)
- DesignSpark PCB
- DipTrace
- EAGLE
- Easy-PC (Beta)
- eCADSTAR (Beta)

Footprint

- ExpressPCB Plus
- Autodesk Fusion
- KiCad (pre V4)
- KiCad (V4 and later)
- KiCad (V6 and later)
- OrCAD / Allegro v17
- OrCAD / Allegro v16
- PADS / DxDesigner
- P-CAD

Footprint

- PADS / DxDesigner
- P-CAD
- PCB123
- Proteus 8.9 and later
- Pulsonix
- TARGET 3001!

- Place Part
- Add to Library

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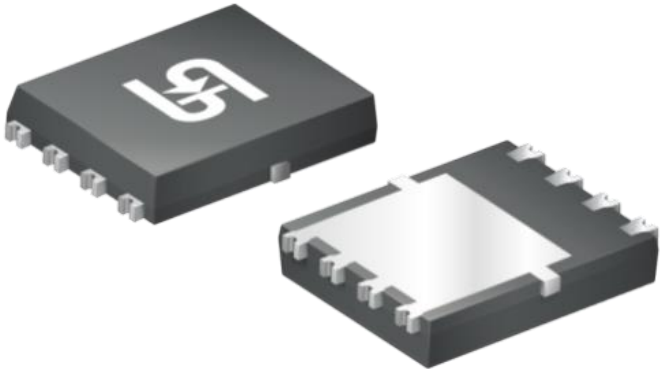
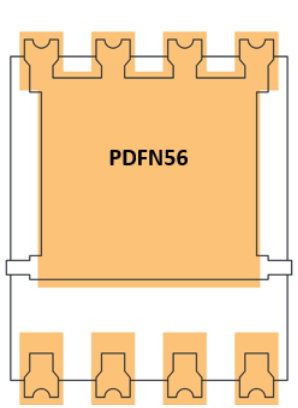
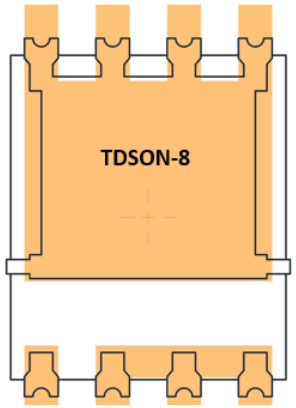
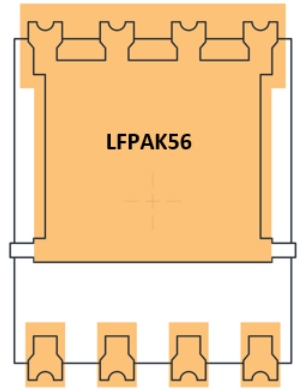
PDFN56U - WETTABLE FLANK FOOTPRINT COMPATIBILITY

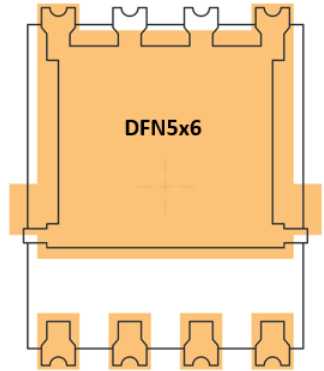
TSC PDFN56U package overlay on competitor land pad



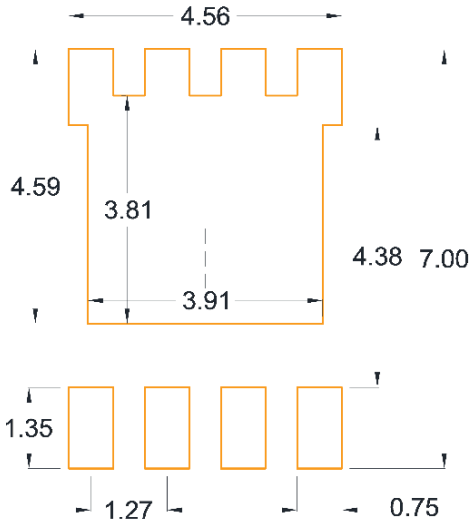


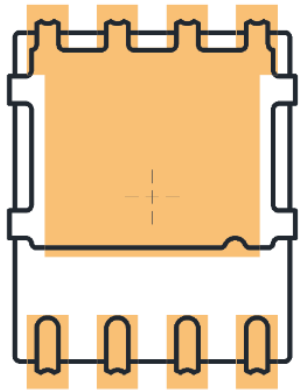




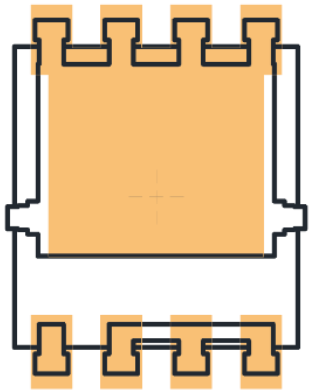


Competitor package overlay on TSC PDFN56U land pad

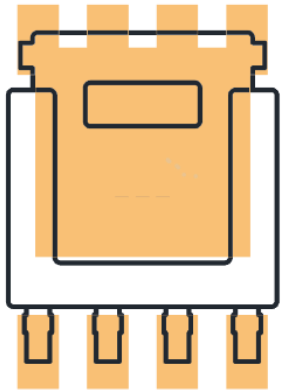




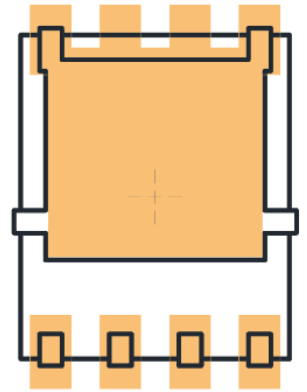
PowerFLAT56



TDSON-8



LFPAK56

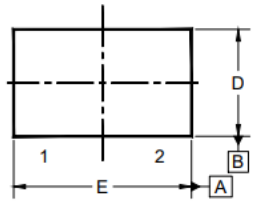


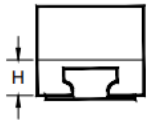
DFN5x6

NOTE: FOOT-PRINT LAYOUTS ARE LIMITED TO WETTABLE PARTS ONLY

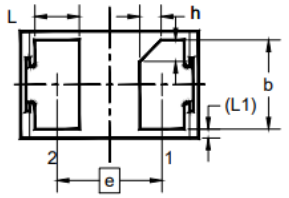
TAIWAN SEMICONDUCTOR

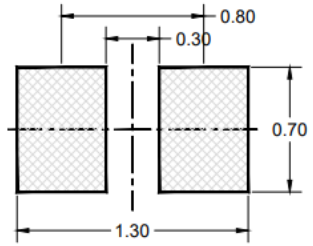
DFN1006-2LW POD Summary and Comparison



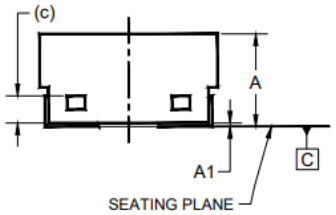


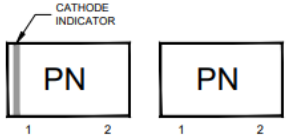
DIM	Unit (mm)	
	Min	Max
A	0.45	0.55
A1	0.00	0.05
b	0.45	0.55
c	0.152 REF	
D	0.55	0.65
E	0.95	1.05
e	0.59 BSC	
L	0.20	0.30
L1	0.05 REF	
H	0.10	---
h	0.07	0.15





SUGGESTED PAD LAYOUT





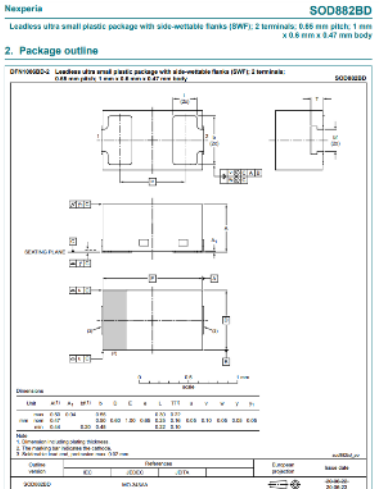
MARKING DIAGRAM

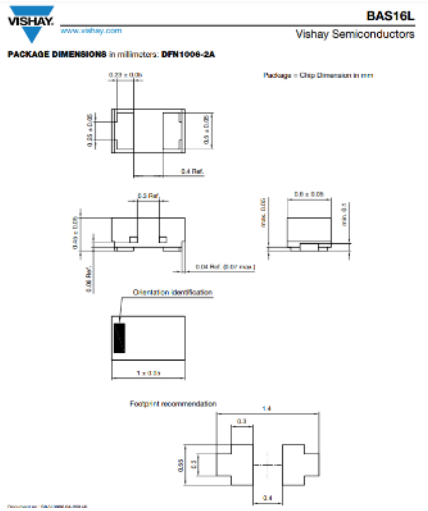
P/N = DEVICE CODE

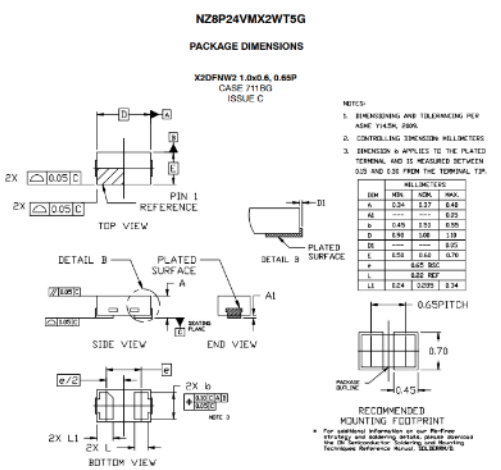
NOTES: UNLESS OTHERWISE SPECIFIED

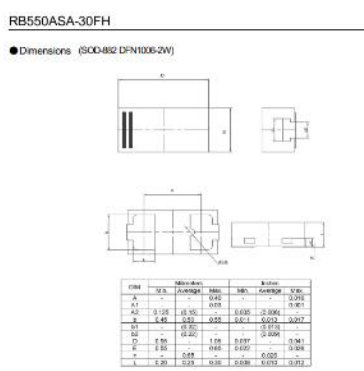
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. SUGGESTED PAD LAYOUT IS FOR REFEF PURPOSE ONLY.
4. DWG NO. REF: HQ2SD07-DFN1006_2LW-1

	Nexperia (1006)		Vishay (1006)		Onsemi (1006)		ROHM (1006)		TSC (1006)	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
A	0.44	0.50	0.40	0.50	0.34	0.40	--	0.40	0.45	0.55
A1	--	0.04			--	0.05	--	0.03	0.00	0.05
b	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55
c							0.125		0.152 BSC	
D	0.6		0.55	0.65	0.50	0.70	0.55	0.65	0.55	0.65
E	1.00		0.95	1.05	0.90	1.10	0.95	1.05	0.95	1.05
e	0.65		~0.63		0.65 BSC		0.65 BSC		0.59 BSC	
L	0.22	0.30	0.18	0.28	0.22 REF		0.20	0.30	0.20	0.30
L1									0.05 REF	
H	0.10	0.22	0.10	--					0.10	--
h									0.07	0.15





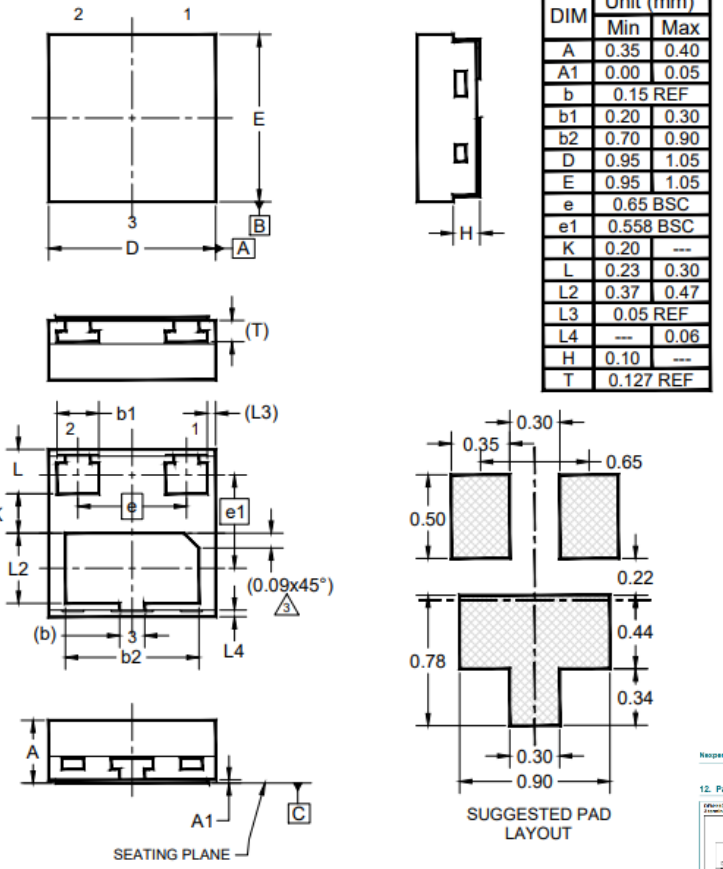




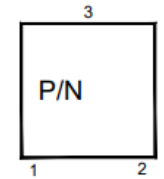
POD AND PAD LAYOUT COMPARABLE

TAIWAN SEMICONDUCTOR

DFN1010-3LW POD Summary and Comparison



DIM	Unit (mm)	
	Min	Max
A	0.35	0.40
A1	0.00	0.05
b	0.15 REF	
b1	0.20	0.30
b2	0.70	0.90
D	0.95	1.05
E	0.95	1.05
e	0.65 BSC	
e1	0.558 BSC	
K	0.20	---
L	0.23	0.30
L2	0.37	0.47
L3	0.05 REF	
L4	---	0.06
H	0.10	---
T	0.127 REF	



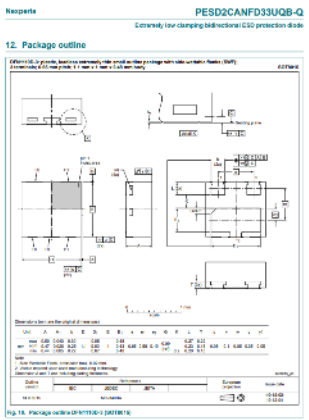
MARKING DIAGRAM

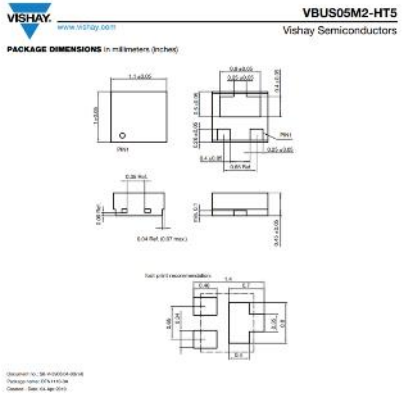
P/N = DEVICE CODE

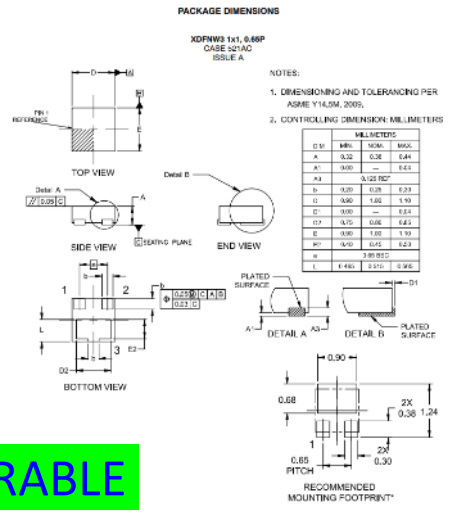
NOTES: UNLESS OTHERWISE SPECIFIED

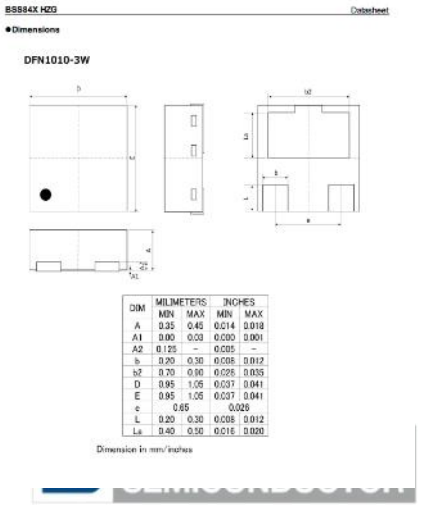
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. LARGE TERMINAL PAD WITH CHAMFER CORNER IS A COMMON ANODE TERMINAL.
4. PACKAGE OUTLINE REFERENCE: JEDEC MO-340BA.
5. DWG NO. REF: HQ2SD07-DFN1010_3LW-124

	Nexperia (1110)		Vishay (1110)		Onsemi (1010)		ROHM (1010)		TSC (1010)	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
A	0.44	0.50	0.40	0.50	0.32	0.44	0.35	0.45	0.35	0.40
A1	0.01	0.04			0.00	0.04	0.00	0.03	0.00	0.05
b			0.20	0.30	0.20	0.30			0.15 REF	
b1	0.22	0.30	0.20	0.30	0.20	0.30	0.20	0.30	0.20	0.30
b2	0.87	0.95	0.75	0.85	0.75	0.85	0.70	0.90	0.70	0.90
D	1.10		1.05	1.15	0.90	1.10	0.95	1.05	0.95	1.05
E	1.00		0.95	1.05	0.90	1.10	0.95	1.05	0.95	1.05
e	0.65 BSC		0.65 BSC		0.65 BSC		0.65 BSC		0.65 BSC	
e1	0.58 BSC								0.558 BSC	
K	0.20	--							0.20	--
L	0.20	0.27	0.21	0.31	0.20	0.30	0.20	0.30	0.23	0.30
L2	0.40	0.48	0.35	0.45	0.40	0.50	0.40	0.50	0.37	0.47
L3									0.05 REF	
H									0.20	--
T	0.10	0.22	0.10	--					0.127 REF	









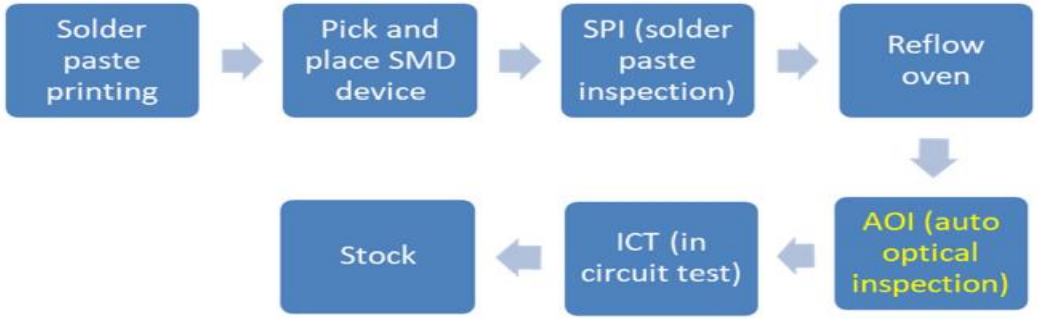
POD AND PAD LAYOUT COMPARABLE

SUMMARY OF KEY SPECIFICATIONS

- **“Wettable Flank” or “Wettable-Flank QFN/DFN”**: Indicates the side plating/flank design.
- **Step cut dimension / step width or step height**
- **Plating material**: The flank should be plated in solderable finish (e.g., tin) so solder can wet to the side.
- **Footprint land extension recommendation**: The application note often gives specific pad-length extension or stencil recommendation.
- **Solder paste / reflow profile**: Ensure process compatibility (lead-free, etc). e.g., reflow peak typical-230°C, max-260°C
- **Inspection criteria / fillet height / side-fillet width.** Alternative is costly XRAY inspections.
- **Reliability qualification / automotive grade / AEC-Q100**
- **Board land pattern & stencil design**
- **Footprint compatibility / backward compatibility**

AOI APPLY IN SMT BACKGROUND

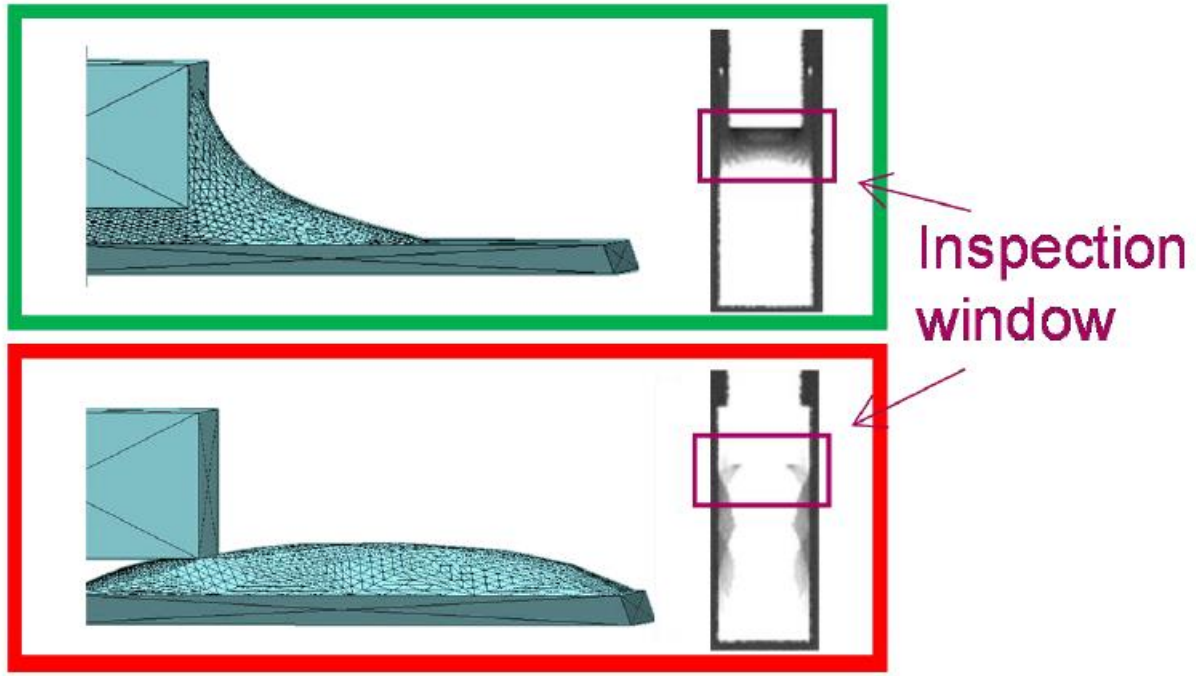
- SMT (Surface mount technology) of assembly device on PCB had become popular now. Among SMT process procedure (Figure below), AOI (Auto Optical Inspection) is important that make sure device pin solder joint soldering well that guarantee soldering reliability.



Before 2005 year, most factories rely on human visual inspection to check device solder joint status. However human visual inspection exists subjectivism, there is no objective criteria caused by different human examination occur different result. On the contrary AOI (Auto Optical Inspection) adopt digital photographic process to compare the difference and judge the result, the judgement tolerance could be control to smaller level. AOI could contribute repetitive and faster SMT solder joint examination than human visual inspection, so most factories adopt AOI to examine device solder joint status in the present day.

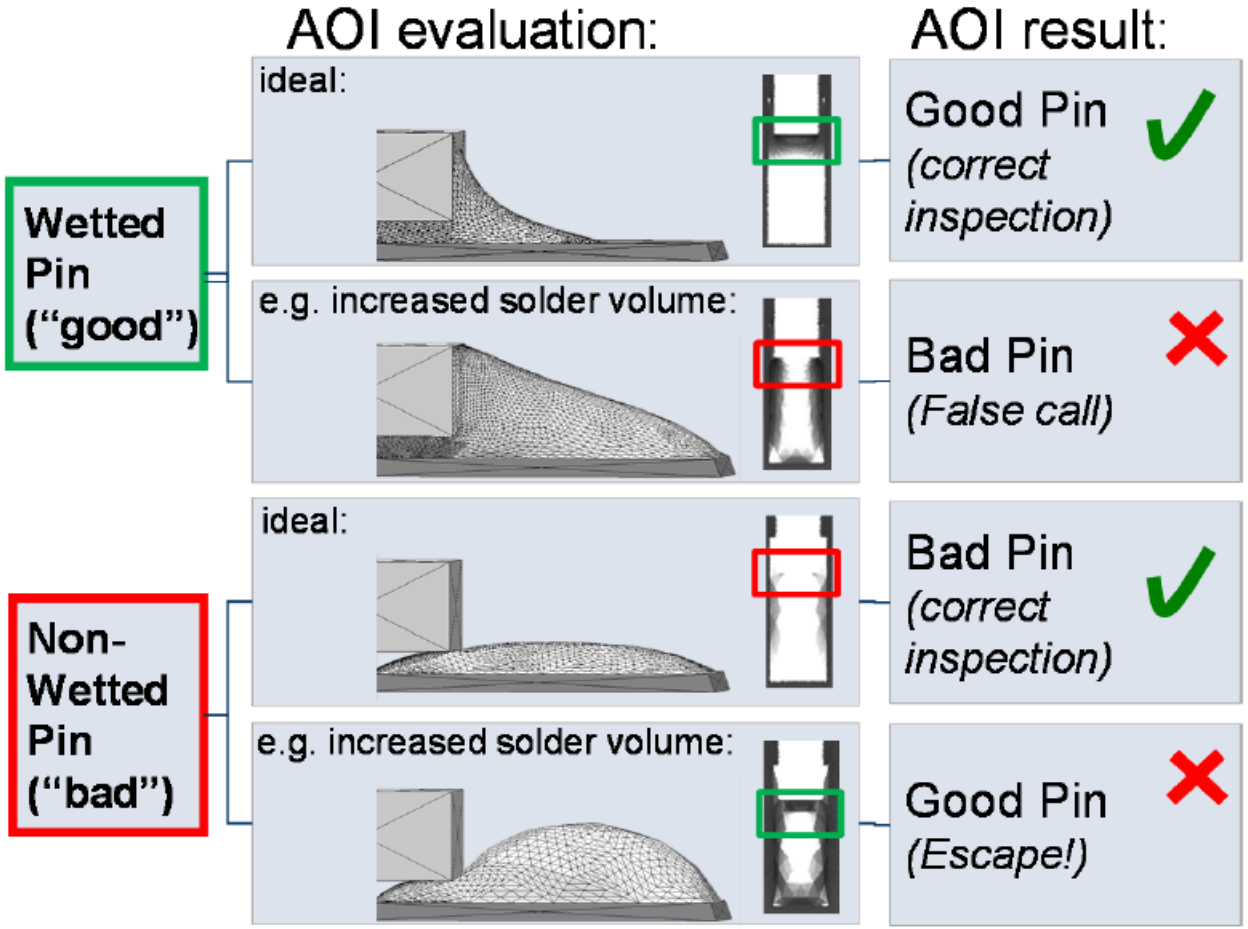
AOI PASS-FAIL JUDGMENT

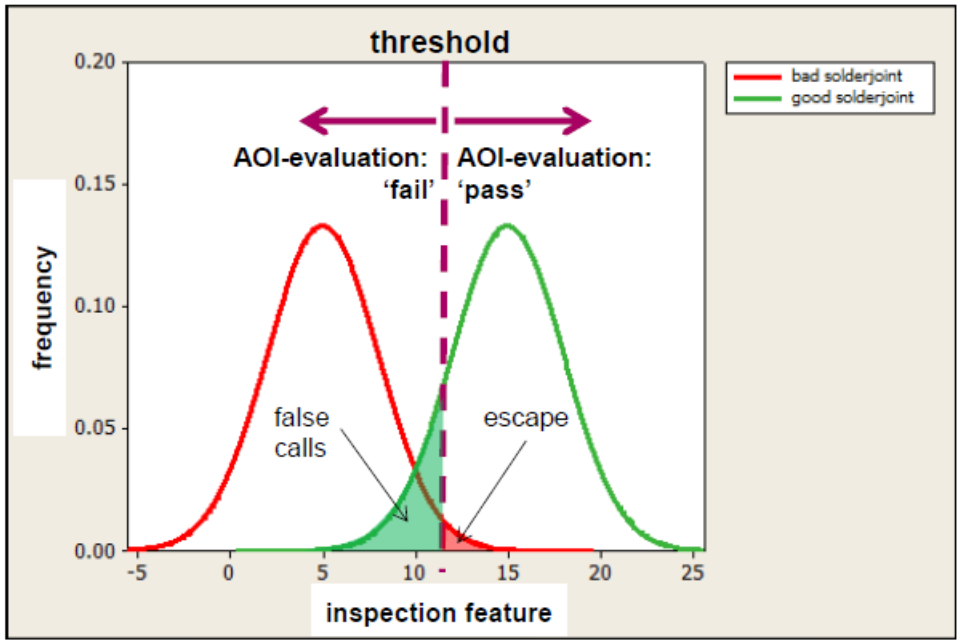
Automatic optical inspection (AOI) of solder joint is a standard post reflow soldering inspection method to check assemblies failures. It is common to systems that an optical gray or color image of a solder joint, recorded with a CCD camera system under different conditions of illumination and be viewed from different directions is subjected to an image analysis procedure which quantifies image features as color, gray images, and gradients. These feature images can then be compared against certain threshold values to arrive at a pass and fail classification for a device solder joint.



AOI PASS-FAIL JUDGMENT

False “Pass” judgments do occur but remain very low in mass production. To keep false “Pass judgements to a minimum it recommended to use a Tin soldering.

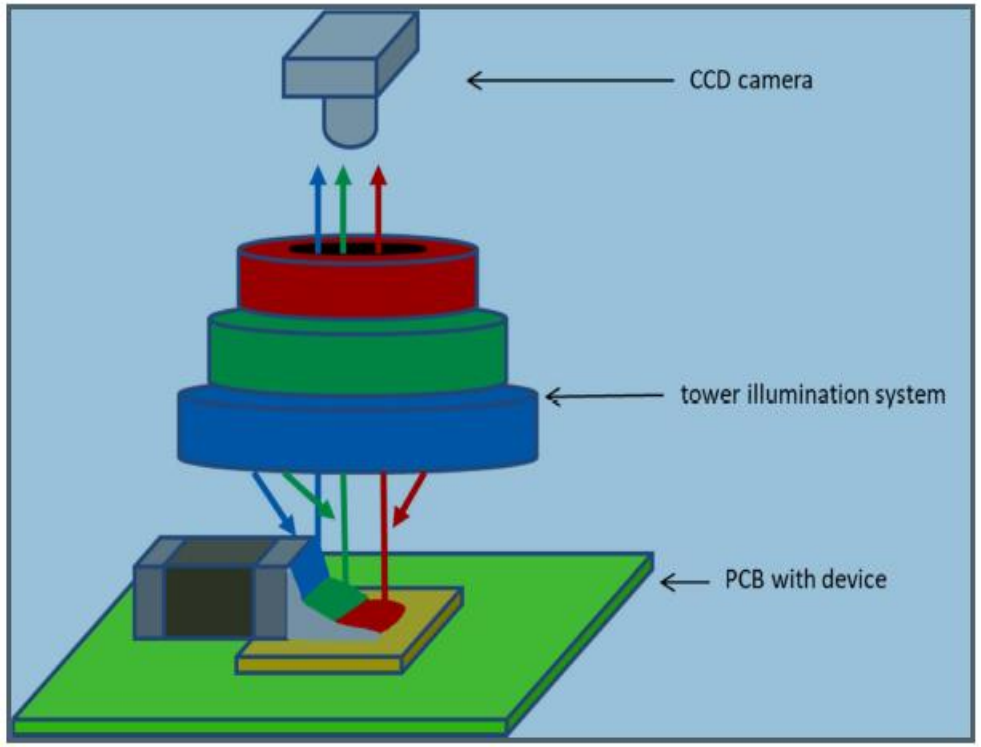




TAIWAN SEMICONDUCTOR

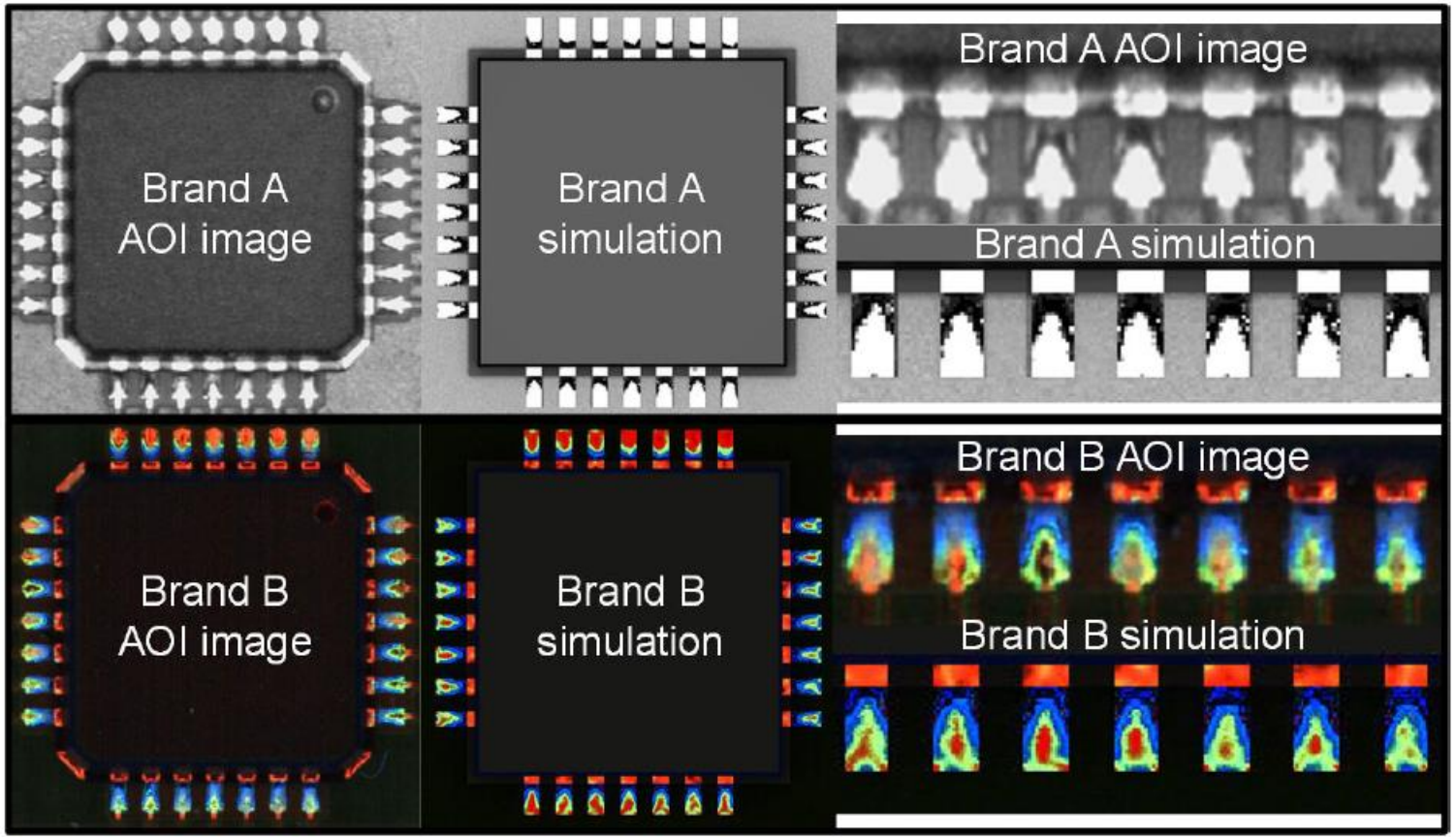
AOI BASIC THEORY

- Modern AOI systems use a tower illumination to illuminate the device at a full 360 degrees (Red, Green, Blue in figure below)
- High resolution CCD camera quickly acquires pictures of reflected light signals
- Software analyzes and compares the data and makes a judgement if the solder joint complies with standards

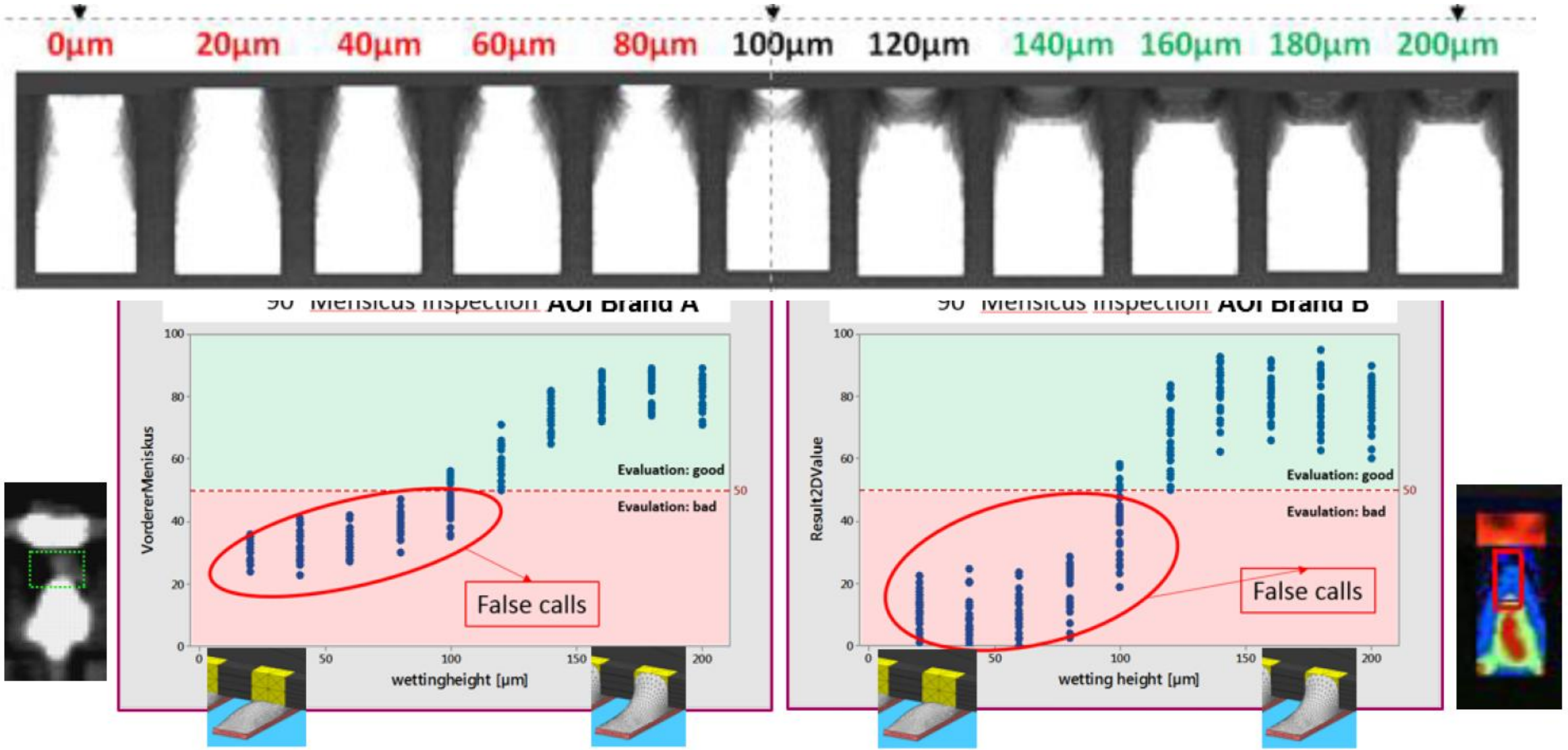


AOI BASIC THEORY

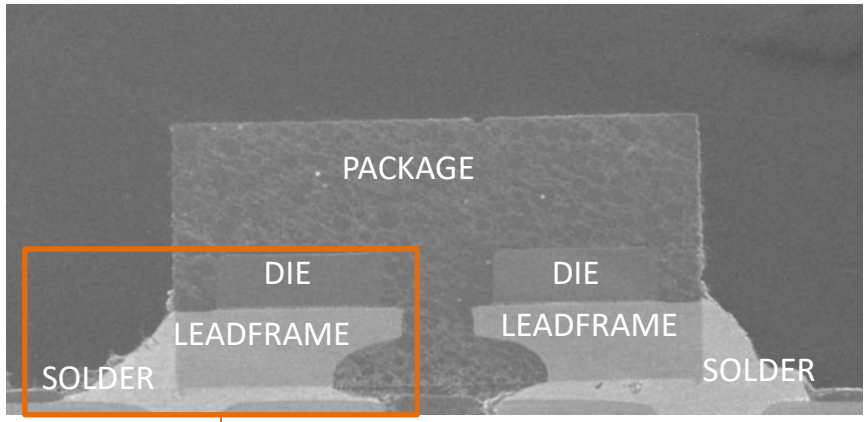
- Software analyzes and compares the data and makes a judgement if the solder joint complies with standards
- Gray-scale, color illumination and simulation can be combined to have a high degree of accuracy



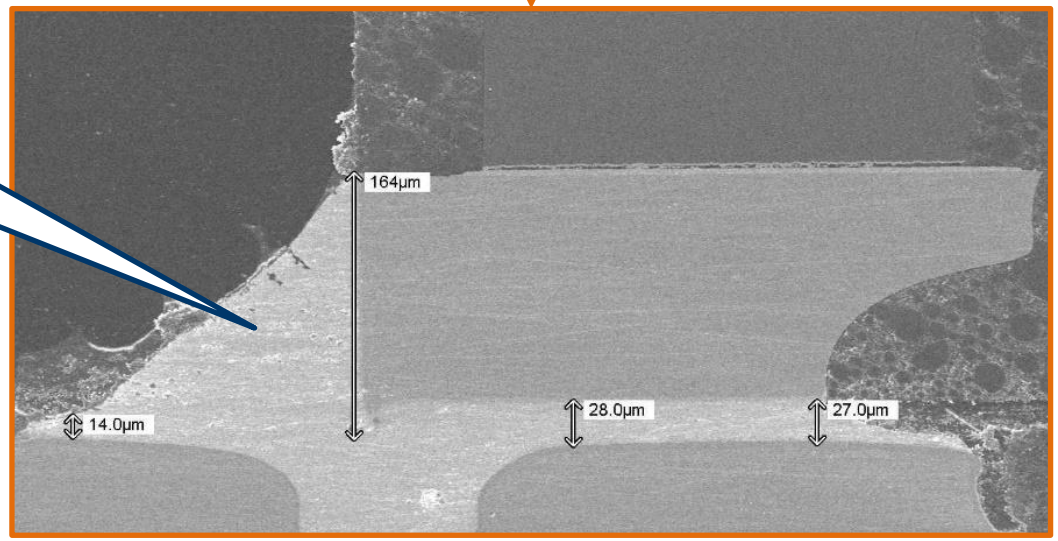
SIDE WALL SOLDER HEIGHT MEASUREMENT



SIDE WALL SOLDER HEIGHT MEASUREMENT

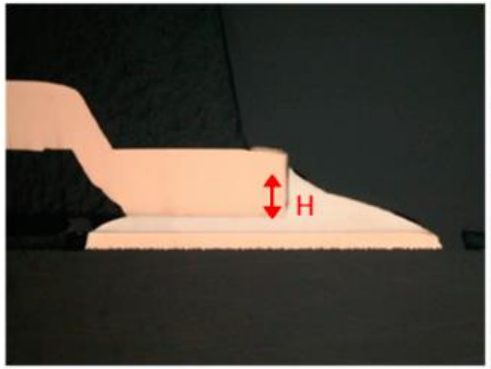
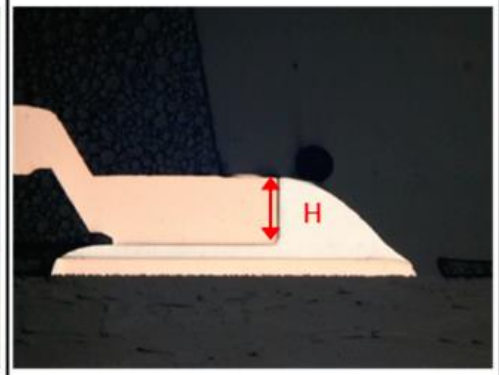
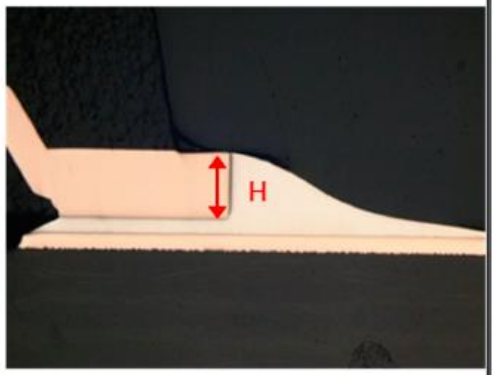


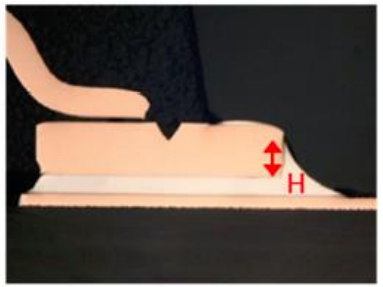
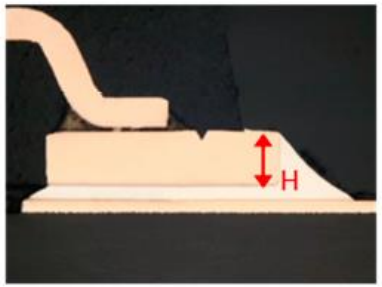
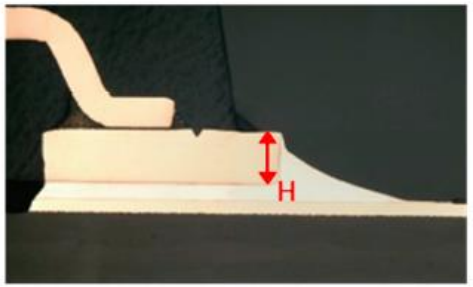
Solder fillet height >100um



TAIWAN SEMICONDUCTOR

INCREASED SOLDER COVERAGE

Package	PDFN56	PDFN56U	PDFN56U
footprint pin length	1.27mm	1.27mm	1.77mm
pin solder cross section			

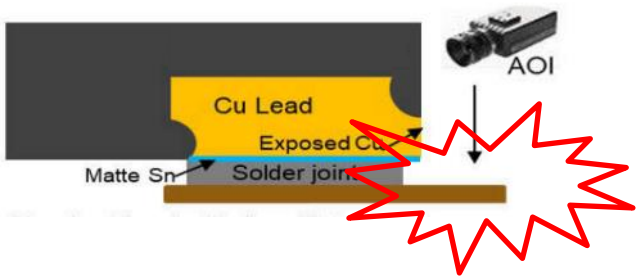
Package	SMPC4.6U	SMPC4.6U	SMPC4.6U
footprint pin length	1.42mm	1.42mm	1.92mm
pin solder cross section			

Challenges of DFN (Dual Flat No-Lead) Packages

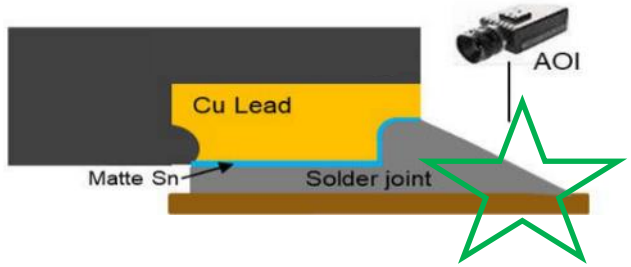
INDUSTRALIZATION 4.0

Intelligent factories requires Automated Optical Inspection (AOI) to check for the solder joints.

Non - Wettable

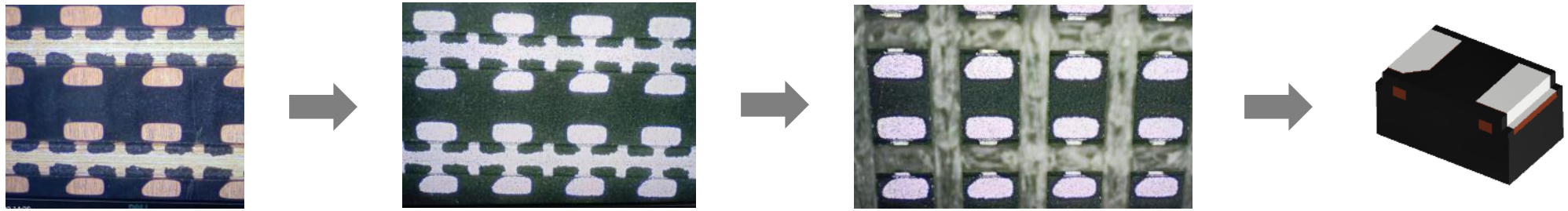


Side Wettable



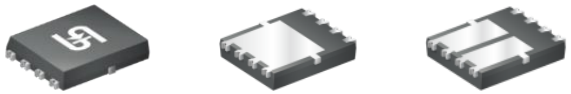
WETTABLE FLANK BACKEND PROCESS FLOW:

SAW → DA → WB → MOLD → 1st CUT → PLATING → 2nd CUT → TEST

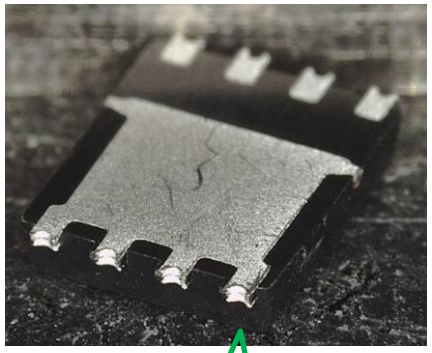


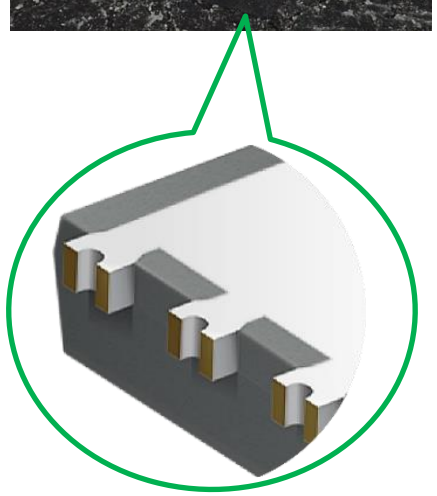
PDFN56U - WETTABLE FLANK PACKAGE

PDFN56U is TSC developed automotive package which is compatible with popular 5mm x 6mm SMT packages. PDFN56U offers both single and dual chips configuration. Wettable Flank Leads of PDFN56U improve accuracy of AOI and solder joint quality.

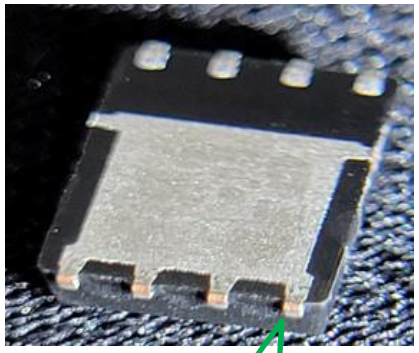


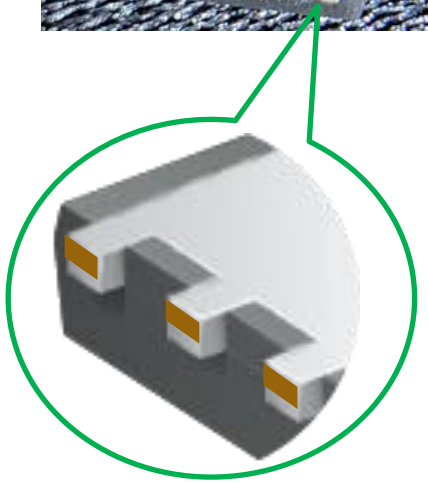
PDFN56U



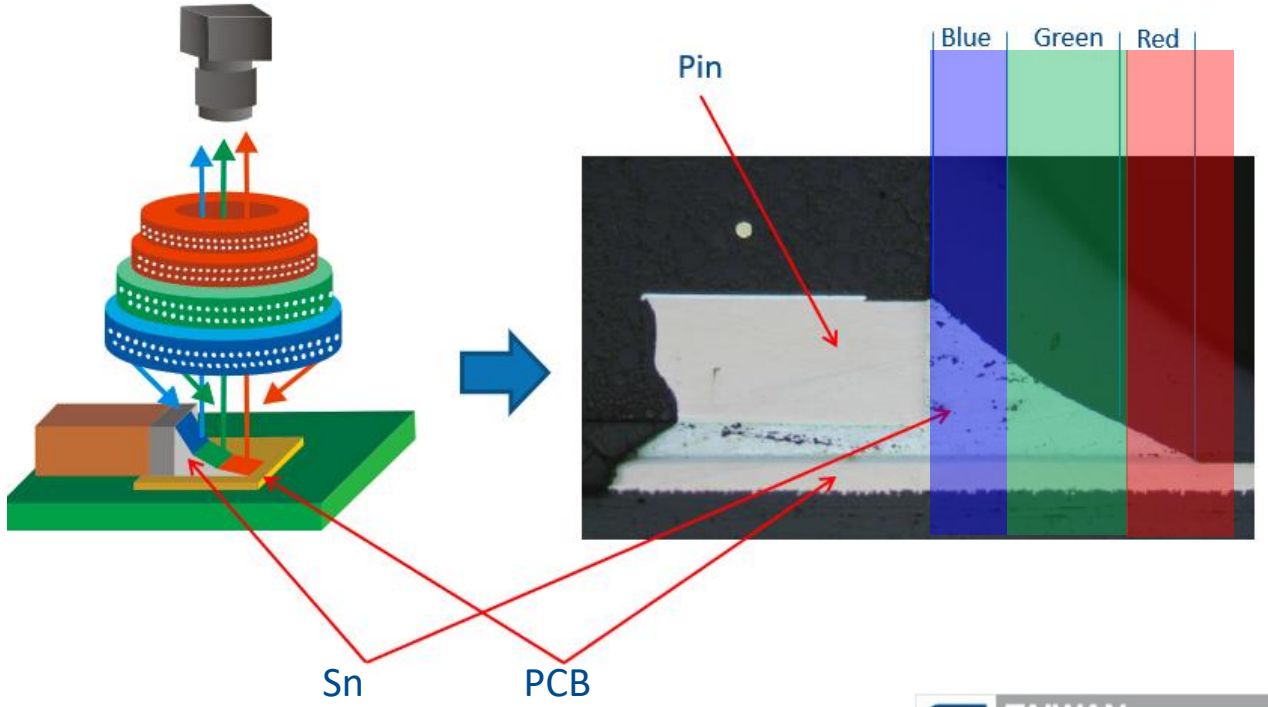


PDFN56





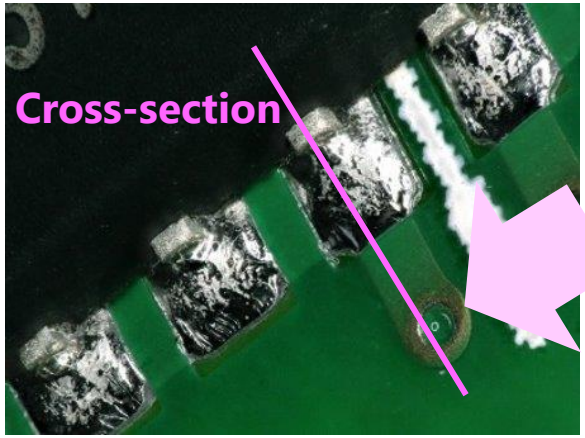
PDFN56U's EMC has better reliability performance with high Tg, low stress and low water absorption EMC properties.



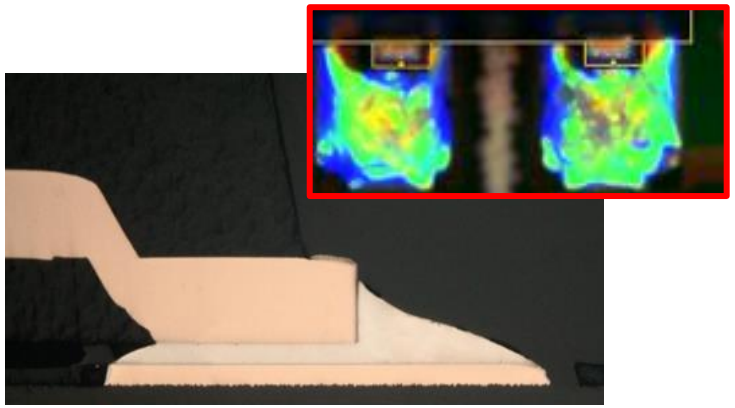
TAIWAN SEMICONDUCTOR

PDFN56U - WETTABLE FLANK PACKAGE

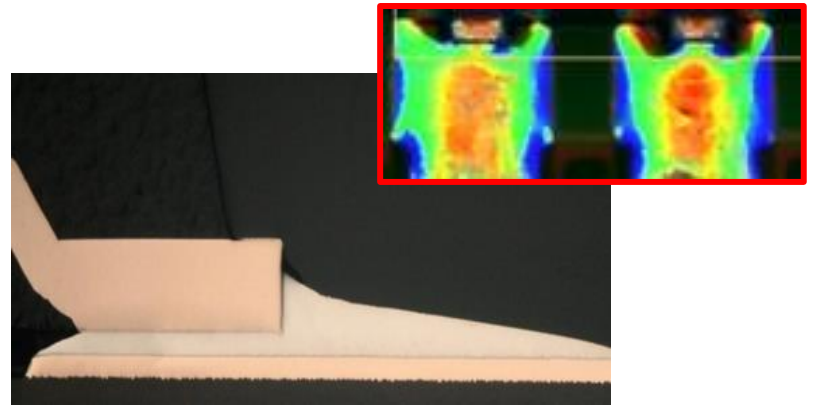
taiwansemi.com/AN-1009_Wettable_flank_packages_AOI_choice.pdf



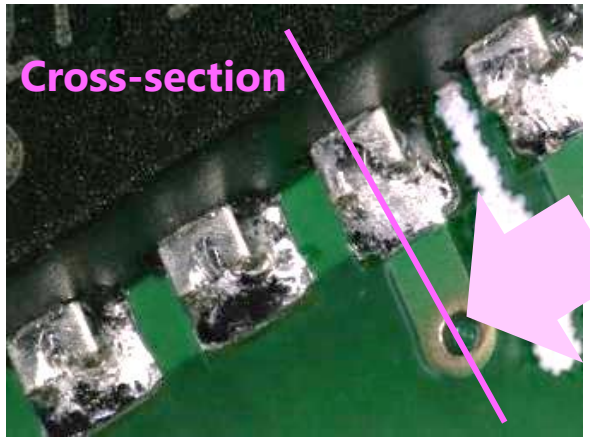
PDFN56 Leads



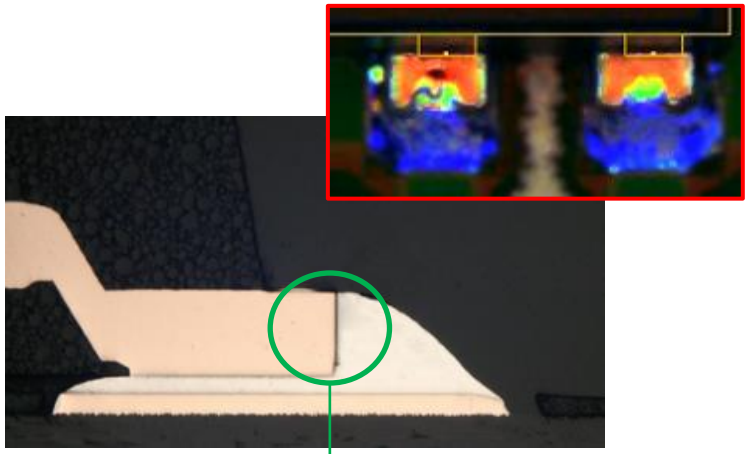
Recommended footprint length

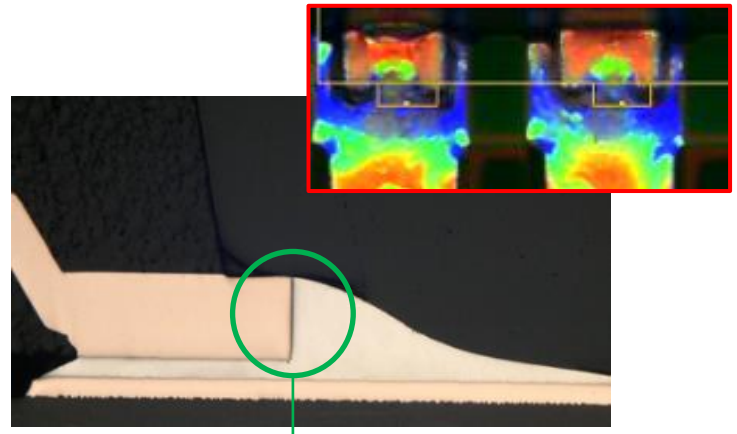


Extended footprint length.



PDFN56U Leads





Better solder coverage

TAIWAN SEMICONDUCTOR

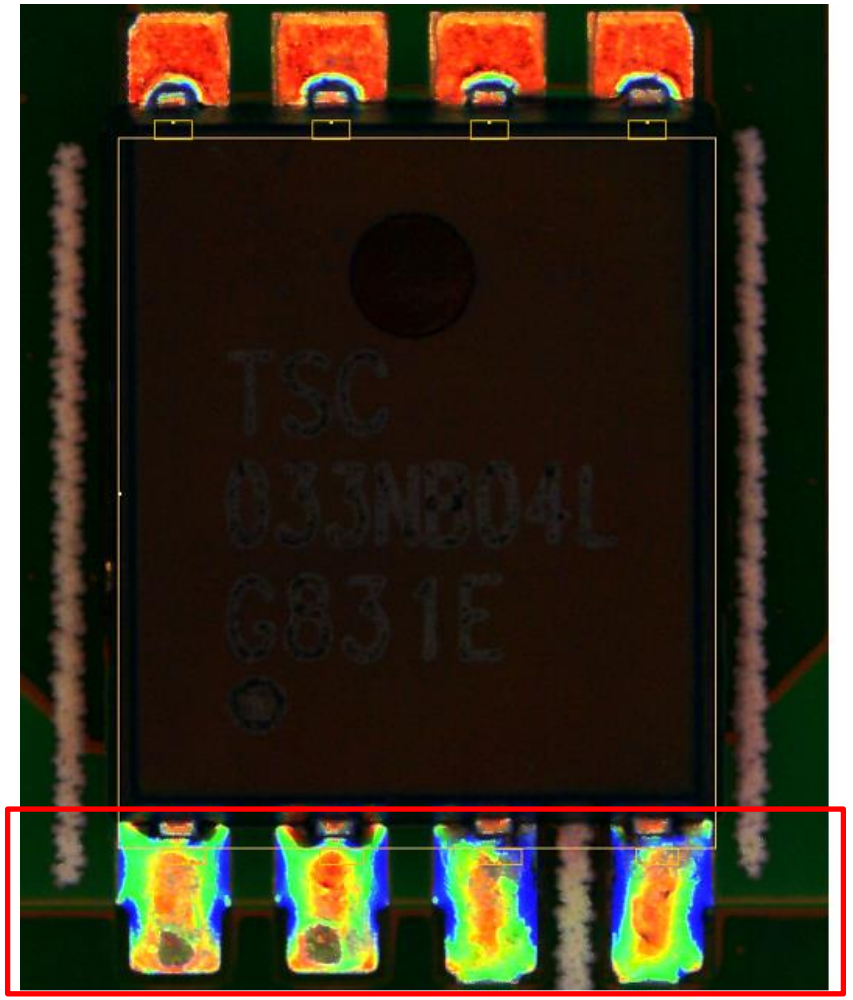
WETTABLE FLANK (AOI)

1.27mm 100% PDFN56

1.27mm 100% PDFN56U

WETTABLE FLANK (AOI)

1.77mm 100% PDFN56

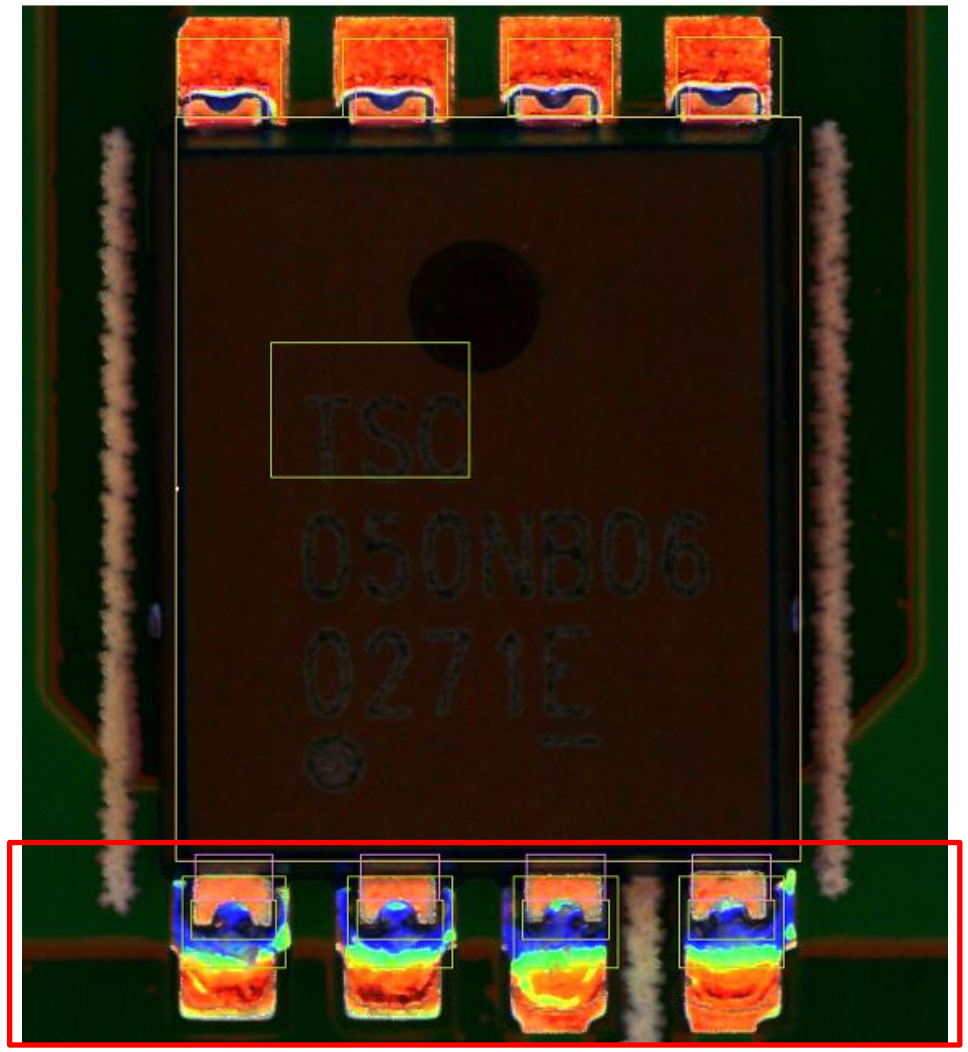


1.77mm 100% PDFN56U

WETTABLE FLANK (AOI)

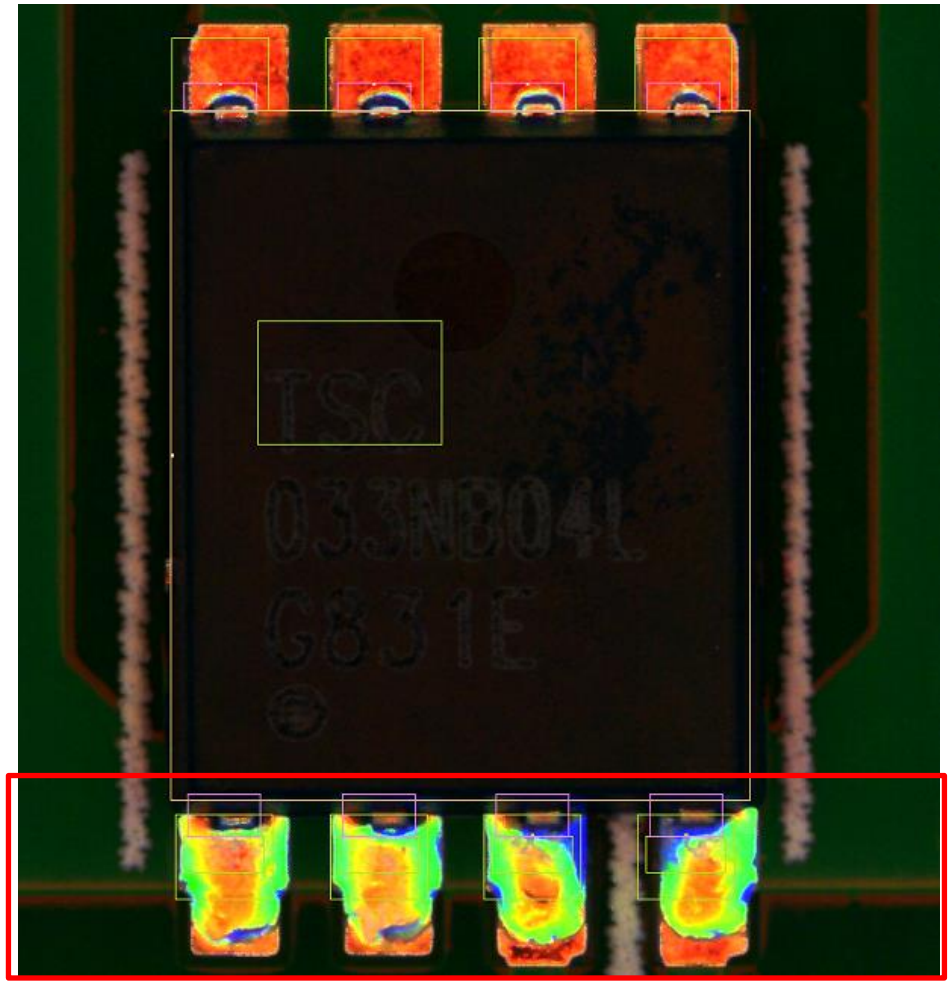
1.77mm 70% PDFN56

1.77mm 70% PDFN56U

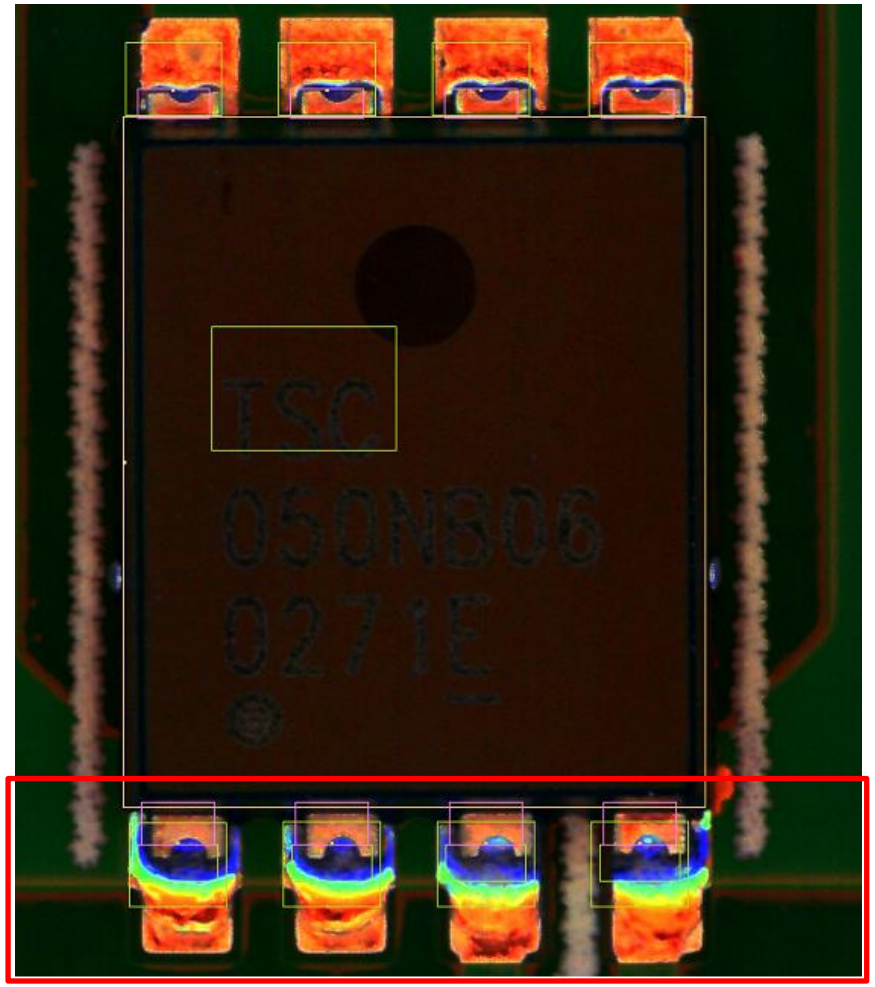


WETTABLE FLANK (AOI)

1.77mm 50% PDFN56

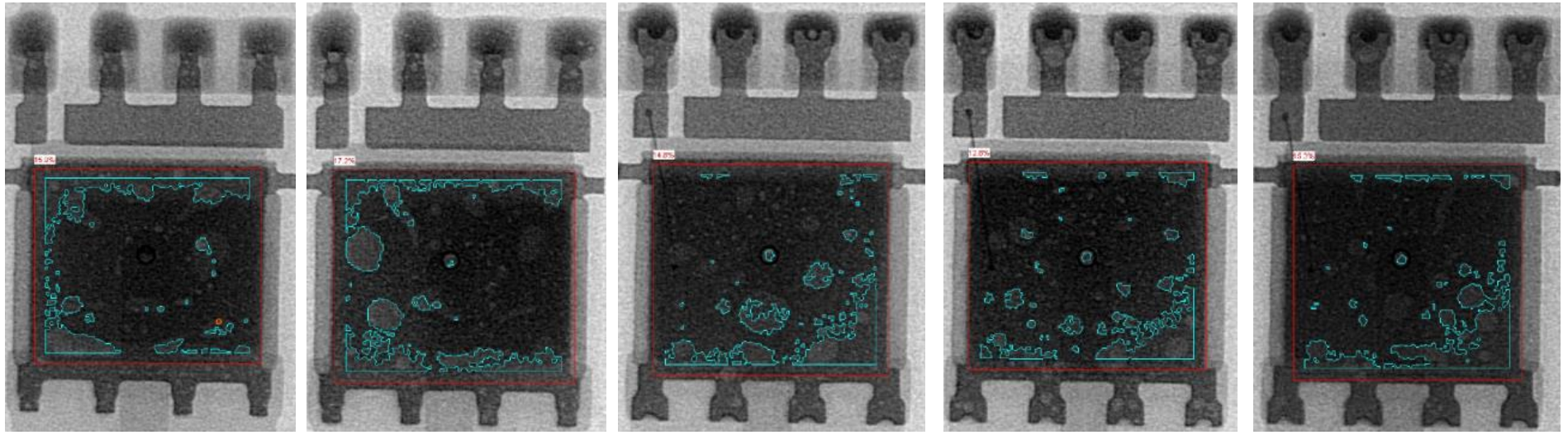


1.77mm 50% PDFN56U



WETTABLE FLANK (X-RAY) – PDFN56 & PDFN56U

IPC-A-610 industry standard requires the total area ratio to be less 25%, and most companies design their PCB and manufacturing processes to maintain less than a 15% ~ 25% solder void ratio.



Solder Void : 15.9%

Solder Void : 17.2%

Solder Void : 14.8%

Solder Void : 12.8%

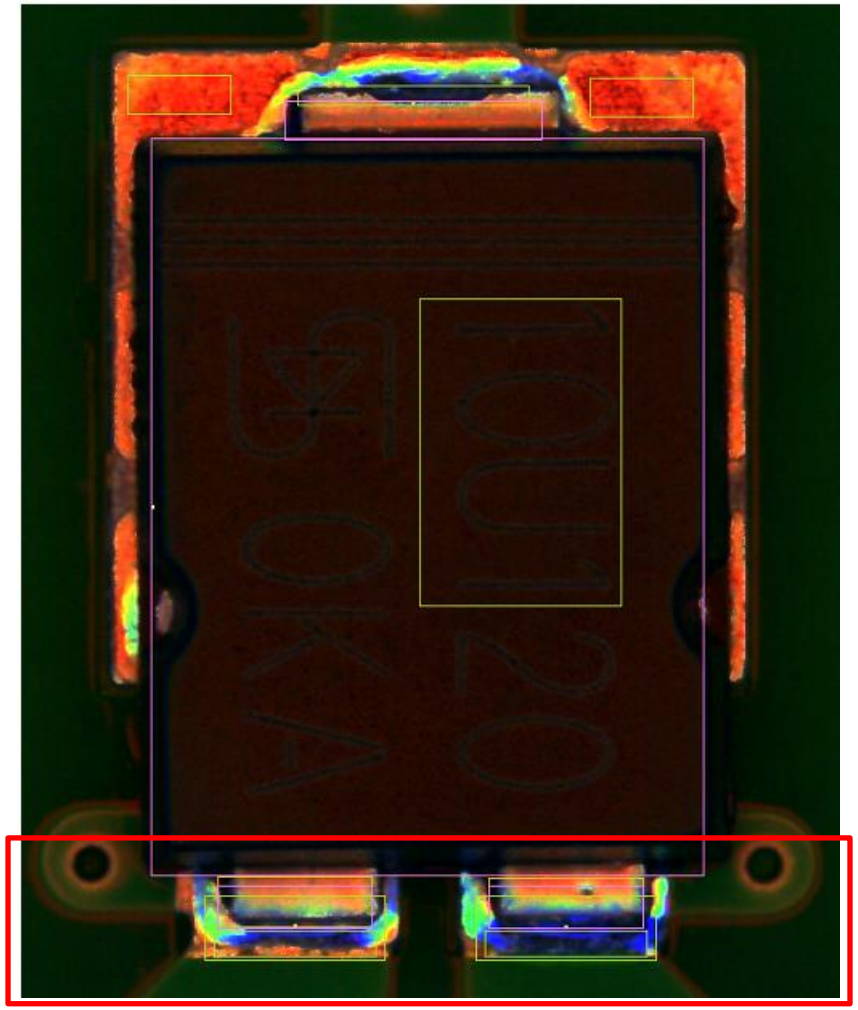
Solder Void : 15.3%

WETTABLE FLANK

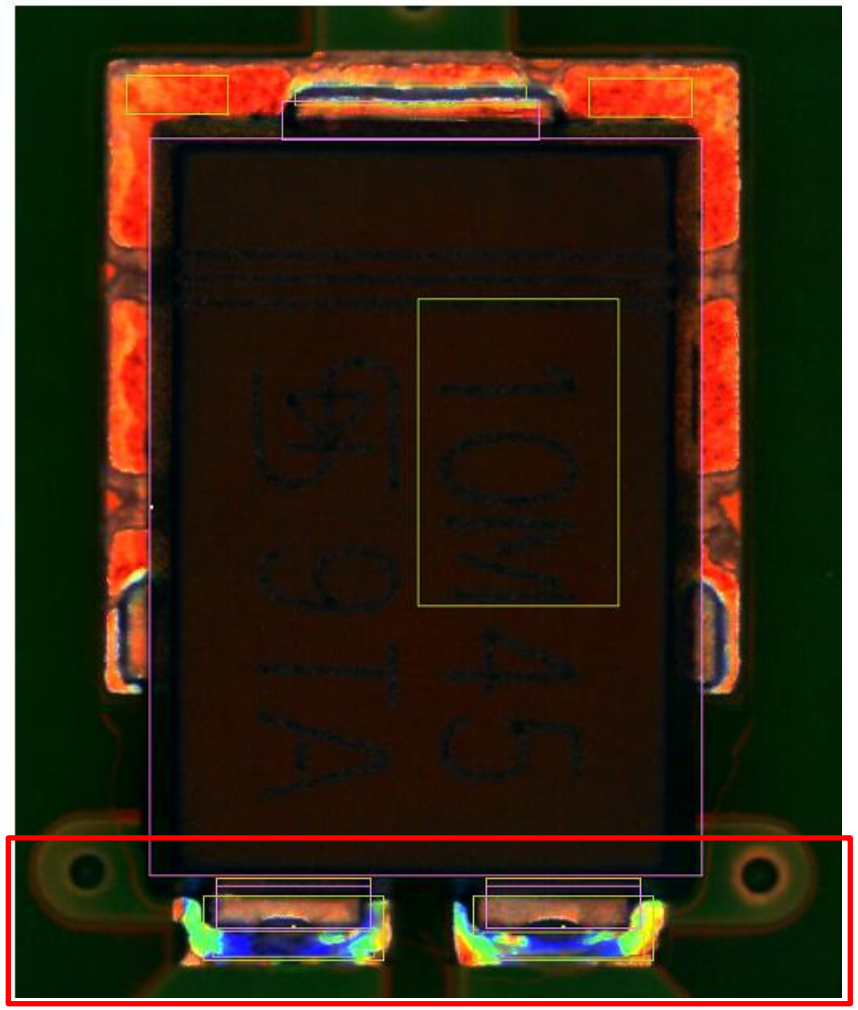
SMPC4.6 / SMPC4.6U

WETTABLE FLANK (AOI)

1.42mm 100% SMPC4.6

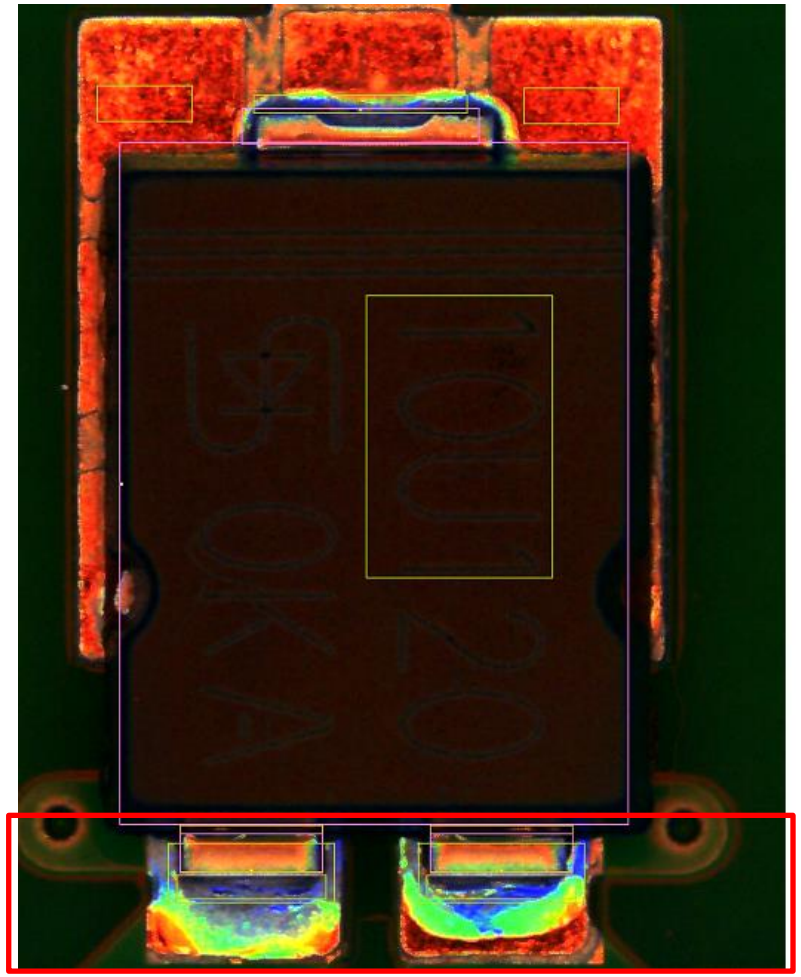


1.42mm 100% SMPC4.6U

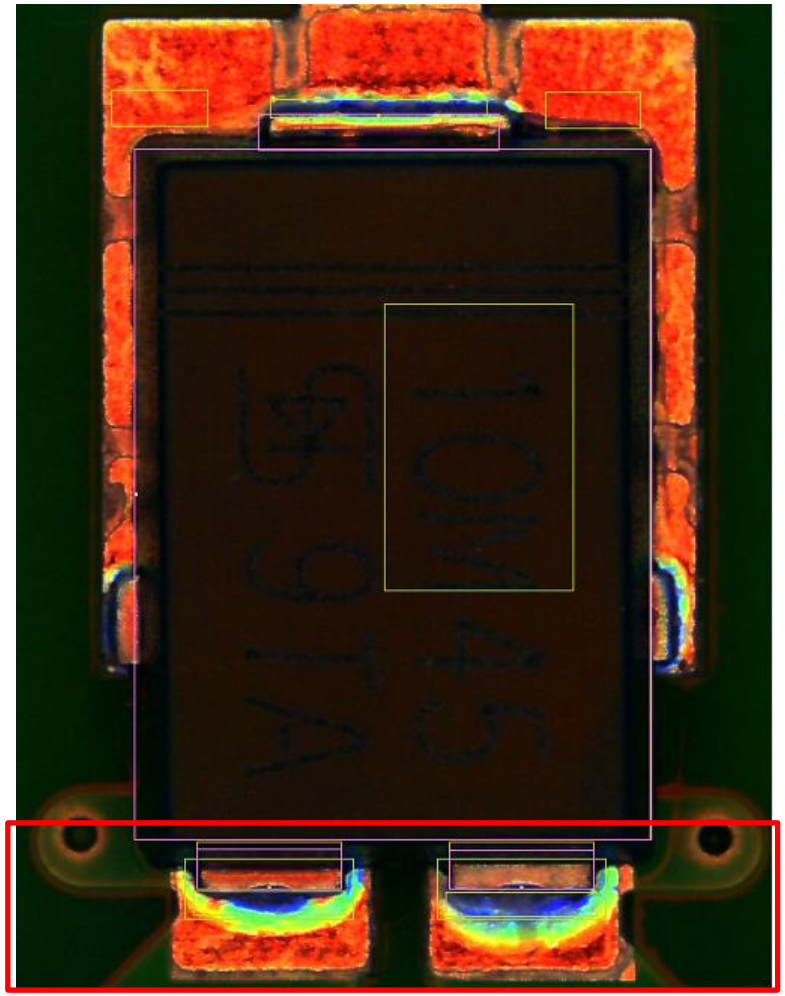


WETTABLE FLANK (AOI)

1.92mm 100% SMPC4.6

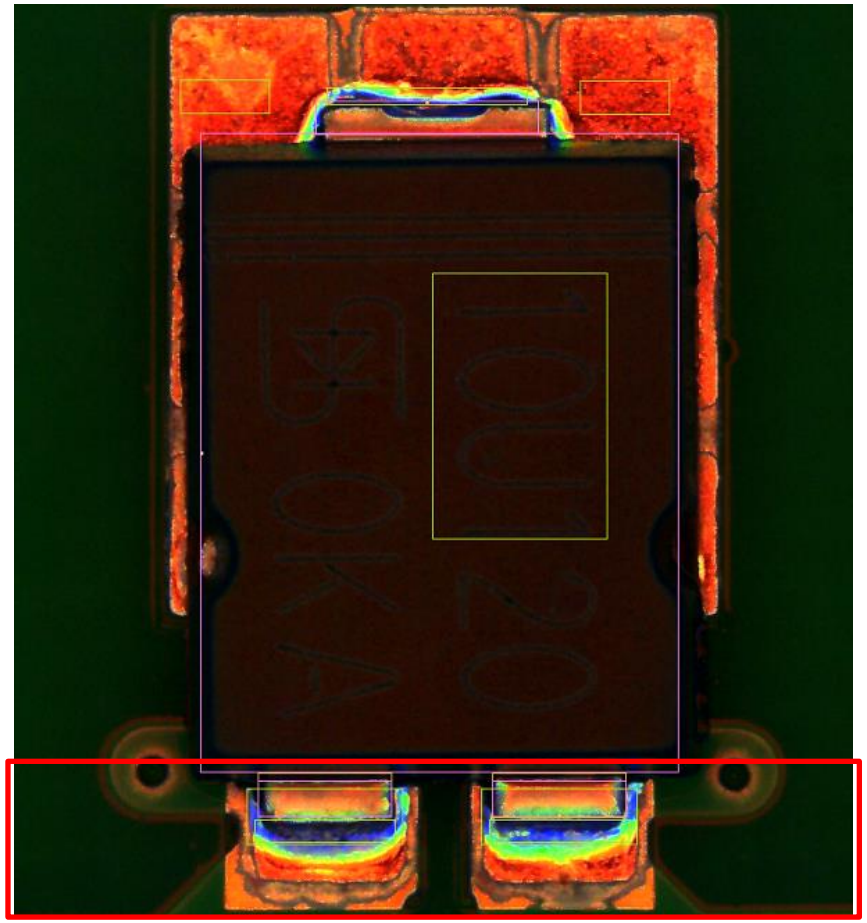


1.92mm 100% SMPC4.6U

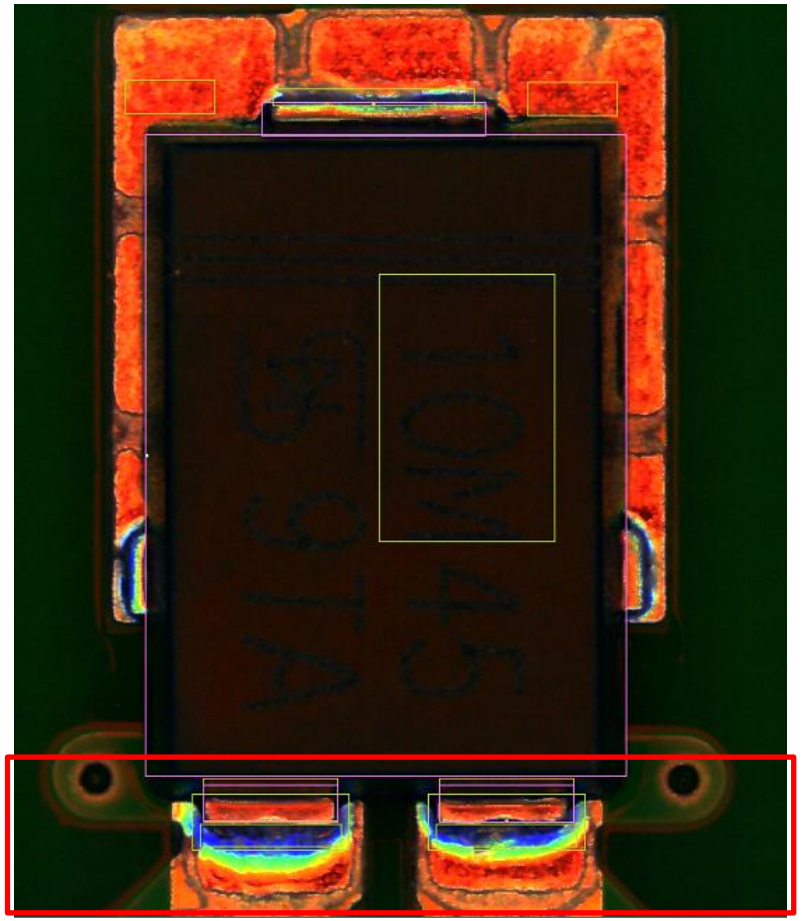


WETTABLE FLANK (AOI)

1.92mm 70% SMPC4.6

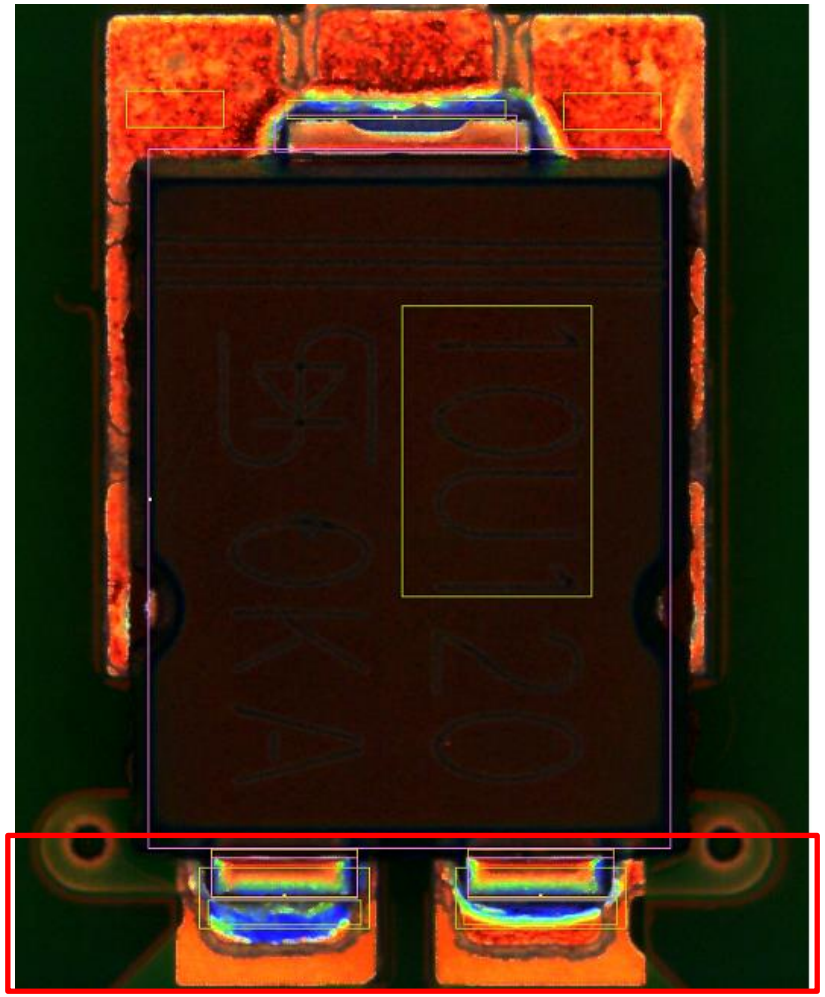


1.92mm 70% SMPC4.6U

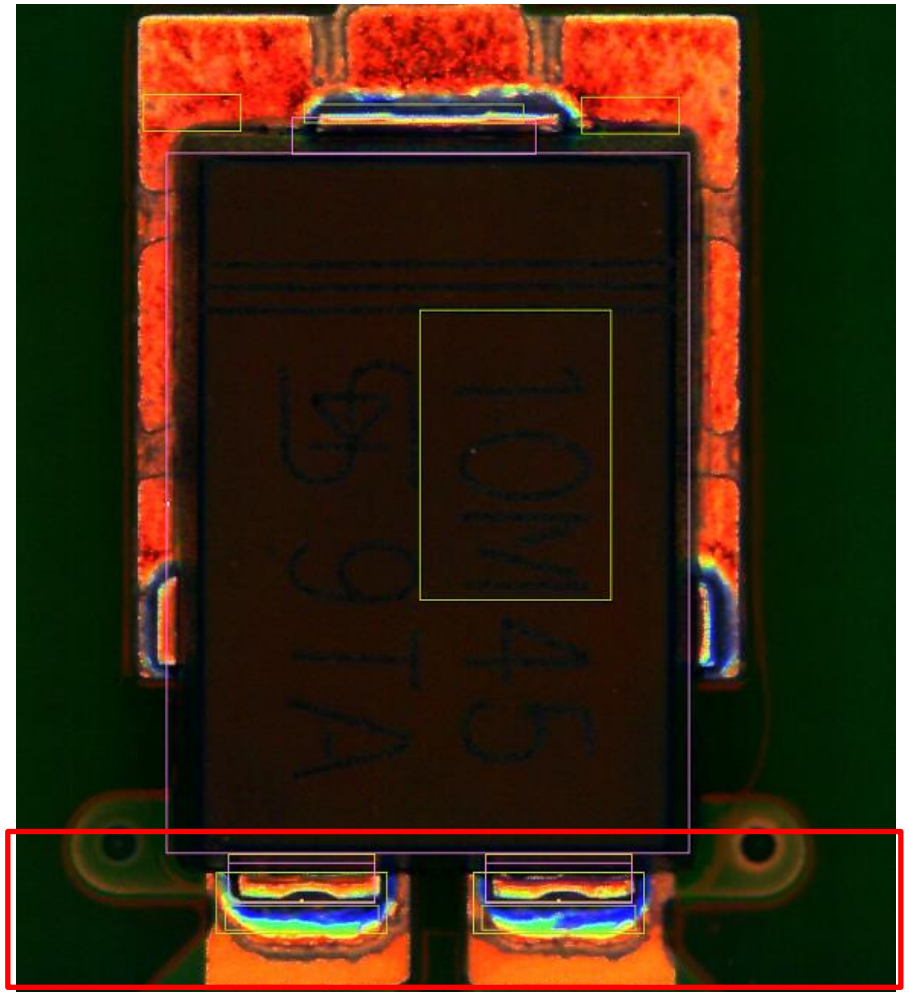


WETTABLE FLANK (AOI)

1.92mm 70% SMPC4.6

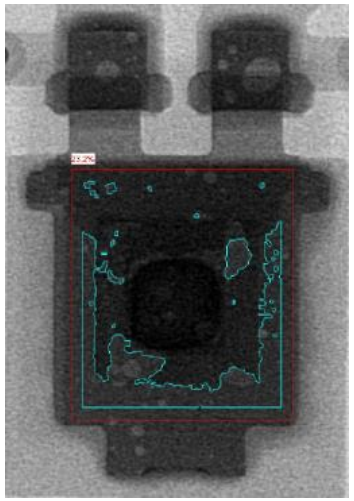


1.92mm 70% SMPC4.6U

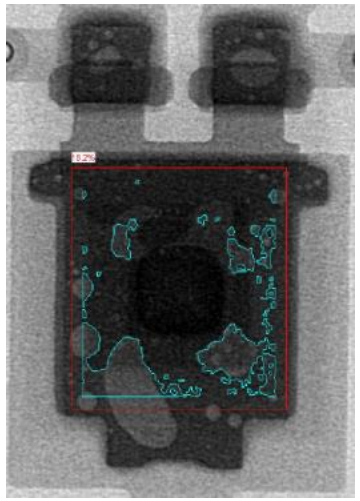


WETTABLE FLANK (X-RAY) – SMPC4.6 & SMPC4.6U

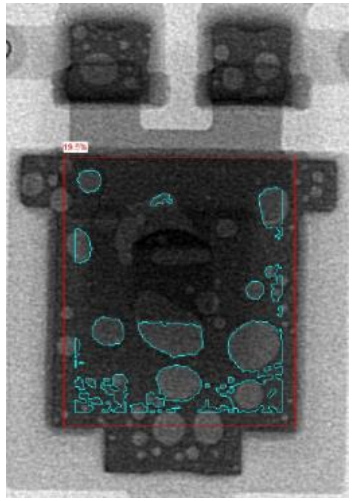
IPC-A-610 industry standard requires the total area ratio to be less 25%, and most companies design their PCB and manufacturing processes to maintain less than a 15% ~ 25% solder void ratio.



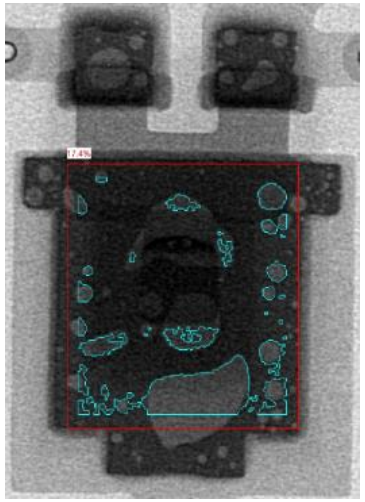
Solder Void : 23.2%



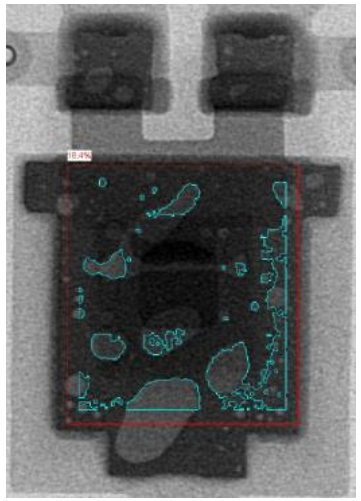
Solder Void : 18.2%



Solder Void : 19.5%



Solder Void : 17.4%

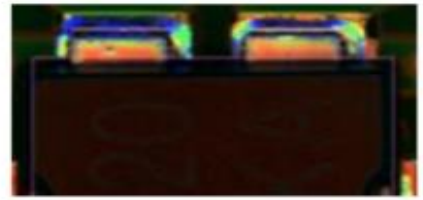
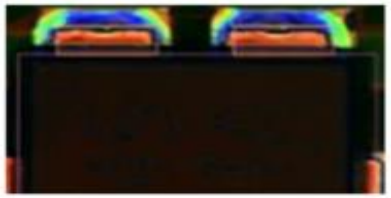
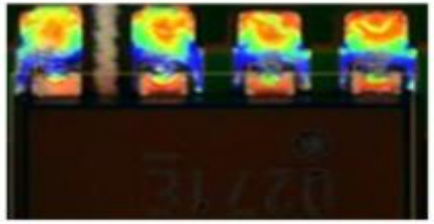
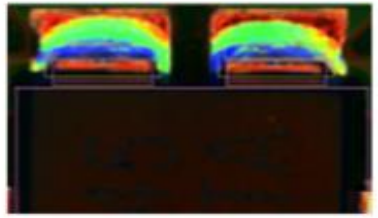


Solder Void : 18.4%

AOI TEST RESULTS

When examining the solder joints after reflow process, the AOI can capture the color light reflectivity signal to display tin solder slope level (next slide). Comparing the typical packages (PDFN56, SMPC4.6 package to the wettable flank packages (PDFN56**U**, SMPC4.6**U**), the results show more of a reflective gradient which is more uniform in shape.

Using an extended footprint for each pin results in the same benefits: Better light reflectivity gradient and more uniformity.

Package	Footprint pin length	AOI result	Package	Footprint pin length	AOI result
PDFN56	1.27mm		SMPC4.6	1.42mm	
PDFN56U	1.27mm		SMPC4.6U	1.42mm	
PDFN56U	1.77mm		SMPC4.6U	1.92mm	

TAIWAN SEMICONDUCTOR

FIT RATE RELIABILITY

Business Growth Through Quality

01. Zero Defect Strategy
02. Built-in Quality
03. Fast Time to Market
04. Stable Supply Chain
05. Manufacturing Efficiency
06. Supplier Quality Management
07. Customer Satisfaction

https://www.taiwansemi.com/en/quality/

- PRODUCT PERFORMANCE & QUALITY
- HIGH RELIABILITY PRODUCTS WITH LOW DEFECT RATE OF < 5PPB.
- QUALITY MANAGEMENT SYSTEM AND FACILITIES CERTIFIED TO ISO9001, IATF16949, ISO14000, AND AIAG STANDARDS.
- SYSTEMS AND PROCESSES CAPABLE OF MEETING VDA6.3 PROCESS AUDIT.
- PRODUCTS/DEVICES QUALIFIED TO AEC Q100/Q101.

RELIABILITY TESTING

- TC: Temperature Cycling (JESD22-A104)
- UHAST: Unbiased Highly Accelerated Stress Test
- RSH: Resistance to Solder Heat (JESD22-B102)
- SD: Solderability (JESD22-B102)
- HAST : High Accelerated Stress Test
- HTRB: High Temperature Reverse Bias (1000+ Hours)

Automotive Quality Programs

TSC is committed to meeting and exceeding the ever-increasing expectations of the global automotive industry.

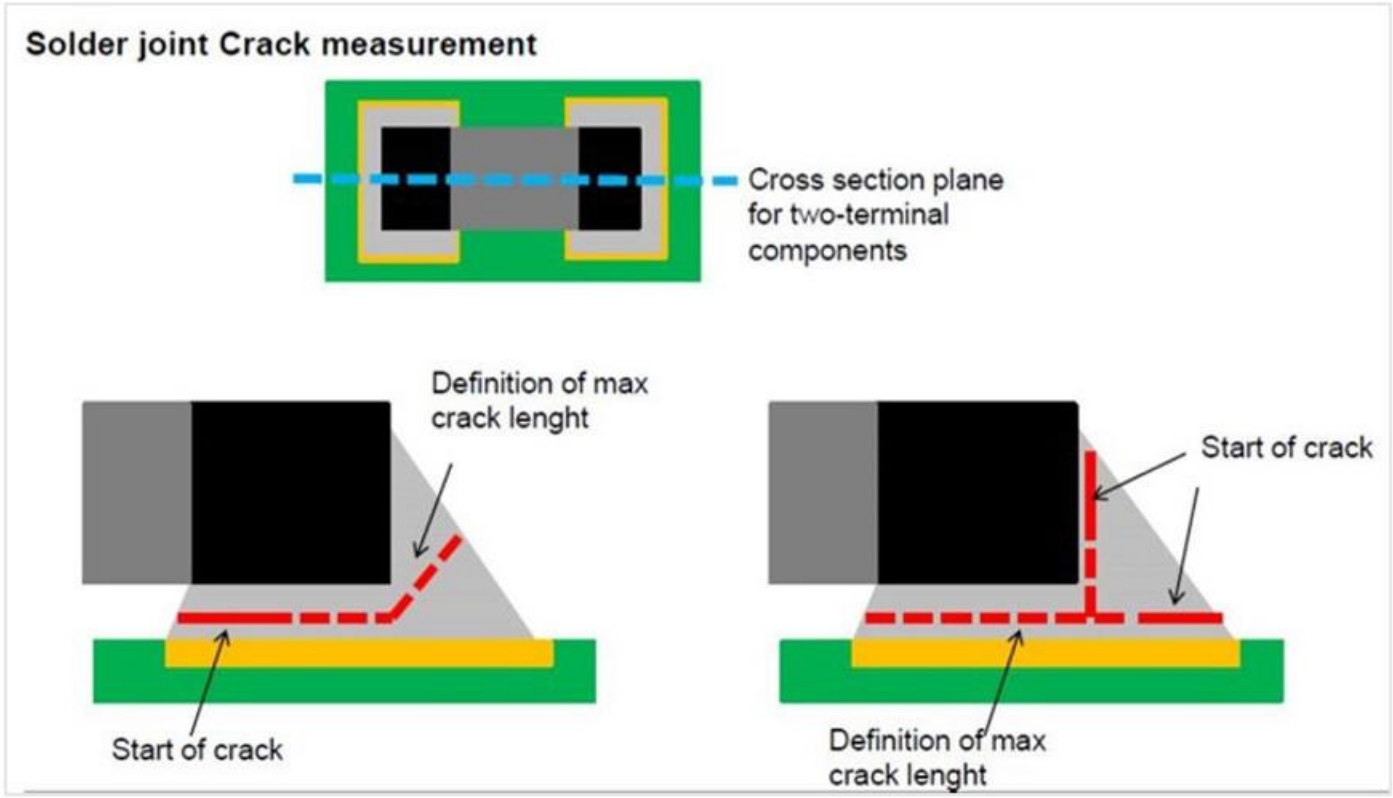
- Zero Error
- Zero Customer Returns
- Zero Warranty
- Zero Defect

TAIWAN SEMICONDUCTOR

RELIABILITY TESTING

After 1300 cycles -40~105℃ testing:

- Electrical function meet TSC datasheet and within 20%.
- Leakage (IGSS and IDSS) increase <5 times or <50nA for initial <10nA.
- Cross section: crack length max.=21.71% (specification<25%), the result pass

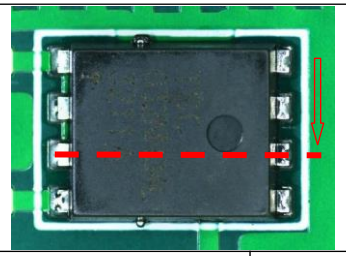
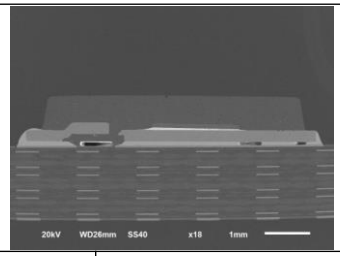
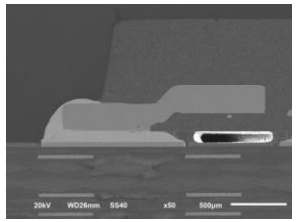
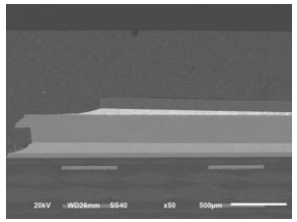
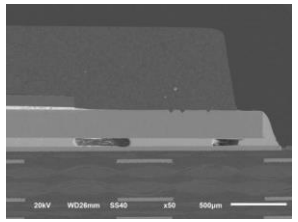
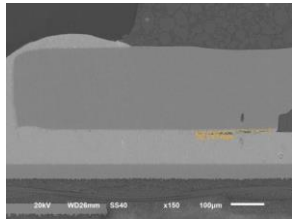
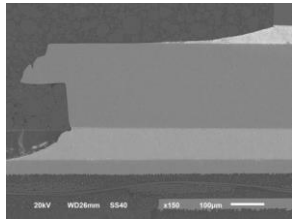
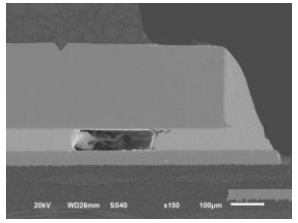


VISUAL INSPECTION

TAIWAN SEMICONDUCTOR

Attachment 1: Photos for cross section after 1300 cycles test

1. Due to manual grinding, Depth of section will be deviation
2. Remark: there are void in tin above the PCB

P-27-A		
Section diagram	Overview	
		
Left lead	Chip overview	Right lead
		
21.71%(221.47um)	N/A	<5%
Details-1	Details-2	Details-3
		

TAIWAN SEMICONDUCTOR

RELIABILITY TESTING

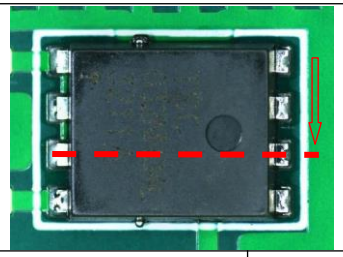
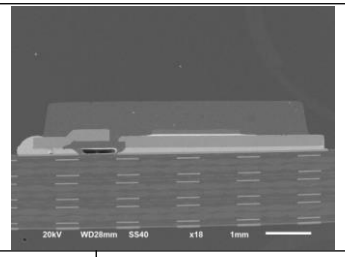
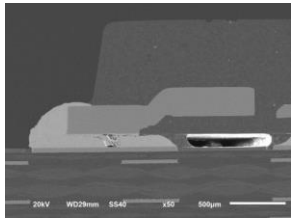
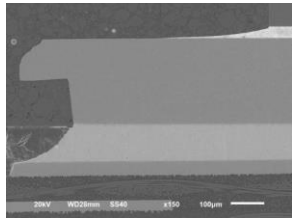
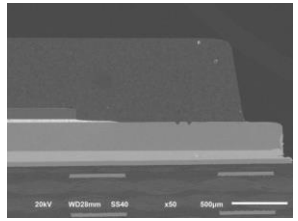
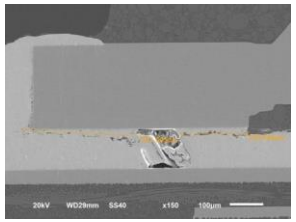
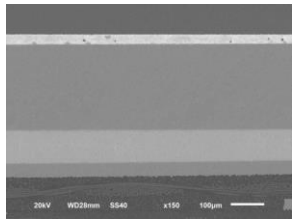
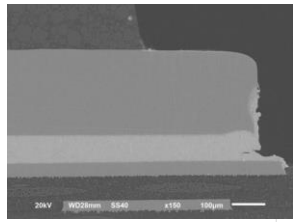
After 2600 cycles -40~105℃ testing:

- Electrical function meet TSC datasheet and within 20%.
- Leakage (IGSS and IDSS) increase <5 times or <50nA for initial <10nA.
- Cross section: crack length max.=59.06% (specification<90%), the result pass.
- Remark: Electrical function “Pass” means meet AEC-Q101 Rev.E requirement

VISUAL INSPECTION

Attachment 2: Photos for cross section after 2600 cycles test

1. Due to manual grinding, Depth of section will be deviation
2. Remark: there are void in tin above the PCB

P-29-A		
Section diagram	Overview	
		
Left lead	Chip overview	Right lead
		
54.03%(351.1um+200.0um)	N/A	<5%
Details-1	Details-2	Details-3
		

TAIWAN SEMICONDUCTOR

ELECTRICAL INSPECTION

Attachment 3: The electrical function test data

Before and after 2600 cycles test@25℃, the electrical data as below:

Test	Item	Condition	P-29-A		P-29-B		P-29-C		P-29-D		unit
			Before	After	Before	After	Before	After	Before	After	
T1	CONT	IB=10.00mA	3.1335	3.1335	3.1335	2.829	3.1335	2.829	2.22	3.438	mV
T2	DVDS	VDS=10.00V ID=1.53A IM=10.0mA	65.405	65.405	63.355	63.387	63.195	63.067	63.515	62.907	mV
T3	VFSD	IS=100.0uA	0.4014	0.4011	0.4139	0.4081	0.4051	0.403	0.4027	0.4017	V
T4	VTH	ID=100.0uA	1.5154	1.5163	1.5214	1.5117	1.5077	1.5062	1.5068	1.5044	V
T5	IGSS	VGS=23.00V	1.9128	1.964	2.5725	2.5112	2.3219	2.3707	2.1865	2.4182	nA
T6	IGSS	VGS=16.00V	0.0354	0.1741	0.039	0.1515	0.1101	0.1601	0.1436	0.1747	nA
T7	IGSS	VGS=-16.00V	-2.778	-2.4362	-2.4545	-3.4096	-4.8986	-2.6101	-3.1044	-2.9549	nA
T8	IDSX	VDS=10.00V, VGS=1.25V	1.9151	2.0372	1.9151	2.2814	2.495	2.5866	2.4035	2.6171	uA
T9	IDSS	VDS=32.00V	11.677	8.5947	11.28	13.142	13.538	14.82	14.576	15.095	nA
T10	IDSS	VDS=40.00V	25.959	22.48	21.656	30.811	26.081	26.844	26.936	28.187	nA
T11	VTH	ID=250.0uA, VGS=VDS	1.6789	1.6783	1.6764	1.6679	1.6649	1.6612	1.6621	1.66	V
T12	VTH	ID=1.000mA, VGS=VDS	1.776	1.7757	1.7739	1.7644	1.7623	1.7602	1.7608	1.7574	V
T13	BVDSS	ID=50.00uA	50.59	50.611	48.339	48.534	48.628	48.744	48.808	48.906	V
T14	BVDSS	ID=250.0uA	50.574	50.599	48.376	48.552	48.65	48.765	48.829	48.912	V
T15	BVDSS	ID=1.000mA	50.608	50.644	48.488	48.659	48.753	48.857	48.924	49.006	V
T16	RDSON	ID=40.00A, VGS=10V	0.0329	0.0335	0.0442	0.0441	0.0448	0.0442	0.0439	0.0441	Ω
T17	RDSON	ID=40.00A, VGS=6V	0.0345	0.0344	0.0448	0.045	0.0458	0.046	0.0455	0.0448	Ω
T18	RDSON	ID=40.00A, VGS=4.5V	0.0361	0.0366	0.049	0.0491	0.049	0.0493	0.0497	0.0494	Ω
T19	ABSDEL	= ABS (BVDSS3 - BVDSS2	0.0335	0.0457	0.1127	0.1066	0.1035	0.0914	0.0944	0.0944	V
T20	VFSD	IS=40.00A, VGS=0V	2.1067	2.1092	2.3541	2.3534	2.3531	2.3537	2.3537	2.3528	V
T21	GMP	VDS=10.00V, ID=10A	17.193	16.927	14.66	14.66	14.66	14.34	14.792	14.277	S
T22	IGSS	VGS=8.000V	0.3941	0.4602	0.3391	0.1988	0.3361	0.4734	0.4002	0.33	nA
T23	IGSS	VGS=-8.000V	-0.2668	-0.1203	-0.1722	-0.2515	-0.1814	-0.401	-0.1753	-0.4041	nA
T24	IDSS	VDS=20.00V	7.6792	1.4536	7.6486	8.5336	8.6862	9.5102	9.0219	10.304	nA

Test	Item	Condition	P-30-A		P-30-B		P-30-C		P-30-D		unit
			Before	After	Before	After	Before	After	Before	After	
T1	CONT	IB=10.00mA	2.5245	2.5245	2.829	1.6109	2.22	4.047	2.829	1.9154	mV
T2	DVDS	VDS=10.00V ID=1.53A IM=10.0mA	63.227	63.195	63.131	63.259	63.163	63.131	63.291	63.387	mV
T3	VFSD	IS=100.0uA	0.3993	0.4002	0.3993	0.3996	0.4005	0.4002	0.3999	0.3999	V
T4	VTH	ID=100.0uA	1.501	1.5026	1.5056	1.5044	1.5059	1.5047	1.5068	1.5059	V
T5	IGSS	VGS=23.00V	2.5173	2.4722	2.1548	2.3762	2.4274	2.389	2.5152	2.2899	nA
T6	IGSS	VGS=16.00V	0.1338	0.1439	0.1887	0.0521	0.1716	0.189	0.128	0.107	nA
T7	IGSS	VGS=-16.00V	-2.9915	-2.1616	-5.2403	-2.7902	-2.5186	-2.1799	-2.9214	-2.4362	nA
T8	IDSX	VDS=10.00V, VGS=1.25V	2.7392	2.6782	2.7392	2.7087	2.7087	2.6476	2.6782	2.6476	uA
T9	IDSS	VDS=32.00V	16.59	12.379	15.492	18.177	11.738	16.956	17.445	16.773	nA
T10	IDSS	VDS=40.00V	35.236	31.208	30.079	26.936	30.415	30.231	30.933	29.774	nA
T11	VTH	ID=250.0uA, VGS=VDS	1.6576	1.6585	1.6594	1.6582	1.66	1.6591	1.6588	1.6594	V
T12	VTH	ID=1.000mA, VGS=VDS	1.7553	1.7565	1.7581	1.7568	1.7577	1.7581	1.7577	1.7577	V
T13	BVDSS	ID=50.00uA	49.965	49.996	49.999	50.035	50.038	50.066	50.099	50.124	V
T14	BVDSS	ID=250.0uA	49.965	49.99	49.999	50.032	50.051	50.072	50.096	50.108	V
T15	BVDSS	ID=1.000mA	50.011	50.023	50.041	50.087	50.09	50.118	50.154	50.154	V
T16	RDSON	ID=40.00A, VGS=10V	0.044	0.0439	0.0444	0.0446	0.0441	0.0442	0.0441	0.0442	Ω
T17	RDSON	ID=40.00A, VGS=6V	0.0455	0.0456	0.0457	0.0449	0.0452	0.0453	0.0451	0.0455	Ω
T18	RDSON	ID=40.00A, VGS=4.5V	0.0493	0.0494	0.049	0.0492	0.049	0.0498	0.0495	0.0492	Ω
T19	ABSDEL	= ABS (BVDSS3 - BVDSS2	0.0457	0.0335	0.0426	0.0548	0.0396	0.0457	0.0579	0.0457	V
T20	VFSD	IS=40.00A, VGS=0V	2.5513	2.5519	2.551	2.5501	2.551	2.5519	2.551	2.551	V
T21	GMP	VDS=10.00V, ID=10A	14.53	14.53	14.726	14.466	14.277	14.403	14.859	14.595	S
T22	IGSS	VGS=8.000V	0.4093	0.452	0.2149	0.4154	0.4856	0.4917	0.3605	0.4032	nA
T23	IGSS	VGS=-8.000V	-0.1997	-0.1539	-0.2485	-0.2454	-0.2759	-0.6421	-0.575	-0.3888	nA
T24	IDSS	VDS=20.00V	10.67	4.1392	9.9069	14.149	6.8857	11.036	11.86	10.822	nA

TAIWAN SEMICONDUCTOR

ENVIRONMENTAL INFORMATION

- **Taiwan Semiconductor Material Category Policy:** Lead (Pb)-free (J-STD-609)
  RoHS-Compliant (2011/65/EU, 2015/863/EU)
  Halogen-free (IEC 61249-2-21)
- **SCIP Database Parts List Compliance:** Companies supplying articles containing substances of very high concern (SVHCs) on the Candidate List in a concentration above 0.1% weight by weight (w/w) on the EU market have to submit information on these articles to ECHA, as from 5 January 2021.
- **Environment Hazardous Substances Compliance (RoHS, POPs, TSCA directive):** The EU Restriction of the use of Hazardous Substances (RoHS) Directive 2002/95/EC took effect in 2006. Its replacement, Directive 2011/65/EU entered into force in 2011 and 2015/863/EU entered into force in 2015. RoHS applies to certain electrical and electronic equipment that are put on the market in EU member countries. RoHS may authorize continued use of lead where no feasible alternatives are available.
- **REACH Regulation 1907-2006-EC Compliance:** Regulation No 1907/2006 of the European Parliament and of the Council of 18 December 2006 on Registration, Evaluation, Authorization and Restriction of Chemicals entered into force on 1st June 2007. Substances are updated several times per year.
- **End-of-Life Vehicle Compliance:** The EU End-of-Life Vehicle Directive, 2000/53/EC, restricts the presence of lead, cadmium, mercury, and hexavalent chromium in vehicles. ELV authorizes continued use of lead where no feasible alternatives are available.
- **Conflict Minerals:** Section 1502 of the 2010 Dodd-Frank Wall Street Reform Act (US HR-4173) requires companies that must report to the SEC to determine if tin, tantalum, tungsten, gold or Cobalt are necessary to the functionality or production of a product manufactured by that company and, if so, to report annually whether directly or indirectly finance or benefit armed groups in the Democratic Republic of the Congo or an adjoining country.
- **California Proposition 65:** California Proposition 65, officially known as the Safe Drinking Water and Toxic Enforcement Act of 1986, was enacted in November 1986. The proposition protects the state's drinking water sources from being contaminated with chemicals known to cause cancer, birth defects or other reproductive harm, and requires businesses to inform Californians about exposures to such chemicals.

https://www.taiwansemi.com/en/quality/environmental/

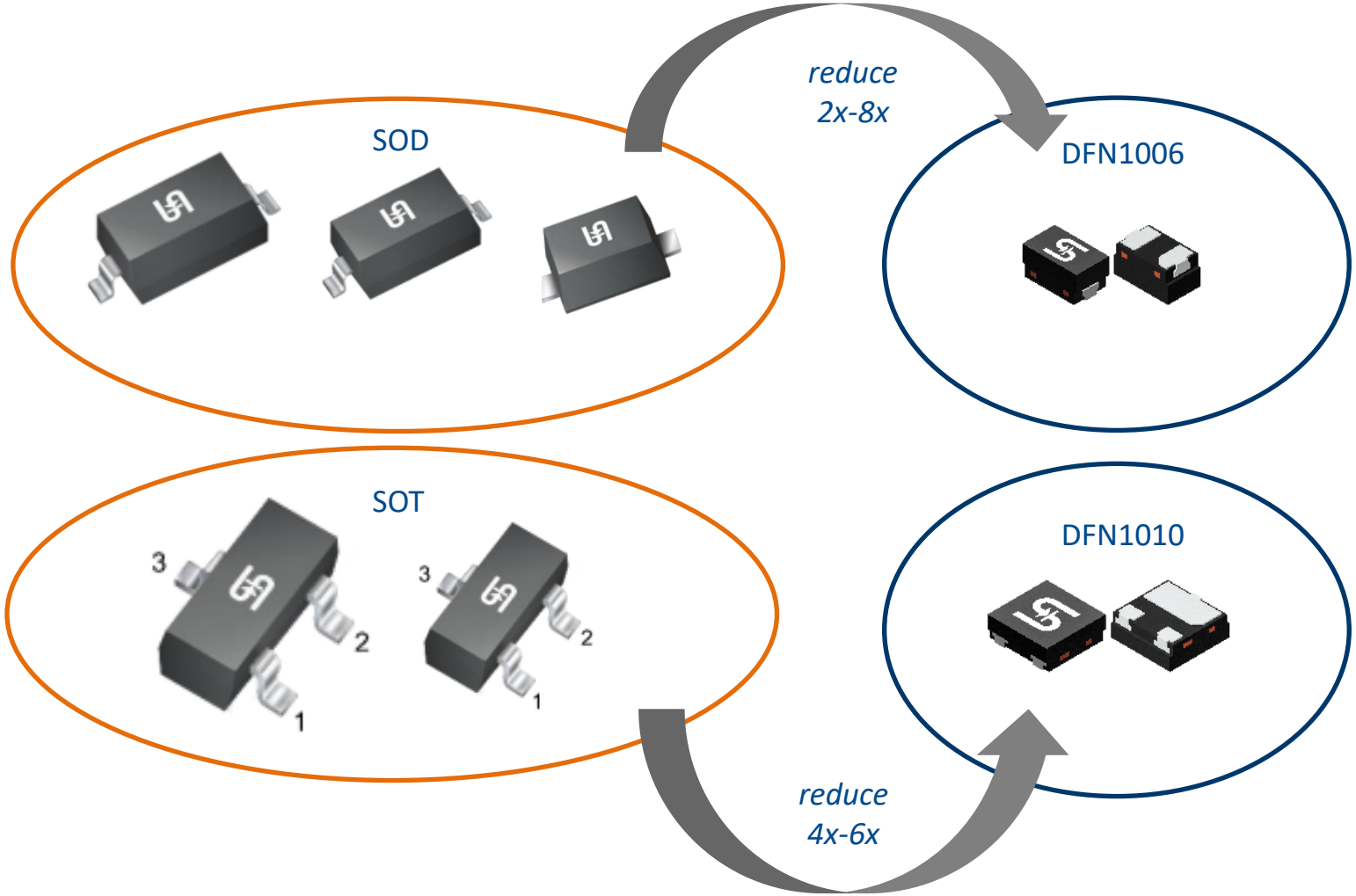
Why DFN (Dual Flat No-Lead) PACKAGE?

KEY DRIVER

Demand for compact devices

MINIATURIZATION

Reducing the size of semiconductor packages while maintaining or enhancing performance.



AECQ-101 capable

TAIWAN SEMICONDUCTOR

Small-signal DFN (Wettable Flank) Development

Design benefits:
- Same electrical performance at smaller size
- Support automated optical inspection (AOI) for solder quality control
- Reduced parasitic inductance and capacitance
- Improve thermal behavior – enables higher reliability
- Miniaturization from SOT23/SOT323, SOD-123/SOD323/SOD523

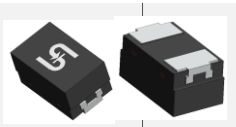
Key technical features and portfolio:
- Smallest form factor, less board space allows more design flexibility
- Lowest thermal resistance $R_{\Theta JX}$
- Optional side wettable flanks (SWF) allows automated optical inspection (AOI)
- AEC-Q101 Qualification

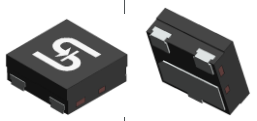
Target functions and applications:
- Linear voltage regulation
- Load switch
- Battery-driven devices
- Power management
- Power switches – Motor, Fan….etc

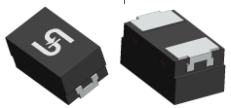
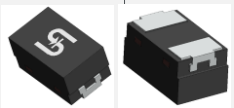
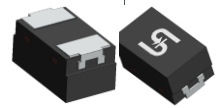
Small-signal DFN (Wettable Flank) Development Plan

Development Planning Engineering sample

		Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4
ESD Protection	DFN1006-2L						July						
	DFN1010-3L								Oct	Low Cj < 10pF			
Bipolar Transistor	DFN1010-3L						Jun						
MOSFET	DFN1010-3L						July						
Switching Diode	DFN1006-2L							May					
Schottky Diode	DFN1006-2L							Apr					
Zener	DFN1006-2L							May					
		2024				2025				2026			

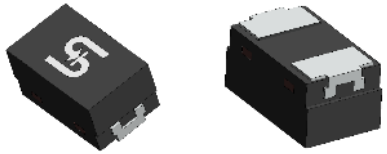


TAIWAN SEMICONDUCTOR

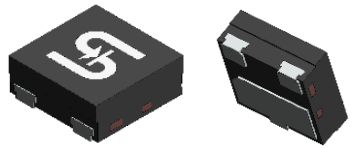
Product Line-Ups



Product	TSC NP PN	TSC NP Package	Vr (V)	IF (mA)	IR (uA)	trr (ns)
Switching diode	BAS16Q1H	DFN1006-2LW	100	215	0.5	4
Switching diode	BAS21Q1H	DFN1006-2LW	250	600	0.1	50
Switching diode	BAW56Q3H	DFN1010-3LW	70	200	2.5	6
Switching diode	BAV70Q3H	DFN1010-3LW	100	300	0.5	4

Product	TSC NP PN	TSC NP Package	Vr (V)	VF (mV)	IF (mA)
Schottky	BAS40Q1H	DFN1006-2LW	40	380	120
Schottky	BAS70Q1H	DFN1006-2LW	70	410	70

Product	TSC NP PN	TSC NP Package	VF (mV)	IF (mA)	Tolerance	Iz (mA)	PD (mW)	BV (V)
Zener	BZX884S-B2V4 ~ B75Q1H series	DFN1006-2LW	900	200	+/-2%	5/2	365	2V4 ~ 75V
Zener	BZX8850S-C2V4 ~ C43Q1H series	DFN1006-2LW	900	200	+/-5%	0.05	365	2V4 ~ 43V



Product	TSC NP PN	TSC NP Package	Vceo (V)	Ic (mA)	hFE
Transistor	BC807-25Q3H	DFN1010-3LW	-45	-500	160~400
Transistor	BC807-40Q3H	DFN1010-3LW	-45	-500	250~600
Transistor	BC817-25Q3H	DFN1010-3LW	45	500	160~400
Transistor	BC817-40Q3H	DFN1010-3LW	45	500	250~600
Transistor	BC846BQ3H	DFN1010-3LW	65	100	200~450
Transistor	BC847BQ3H	DFN1010-3LW	45	100	200~450
Transistor	BC847CQ3H	DFN1010-3LW	45	100	420~800
Transistor	BC856BQ3H	DFN1010-3LW	-65	-100	220~475
Transistor	BC857CQ3H	DFN1010-3LW	-45	-100	420~800
Transistor	BC857BQ3H	DFN1010-3LW	-45	-100	220~475

Product	TSC NP PN	TSC NP Package	Vrwm (V)	Vbr (V)	Cj (pF)	IEC61000-4-2 (kV)
ESD Protection	TESDA1L2B17P1Q1	DFN1006-2LW	15/24	21/31	17	23/23
ESD Protection	TESDA18VB05P1Q1	DFN1006-2LW	18	24	0.5	10/15
ESD Protection	TESDA22VU60P2Q3	DFN1010-3LW	22	29	60	30/30
ESD Protection	TESDA24VB17P2Q3	DFN1010-3LW	24	32	17	30/30
ESD Protection	TESDA13VU1052Q3	DFN1010-3LW	13	16	105	30/30
ESD Protection	TESDA26VU55P2Q3	DFN1010-3LW	26	35	55	30/30
ESD Protection	TESDA24VB6P02Q3	DFN1010-3LW	24	31	6	23/23
ESD Protection	TESDA22VU30P2Q3	DFN1010-3LW	22	29	30	30/30

Product	Type	TSC NP PN	TSC NP Package	Vds	Ron (ohm)	ESD
MOSFET	N-CH	TQM2N7002KQ3H	DFN1010-3LW	60	1.6	Y
MOSFET	N-CH	TQM2N7002Q3H	DFN1010-3LW	60	1.6	N
MOSFET	P-CH	TQM84KQ3H	DFN1010-3LW	-60	7	Y
MOSFET	N-CH	TQM123KQ3H	DFN1010-3LW	100	6	Y
MOSFET	N-CH	TQM138KQ3H	DFN1010-3LW	60	1.6	Y

ESD DIODE development roadmap

Released Development Planning

Bi, VRWM 24V, CJ 17pF		TESDA24VB17P1M3						SOD-323				
Bi, VRWM 24V, CJ 17pF		TESDA24VB17P1Q1						DFN1006 with Wettable flank				
Bi, VRWM 5V, CJ 0.5pF		TESDA5V0B05P1Q1						DFN1006 with Wettable flank				
Bi, VRWM 24V, CJ 6pF				TESDA24VB6P02Q3				DFN1010 with Wettable flank				
Bi, VRWM 24V, CJ 5pF				TESDA24VB5P02CX				SOT-23				
Bi, VRWM 24V, CJ 1.3pF					TESDA24VB1P32CX			SOT-23				
Bi, VRWM 15V/24V, CJ 17pF					TESDA1L2B17P1Q1			DFN1006 with Wettable flank				
Bi, VRWM3.3V~24V CJ 0.8pF				TESDAXXVB08P1M3				SOD-323				
	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4
	2024				2025				2026			

TAIWAN SEMICONDUCTOR

TVS DIODE DEVELOPMENT ROADMAP

Released | Development | Planning

Uni, 5000W VRWM 43V~100V	5KSMCXXAH	SMC (DO-214AB)
Bi, 5000W VRWM 10V~100V	5KSMCXXCAH	SMC (DO-214AB)
Bi, 400W VRWM 5V~75V	SMF4LXXCAH	SOD-123W
Bi, 600W VRWM 12V~60V	SMA6SXXCAH / SMA6FXXCAH	SOD-128 / Thin SMA
Bi, SuperClamp VRWM 24V	LSMC24CAH	SMC (DO-214AB)
Bi, SuperClamp VRWM 24V	LSMB24CAH	SMB (DO-214AA)
Uni/Bi, 400W, Non-Auto VRWM 5V~200V	SMAJXX(C)A-TR	SMA (DO-214AC)
Uni/Bi, 600W, Non-Auto VRWM 5V~150V	SMBJXX(C)A-TR	SMB (DO-214AA)
Uni/Bi, 1500W, Non-Auto VRWM 5V~150V	SMCJXX(C)A-TR	SMC (DO-214AB)
Uni/Bi, 3000W, Non-Auto VRWM 5V~150V	SMDJXX(C)A-TR	SMC (DO-214AB)

Q1 Q2 Q3 Q4 Q1 Q2 Q3 Q4 Q1 Q2 Q3 Q4

2024 | 2025 | 2026

45 YEARS ANNIVERSARY

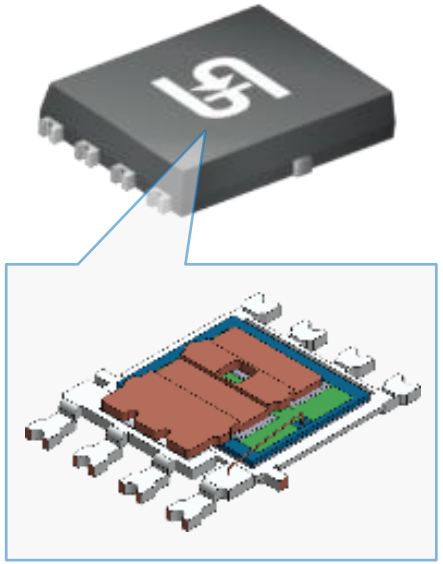
TAIWAN SEMICONDUCTOR

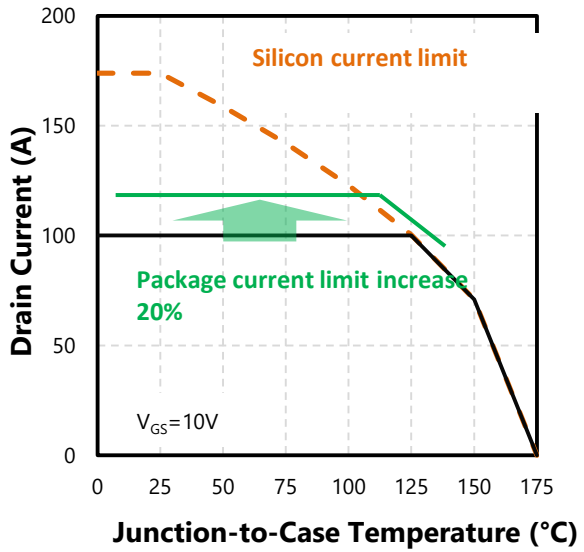
UPCOMING NEW PRODUCTS IN 2025

In development

Ultra low Rdson MOSFETs

PerFET™ MOSFET in the PDFN 5mm x 6mm package now feature advanced clip source bonding technology. This innovation significantly reduces parasitic inductance and enhances thermal and electrical performance. It is ideal for high-efficiency, high-current applications in compact designs.





Product Table						
P/N	Voltage [V]	RDS(on) [mΩ]	VGS(th) [V]	ID [A]	Qg [nC]	Package
TQM011NH04LCR	40	1.1	1.4 - 2.2	120	143	PDFN56U
TQM011NH04CR	40	1.1	2.4 - 3.6	120	127	PDFN56U
TQM013NH04LCR	40	1.3	1.4 - 2.2	120	104	PDFN56U
TQM013NH04CR	40	1.3	2.4 - 3.6	120	88	PDFN56U
TQM038NH08LCR	80	3.8	1.4 - 2.2	120	47	PDFN56U
TQM038NH08CR	80	3.8	2.4 - 3.6	120	35	PDFN56U
TQM036NH10LCR	100	3.6	1.4 - 2.2	120	54	PDFN56U
TQM039NH10CR	100	3.9	2.4 - 3.6	120	40	PDFN56U
TQM040NH10LCR	100	4.0	1.4 - 2.2	120	47	PDFN56U
TQM043NH10CR	100	4.3	2.4 - 3.6	120	35	PDFN56U

Features

- AEC-Q101 qualified
- Ultra low package resistance
- Good thermal conducting
- Better current capability and SOA

Target Release Schedule

❖ **Q1 2026**

TAIWAN SEMICONDUCTOR

PerFET™ 40V

The PerFET™ 40V series family implemented the latest trench technology that enable exceptionally low on-state resistance and switching figure-of-merit (FOM - R*Q). The achievement of 50% RDS(on) and 40% FOM reduction compared to the previous technology (NB Series) puts this portfolio at the industry leading edge of performance. The value of RDS(on) at temperatures of -50°C to 175°C presented less variation due to its lower temperature coefficient (K).

A portfolio of 18 items, including both normal-level and logic-level gate drive types, enables customers to select the best-fit product for their design.

The PDFN56U wettable flank package offers improved solder joint quality and enhanced AOI accuracy. Additionally, it is highly footprint-compatible with the majority of 5mm × 6mm packages on the market.

Key Features

- AEC-Q101 qualified
- Best-in-class FOM (RDS(on) * Qg)
- Optimized RDS(on) for low conduction losses
- Low gate charge for reduced switching losses
- Optimized Qgd/Qgs ratio reduced induced gate voltages during switching
- 175°C junction temperature (Tj)
- Wettable flank enhanced AOI accuracy

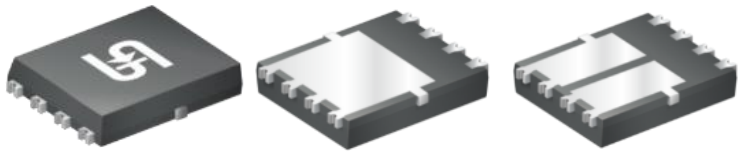
Key Applications

- 12V Automotive applications
- High efficiency power supply
- Server power supply
- Motor drive applications

TxM: TSM – Standard grade ; TQM – Automotive grade.

Product Table

P/N	Voltage [V]	RDS(on) [mΩ]	VGS(th) [V]	ID [A]	Qg [nC]	Package
TxM019NH04LCR	40	1.9	1.4 - 2.2	100	104	PDFN56U
TxM019NH04CR	40	1.9	2.4 - 3.6	100	89	PDFN56U
TxM025NH04LCR	40	2.5	1.4 - 2.2	100	63	PDFN56U
TxM025NH04CR	40	2.5	2.4 - 3.6	100	59	PDFN56U
TxM032NH04LCR	40	3.2	1.4 - 2.2	81	50	PDFN56U
TxM032NH04CR	40	3.2	2.4 - 3.6	81	45	PDFN56U
TxM043NH04LCR	40	4.3	1.4 - 2.2	54	42	PDFN56U
TxM043NH04CR	40	4.3	2.4 - 3.6	54	37	PDFN56U
TxM056NH04LCR	40	5.6	1.4 - 2.2	54	30	PDFN56U
TxM056NH04CR	40	5.6	2.4 - 3.6	54	27	PDFN56U
TxM070NH04LCR	40	7.0	1.4 - 2.2	54	23	PDFN56U
TxM070NH04CR	40	7.0	2.4 - 3.6	54	19	PDFN56U
TxM076NH04LDCR	40	7.6	1.4 - 2.2	40	23	PDFN56UD
TxM076NH04DCR	40	7.6	2.4 - 3.6	40	19	PDFN56UD
TSM056NH04LCV	40	5.6	1.4 - 2.2	54	27	PDFN33
TSM056NH04CV	40	5.6	2.4 - 3.6	54	30	PDFN33
TSM070NH04LCV	40	7.0	1.4 - 2.2	54	19	PDFN33
TSM070NH04CV	40	7.0	2.4 - 3.6	54	23	PDFN33

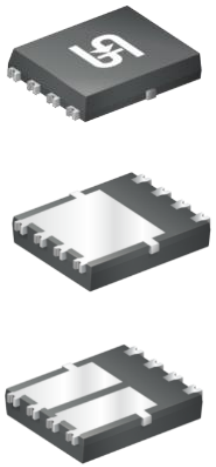


TAIWAN SEMICONDUCTOR

PerFET™ 60V POWER MOSFETS

In development

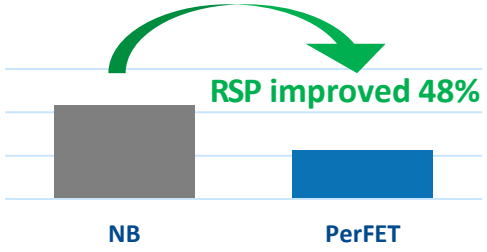
PDFN56U/D



Product Table								
P/N	Voltage	RDS(on) [mΩ]	VGS [V]	VGS(th) [V]	ID	Qg	Tj.max	Package
TQM026NH06LCR	60V	2.6	±20V	1.4V ~ 2.2V	100A	84nC	175°C	PDFN56U
TQM027NH06CR	60V	2.7	±20V	2.4V ~ 3.6V	100A	87nC	175°C	PDFN56U
TQM037NH06LCR	60V	3.7	±20V	1.4V ~ 2.2V	100A	53nC	175°C	PDFN56U
TQM038NH06CR	60V	3.8	±20V	2.4V ~ 3.6V	100A	55nC	175°C	PDFN56U
TQM050NH06LCR	60V	5.0	±20V	1.4V ~ 2.2V	81A	37nC	175°C	PDFN56U
TQM052NH06CR	60V	5.2	±20V	2.4V ~ 3.6V	81A	39nC	175°C	PDFN56U
TQM080NH06LCR	60V	8.0	±20V	1.4V ~ 2.2V	54A	23nC	175°C	PDFN56U
TQM085NH06CR	60V	8.5	±20V	2.4V ~ 3.6V	54A	24nC	175°C	PDFN56U
TQM115NH06LCR	60V	12.0	±20V	1.4V ~ 2.2V	54A	16nC	175°C	PDFN56U
TQM120NH06CR	60V	12.0	±20V	2.4V ~ 3.6V	54A	16nC	175°C	PDFN56U
TQM130NH06LDCR	60V	13.0	±20V	1.4V ~ 2.2V	40A	16nC	175°C	PDFN56UD
TQM130NH06DCR	60V	13.0	±20V	2.4V ~ 3.6V	40A	16nC	175°C	PDFN56UD

Features

- AEC-Q101 qualified
- Very low on-resistance reduce conduction loss
- less Rdson variation at -55°C to 175°C
- Excellent FOM (Rdson * Qg)



Application

- 12V - 24V Automotive applications
- Switching power supply
- Server power supply
- Motor drive applications

Target Release Schedule

❖ **Mar 2026**

TAIWAN SEMICONDUCTOR

UPCOMING NEW PRODUCTS IN 2025

In development

PerFET™ 80V and 100V Power MOSFETs

Taiwan Semiconductor introduces its next-generation PerFET™ 80V and 100V Power MOSFETs, optimized for high-frequency switching. These devices are ideal for synchronous rectification in telecom and server power supplies, as well as for industrial applications such as solar inverters, power tools, DC-DC brick converters, and power adapters.

Packaged in a compact PDFN56U package, the PerFET™ 80V and 100V MOSFETs feature a wettable flank design, which improves solder joint reliability and enhances automated optical inspection (AOI) accuracy. The product portfolio includes 18 variants, offering both standard gate drive (10V) and logic-level gate drive (5V) options—giving designers the flexibility to choose the optimal solution for their application.

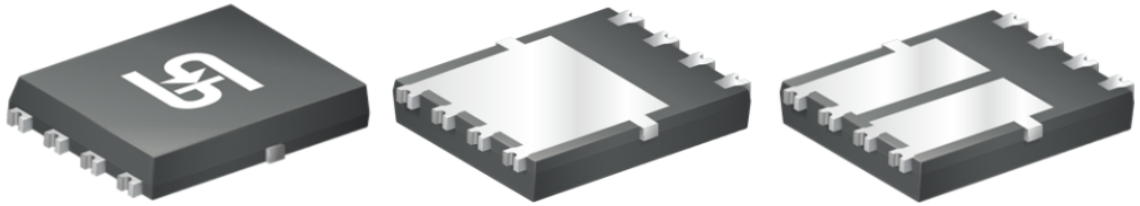


Figure1: PDFN56U and PDFN56U Dual package

Key Features

- Reliability meets AEC-Q101 requirements
- Best-in-class FOM ($R_{DS(on)}$ * Q_g)
- Optimized $R_{DS(on)}$ for low conduction losses
- Low gate charge for reduced switching losses
- 175°C junction temperature (T_J)
- Wettable flank enhanced AOI accuracy

Applications

- 48V Automotive applications
- SMPS, Server and Telecom power supply
- DC/DC converter
- BLDC motor driver
- E-Fuse

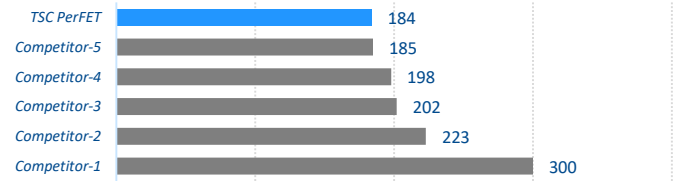
TAIWAN SEMICONDUCTOR

PerFET™ 80V & 100V

PerFET™ 80V and 100V technology in the PDFN56U (5mm x 6mm) single and dual packages are designed for high power, high switching frequency and high-performance requirement automotive and industrial applications. A portfolio of 18 items, including both normal-level and logic-level gate drive types, enables customers to select the best-fit product for their design.

The PDFN56U wettable flank package offers improved solder joint quality and enhanced AOI accuracy. Additionally, it is highly footprint-compatible with the majority of 5mm × 6mm packages on the market.

FOM Comparison



Key Features

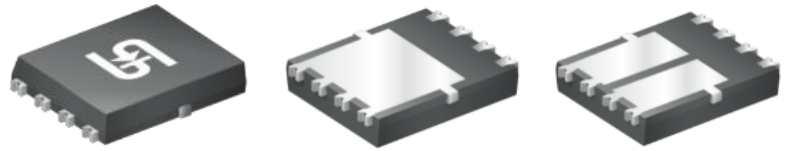
- AEC-Q101 qualified
- Best-in-class FOM (RDS(on) * Qg)
- Optimized RDS(on) for low conduction losses
- Low gate charge for reduced switching losses
- 175°C junction temperature (Tj)
- Wettable flank enhanced AOI accuracy

Key Applications

- 48V Automotive applications
- SMPS, Server and Telecom power supply
- DC/DC converter
- BLDC motor driver
- E-Fuse

Product Table

P/N	Voltage [V]	RDS(on) [mΩ]	VGS(th) [V]	ID [A]	Qg [nC]	Package
TQM048NH10LCR	100	4.8	1.4 - 2.2	100	47	PDFN56U
TQM048NH10CR	100	4.8	2.4 - 3.6	100	35	PDFN56U
TQM075NH10LCR	100	7.5	1.4 - 2.2	100	37	PDFN56U
TQM075NH10CR	100	7.5	2.4 - 3.6	100	22	PDFN56U
TQM100NH10LCR	100	10	1.4 - 2.2	81	25	PDFN56U
TQM100NH10CR	100	10	2.4 - 3.6	81	20	PDFN56U
TQM170NH10LCR	100	17	1.4 - 2.2	54	17	PDFN56U
TQM170NH10CR	100	17	2.4 - 3.6	54	11	PDFN56U
TQM240NH10LCR	100	24	1.4 - 2.2	54	10	PDFN56U
TQM240NH10CR	100	24	2.4 - 3.6	54	8.4	PDFN56U
TQM250NH10LDCR	100	25	1.4 - 2.2	40	10	PDFN56UD
TQM250NH10DCR	100	25	2.4 - 3.6	40	8.4	PDFN56UD
TQM058NH08LCR	80	5.8	1.4 - 2.2	100	35	PDFN56U
TQM063NH08CR	80	6.3	2.4 - 3.6	100	27	PDFN56U
TQM130NH08LCR	80	13	1.4 - 2.2	54	17	PDFN56U
TQM145NH08CR	80	14.5	2.4 - 3.6	54	13	PDFN56U
TQM210NH08LDCR	80	21	1.4 - 2.2	38	10	PDFN56UD
TQM230NH08DCR	80	23	2.4 - 3.6	38	8.4	PDFN56UD

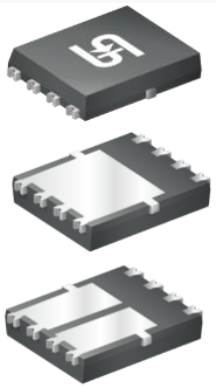


TAIWAN SEMICONDUCTOR

-30V/-40V/-60V P-CH POWER MOSFETS

In development

PDFN56U/D



TO-252

Product Table							
P/N	Voltage	RDS(on) [mΩ]	VGS [V]	VGS(th) [V]	Qg	Tj.max	Package
TQM075PC03LCR	-30V	7.5	±20	1.4 ~ 2.4	TBD	175°C	PDFN56U
TQM100PC03LCR	-30V	10.0	±20	1.4 ~ 2.4	TBD	175°C	PDFN56U
TQM045PC04LCR	-40V	4.5	±20	1.4 ~ 2.4	TBD	175°C	PDFN56U
TQM095PC04LCR	-40V	9.5	±20	1.4 ~ 2.4	TBD	175°C	PDFN56U
TQM140PC04LCR	-40V	14.0	±20	1.4 ~ 2.4	TBD	175°C	PDFN56U
TQM150PC06LCR	-60V	15.0	±20	1.4 ~ 2.4	TBD	175°C	PDFN56U
TQM650PC06LCR	-60V	65.0	±20	1.4 ~ 2.4	TBD	175°C	PDFN56U
TQM660PC06LDCR	-60V	66.0	±20	1.4 ~ 2.4	TBD	175°C	PDFN56UD
TQM060PC04LCP	-40V	6.0	±20	1.4 ~ 2.4	TBD	175°C	DPAK
TQM105PC04LCP	-40V	10.5	±20	1.4 ~ 2.4	TBD	175°C	DPAK
TQM150PC04LCP	-40V	15.0	±20	1.4 ~ 2.4	TBD	175°C	DPAK
TQM165PC06LCP	-60V	16.5	±20	1.4 ~ 2.4	TBD	175°C	DPAK
TQM660PC06LCP	-60V	66.0	±20	1.4 ~ 2.4	TBD	175°C	DPAK

Features

- Advanced trench technology
- AEC-Q101 qualified
- Logical level
- Low Qg for easy drive
- Excellent FOM (Rdson * Qg)

Application

- 12V - 24V Automotive applications
- Power Reverse Protections
- Oil / Water / Heat pumps

Target Release Schedule

- **Q4 2026**

TAIWAN SEMICONDUCTOR

PDFN33U PACKAGE DEVELOPMENT

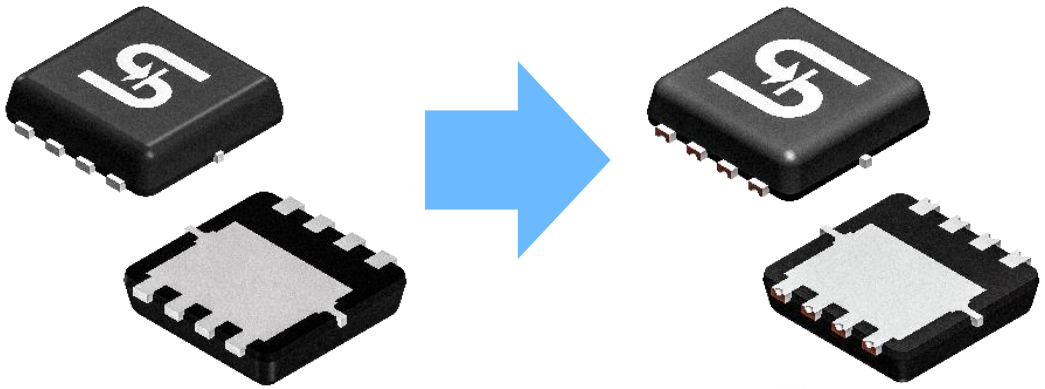
In development

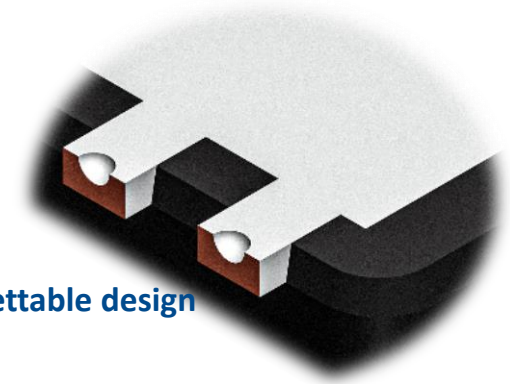
POD

Package name：PDFN33U
Package P/N code：CU
Package size：3.3mm x 3.3mm
The same POD with regular PDFN33 package in the market

PDFN33；CV

PDFN33U；CU





Wettable design

	Product Table					
	TSC P/N	BVDSS [V]	RDS(on) [mΩ]	VGS [V]	VGS(th) [V]	Tj max. [°C]
N-MOS	TQM056NH04LCU	40	5.6	±16	1.4 - 2.2	175
	TQM056NH04CU	40	5.6	±20	2.2 - 3.8	175
	TQM070NH04LCU	40	7.0	±16	1.4 - 2.2	175
	TQM072NH04CU	40	7.0	±20	2.2 - 3.8	175
	TQM130NH08LCU	80	13.0	±20	1.4 - 2.2	175
	TQM140NH08CU	80	14.0	±20	2.2 - 3.8	175
	TQM210NH08LCU	80	21.0	±20	1.4 - 2.2	175
	TQM220NH08CU	80	22.0	±20	2.2 - 3.8	175
	TQM150NH10LCU	100	15.0	±20	1.4 - 2.2	175
	TQM165NH10CU	100	16.5	±20	2.2 - 3.8	175
	TQM220NH10LCU	100	22.0	±20	1.4 - 2.2	175
	TQM235NH10CU	100	23.5	±20	2.2 - 3.8	175
P-MOS	TQM075PC03LCU	-30	7.5	±20	1.4 - 2.2	175
	TQM100PC03LCU	-30	10.0	±20	1.4 - 2.2	175
	TQM140PC04LCU	-40	14.0	±20	1.4 - 2.2	175
	TQM650PC06LCU	-60	65.0	±20	1.4 - 2.2	175

Release schedule

- 40V, 80V & 100V N-MOS：Q2, 2026
- -30V, -40V & -60V P-MOS：Q4, 2026

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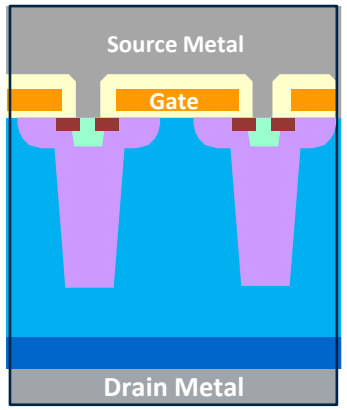
TECHNOLOGY TREND OF SUPER JUNCTION MOSFET

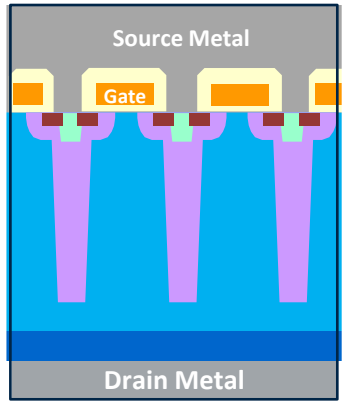
1st Generation



N Series

- *Deep trench technology*
- *Greatly reduce Rdson*
- *Improved switching performance*

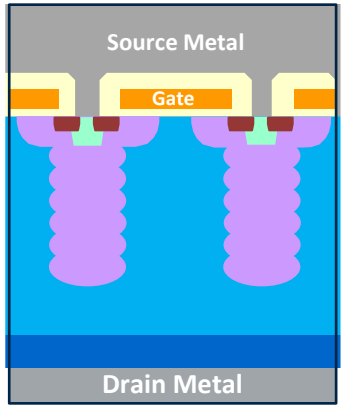
2nd Generation



NB Series

- *Deep trench technology*
- *Increased density*
- *Reduced Rdson*
- *Improved di/dt.*

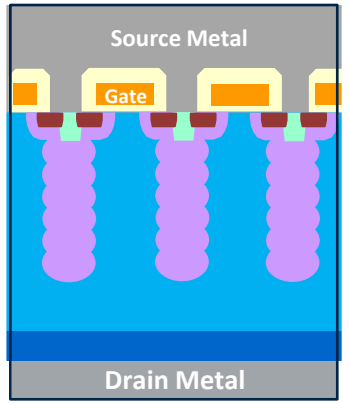
3rd Generation



NC Series

- *Multi EPI technology*
- *Improved switching performance*
- *Improved EMI performance*
- *Higher di/dt and dv/dt*

4th Generation



NE Series

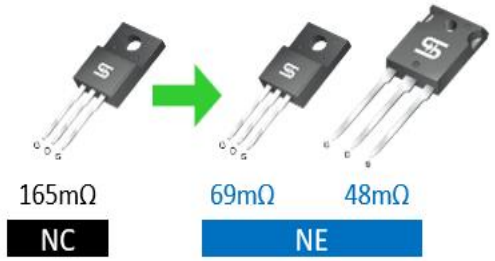
- *Multi EPI technology*
- *Increased density*
- *Reduced Rdson*
- *Reduced Qg*
- *Enhanced gate noise immunity*

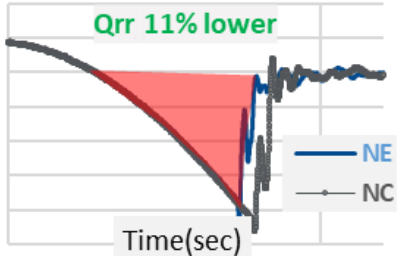
TAIWAN SEMICONDUCTOR

GEN-4th NE SERIES SUPER JUNCTION MOSFETS

The 600V NE Family utilizes 4th-generation super junction technology, enabling exceptionally low on-state resistance (RDS(on)) and low gate charge capacitance (Qg). This achievement results in a 30% improvement in figure-of-merit (FoM; RDS(on) × Qg), delivering higher value in many high-voltage applications compared to alternative options.

The 600V NE Family offers various package options, including PDFN8x8 and TOLL, to accommodate a broader range of design requirements for different applications.





Key Features

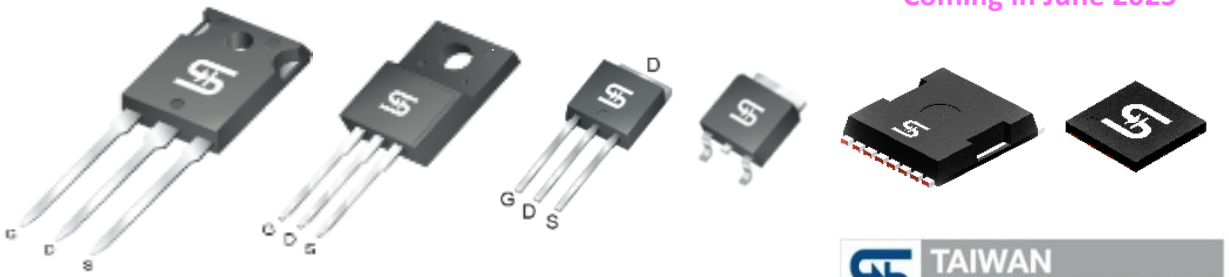
- 4th generation super junction technology
- Ultra low Rdson available
- Better FOM and Lower Qrr
- High gate noise immunity
- The Kelvin-source pin helps reduce switching losses [TOLL]

Key Applications

- SMPS and server power supply
- Lighting power
- HV motor driver
- Micro PV inverter

Product Table				
P/N	Voltage [V]	RDS(on) [mΩ]	ID [A]	Package
TSM60NE069CIT C0G	600	69	26	ITO-220TL
TSM60NE084CIT C0G	600	84	22	ITO-220TL
TSM60NE110CIT C0G	600	110	19	ITO-220TL
TSM60NE145CIT C0G	600	145	14	ITO-220TL
TSM60NE180CIT C0G	600	180	13	ITO-220TL
TSM60NE200CIT C0G	600	200	12	ITO-220TL
TSM60NE285CIT C0G	600	285	7.1	ITO-220TL
TSM60NE048PW C0G	600	48	64	TO-247-3L
TSM60NE069PW C0G	600	69	46	TO-247-3L
TSM60NE084PW C0G	600	84	41	TO-247-3L
TSM60NE285CH C5G	600	285	11	TO-251
TSM60NE285CP C0G	600	285	11	TO-252
TSM60NE084TL RAG *	600	84	47	TOLL
TSM60NE110TL RAG *	600	110	30	TOLL
TSM60NE110CE RVG *	600	110	30	PDFN88
TSM60NE145CE RVG *	600	145	14	PDFN88
TSM60NE180CE RVG *	600	180	13	PDFN88
TSM60NE285CE RVG *	600	285	11	PDFN88

*** Coming in June 2025**



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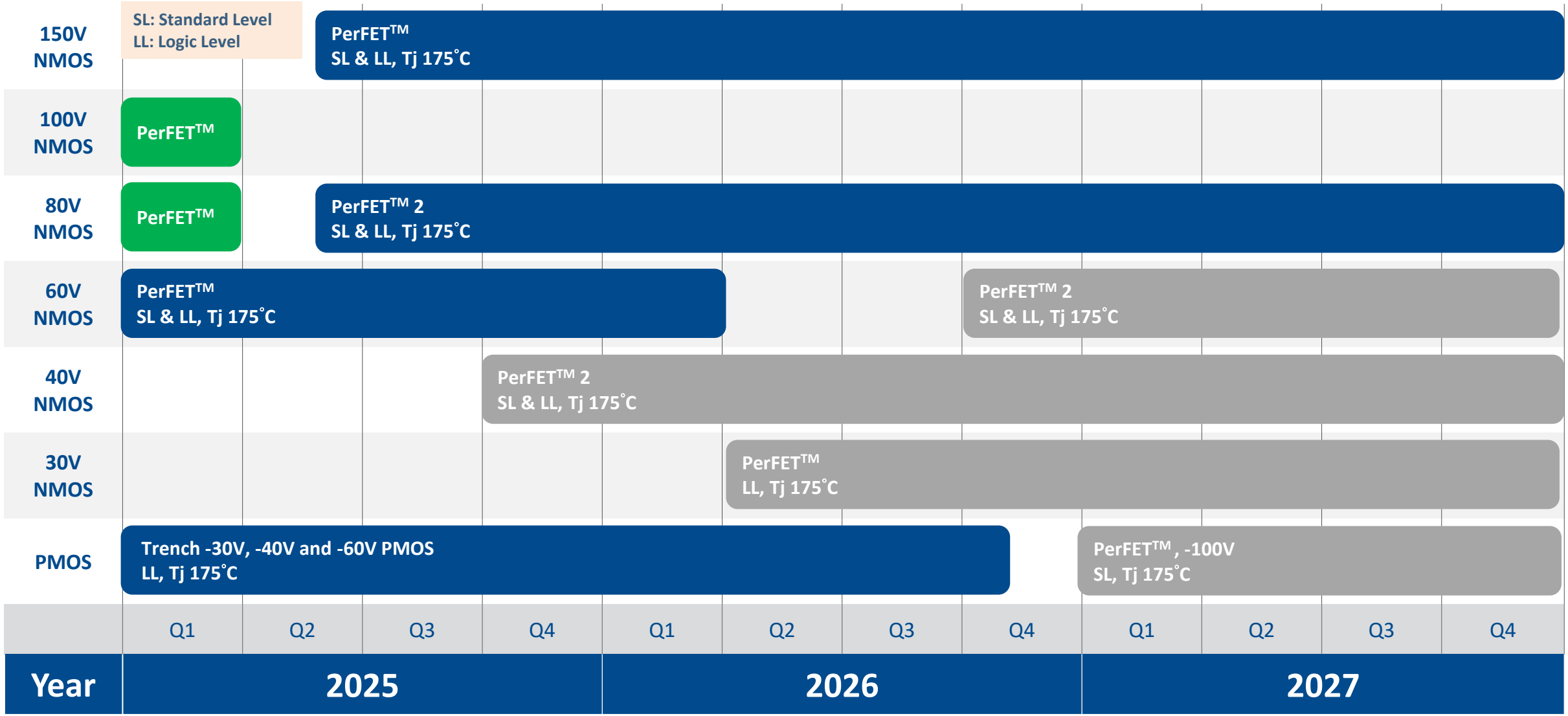
WAFER TECHNOLOGY ROADMAP

Production | Development | Plan



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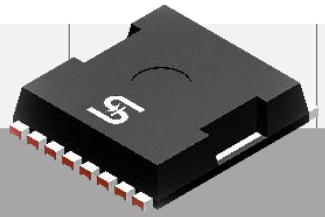
PACKAGE TECHNOLOGY ROADMAP

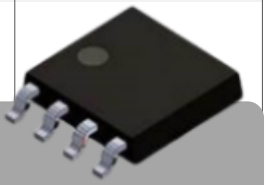
Developing | Plan

TOLL
10mm x 12mm



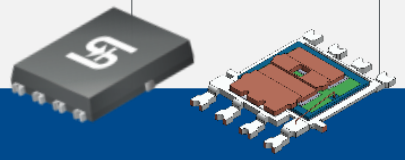
Automotive
TOLL

PDFN88G
8mm x 8mm

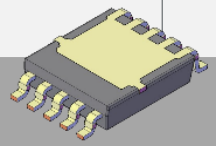


Automotive
PPAK88G

PDFN56U
5mm x 6mm

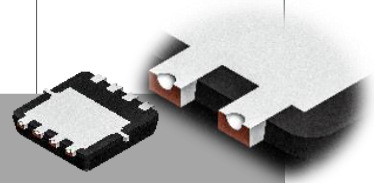


Automotive
Clip bond



Automotive
TSCPAK57 (5mm x7.5mm)

PDFN33U
3.3mm x 3.3mm



Automotive
Wettable-Flank

	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4
Year	2025				2026			

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TECHNOLOGY ROADMAP FOR HV MOSFET

Developing | Plan

650V

NE Series (ITO-220, TO-247, PDFN88 and TOLL)
Tj 150 ˚C

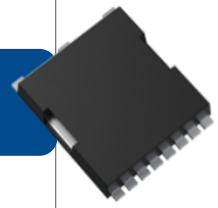
NF Series (PDFN88 and TOLL)
Fast recovery; Tj 150 ˚C

600V

600V NE Series in PDFN88
Tj 150 ˚C

NF Series (PDFN88 and TOLL)
Fast recovery; Tj 150 ˚C

600V NE Series in TOLL
Tj 150 ˚C



	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4
Year	2025				2026			

Wettable Flank Package

For Better Solder Joint Quality

TAIWAN SEMICONDUCTOR

WHY TSC?

1. PRODUCT PERFORMANCE & QUALITY

- HIGH RELIABILITY PRODUCTS WITH LOW DEFECT RATE OF < 5PPB.
- QUALITY MANAGEMENT SYSTEM AND FACILITIES CERTIFIED TO ISO9001, IATF16949, ISO14000, AND AIAG STANDARDS.
- SYSTEMS AND PROCESSES CAPABLE OF MEETING VDA6.3 PROCESS AUDIT.
- PRODUCTS/DEVICES QUALIFIED TO AEC Q100/Q101.

2. TECHNOLOGY & INNOVATION

- OUR INNOVATION-DRIVEN APPROACH LEVERAGES CUTTING-EDGE TECHNOLOGIES TO CONTINUOUSLY DELIVER ADVANCED, IMPACTFUL, AND SCALABLE SOLUTIONS.
- STATE OF THE ART WITH INDUSTRY 1ST SUPER CLAMP™ IN ULTRA-LOW CLAMPING VOLTAGE IN TRANSIENT VOLTAGE SUPPRESSOR (TVS).
- INDUSTRY 1ST: DOWNSIZING WITH COST EFFECTIVE SOLUTION, BI-DIRECTIONAL TVS IN SOD128 PACKAGE.
- INDUSTRY 1ST: MINIMIZATION OF 1.2KV SIC SCHOTTKY DIODE IN LOW PROFILE SURFACE MOUNT PACKAGE.

3. SUPPLY CHAIN RELIABILITY

- STABLE SUPPLY AND FAST DELIVERY WITH DIE BANK CONCEPT.
- MULTI-LOCATION MANUFACTURING SITES.
- GLOBAL LOGISTIC WAREHOUSES IN EUROPE, NORTH AMERICA, AND ASIA.

4. CUSTOMER SUPPORT & COLLABORATION

- APPLICATION SUPPORT, DESIGN CONSULTATION WITH FAE SUPPORT.
- FAST RESPONSE ON CUSTOMER SPECIAL PRODUCT REQUIREMENTS.
- STRONG COMMITMENT TO CUSTOMER SUPPORT AND SERVICE, EXEMPLIFIED BY GREAT DELIVERY TRACK RECORD DURING SUPPLY SHORTAGE.
- LONG TAIL DELIVERY AND SUPPORT OF LEGACY PRODUCTS, SUCH AS CONTINUED DELIVERY OF AXIAL LEAD PRODUCTS.

5. BRAND TRUST & PROVEN TRACK RECORD

- CERTIFIED SUPPLIER IN MAJOR ICE AND EV AUTOMOTIVE AND INDUSTRIAL CUSTOMERS.
- STABLE OWNERSHIP ALLOWS CONTINUOUS LONG-TERM INVESTMENTS. THIS HELPS US TO AVOID CUSTOMER SERVICE AND PRODUCT DEVELOPMENT INTERRUPTIONS, JUST TO ACHIEVE SHORT-TERM COST-CUTTING.

6. PRICING & COST COMPETITIVENESS

- CONTINUOUSLY BENCHMARK AGAINST MARKET WITH IMPROVE INTERNAL EFFICIENCIES THROUGH AUTOMATION, SMART OUTSOURCING, AND OPERATIONAL EXCELLENCE TO ENSURE COST-EFFECTIVE PRODUCT OFFERINGS.

TSC, Your Reliable Partner

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REFERENCES

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[2] - Robert Bosch GmbH: Wettable-Flanks: Enabler for The Use of Bottom-Termination Components in Mass Production for High Reliability Electronic Control Units, Udo Welzel, Marco Braun, Stefan Scheller, Sven Issing, Harald Feufel

[3] - ON-Semi: Application Note AND9657, Board Level Application Notes for Sawn Singulated DFN and QFN Wettable Flank Packages, March 2018, Rev.0

Q & A TIME

TAIWAN SEMICONDUCTOR