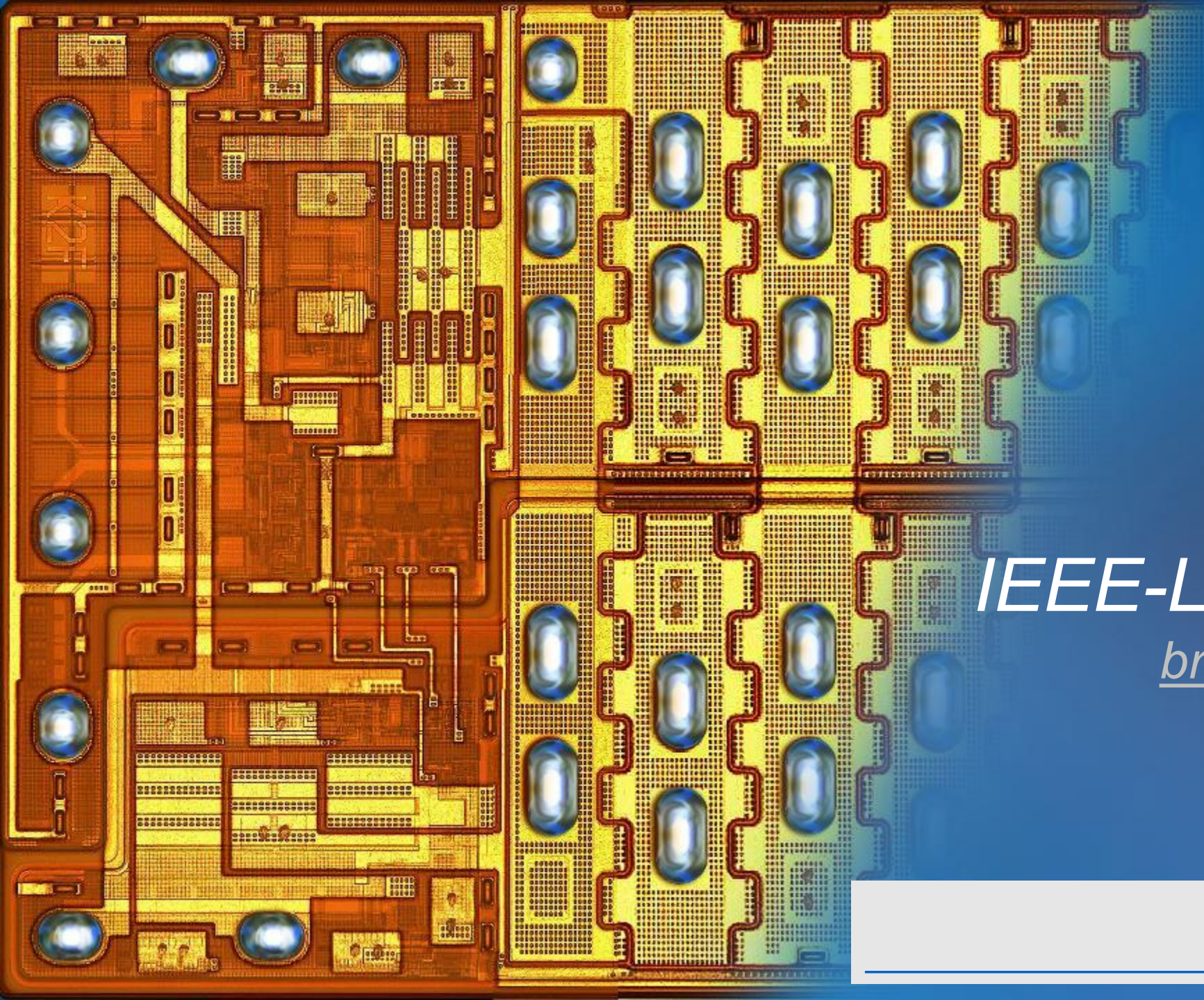


GaN at 125°C: Efficiency & Reliability

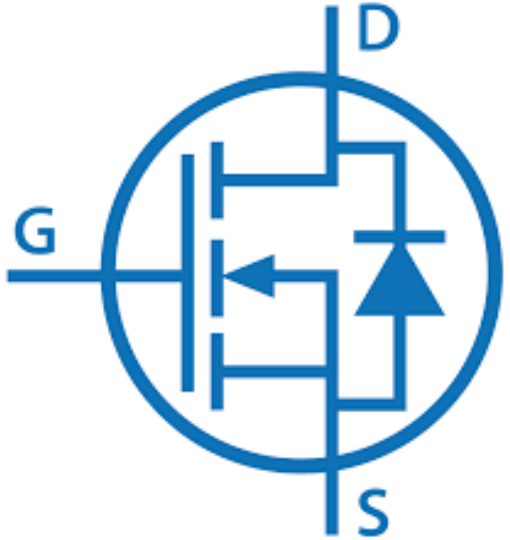
IEEE-Long Island 2025

brian.miller@epc-co.com

EFFICIENT POWER CONVERSION

Agenda: GaN @ 125 °C

- Review of GaN Power Devices
- Why focus on 125 °C?
- Efficiency Factors
  - Conduction Loss
  - Switching Loss
  - Deadtime Loss
- Reliability
  - Reliability vs Junction Temperature
- Summary

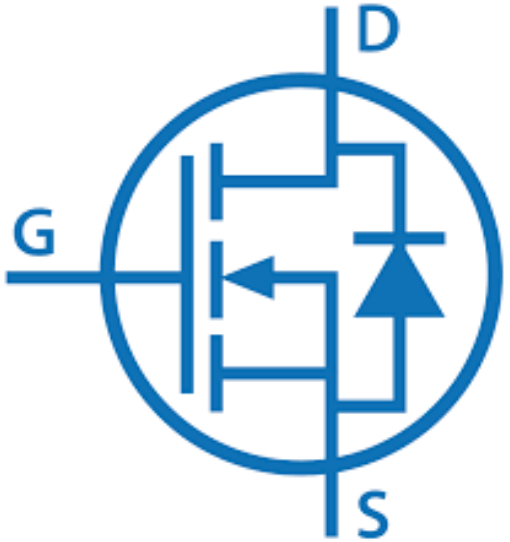


For PDH Credit:
www.ieee.li/forms/4491

Introduction

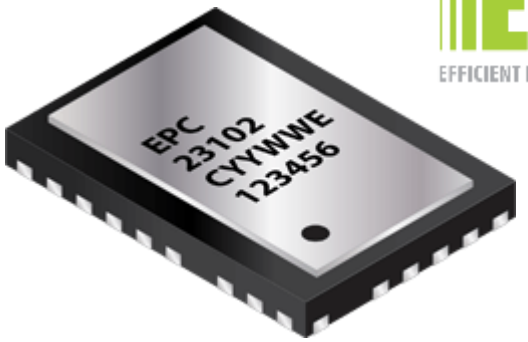
- Why use GaN FETs?

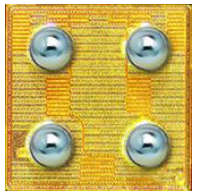
- Advantages vs. silicon MOSFETs:
  - Wide bandgap material GaN allows
    - Smaller FETs
    - Less weight
  - Fast, efficient switching
    - Power supplies can operate at higher frequencies
    - And/or: more efficiency
  - Thermally efficient: heat conducts very well
  - No reverse recovery
    - Because no parasitic PN diode
    - Diode function, but no reverse recovery

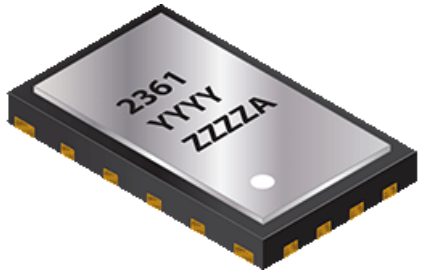


Review of GaN FETs

- Many suppliers of GaN FETs and ICs
- Voltage: 15 V to > 1.2 kV
  - 100 V as small as 0.9x0.9 mm
- Frequency: DC to GHz
  - RF GaN FETs were first:
    - depletion mode = normally ON
    - not popular for power FETs
  - Focus here: < 10 MHz power FETs
- Resistance:
  - 3 x 5 mm PQFN, 100 V: as low as 0.75 mΩ (typ)
- Gate Drive:
  - Typical: ON = 5V, OFF = 0V







Why look at 125 °C condition?

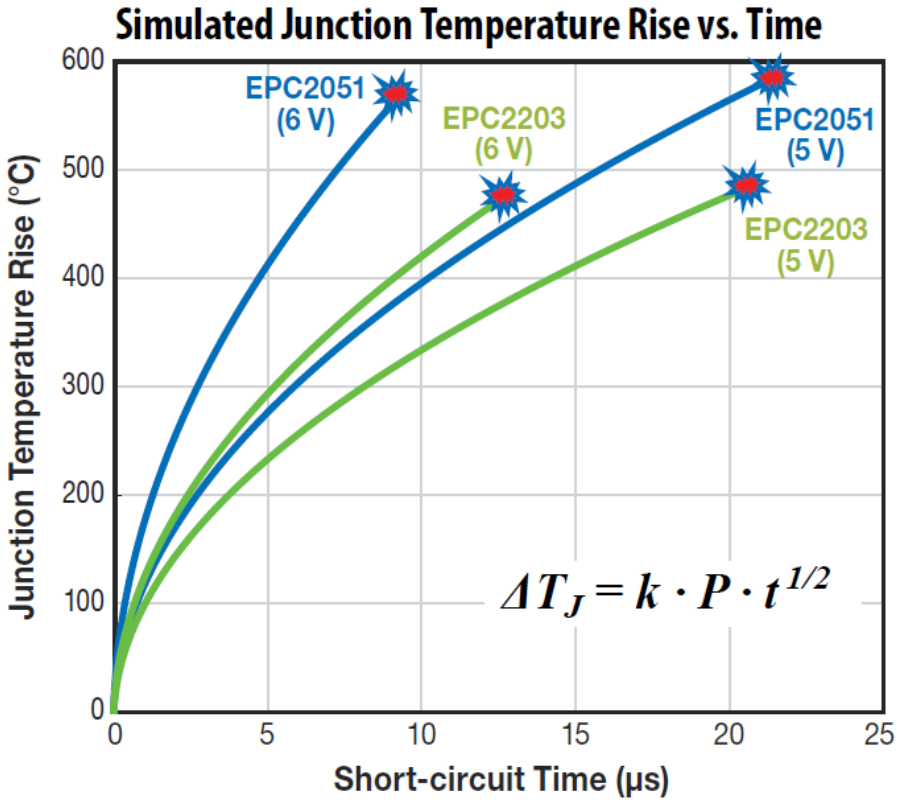
- A common top thermal design limit
  - 150 °C max – 25 °C margin = 125 °C
- 125°C junction temperature, not ambient!

- **Efficiency** at design thermal max (125 °C) is often a limiting factor
  - Due to thermal design
  - Different vs. efficiency at 25 °C
  - “Different” = lower efficiency
- **Reliability** at thermal max (125 deg. C) is often a concern
  - Due to experience with silicon MOSFETs

Why not above 150 °C?

- GaN is wide bandgap, and can remain a semiconductor at high temperatures
- > 400 °C

- But many/most suppliers don't use this ability. Why not?
  - Design trade-offs: lowest Rds,on vs. leakage
  - FR-4 boards temp rating ~ 130 °C
  - Solder may melt (lead 183 °C, lead-free 227 °C
  - EPC doesn't typically qualify above 150 °C
  - So: FETs designed for 150-175 °C max



Reference: EPC Reliability Report Phase 16, Fig. 3-20

Power Supply Efficiency

Loss Factors in DC-DC converters

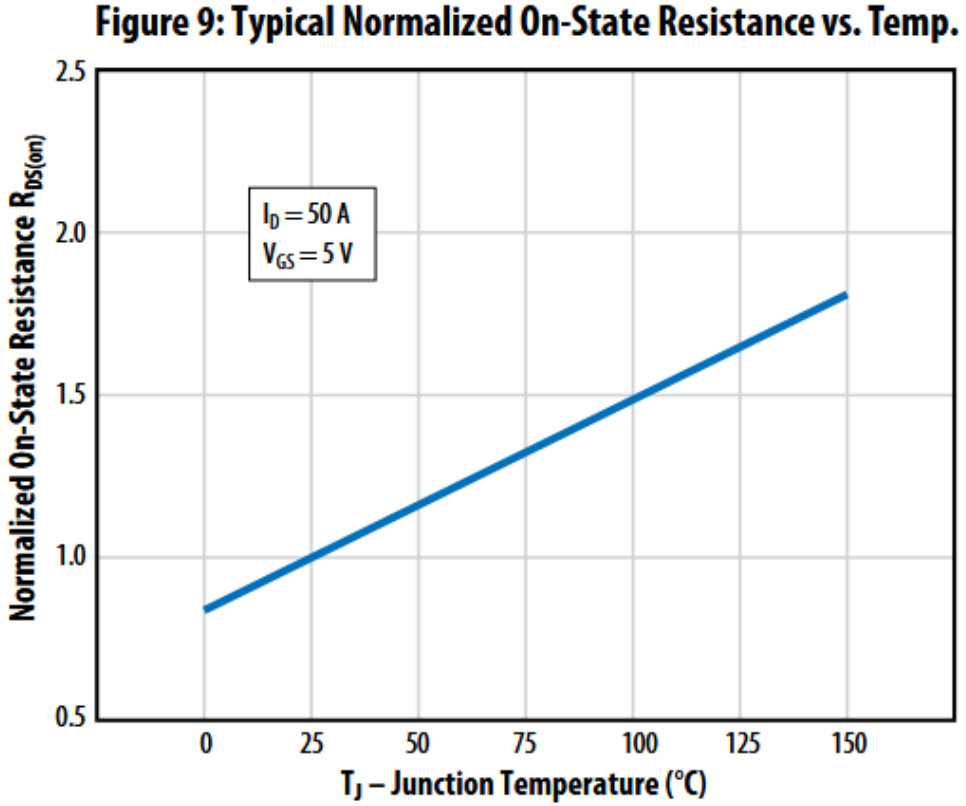
- Let's concentrate on DC-DC power supply designs
- Main losses:
  - Conduction Loss
  - Switching Loss
  - Dead Time Loss

- Other losses not covered include:
  - Gate Drive
  - PCB Loss
  - Layout-induced loss variation: Common Mode L, etc.

Conduction Loss

- Conduction loss seems simple
- Just look at the FET's on-resistance (Rds,on)! Right?
- Well… how does it change over temperature
- Depends on the FET

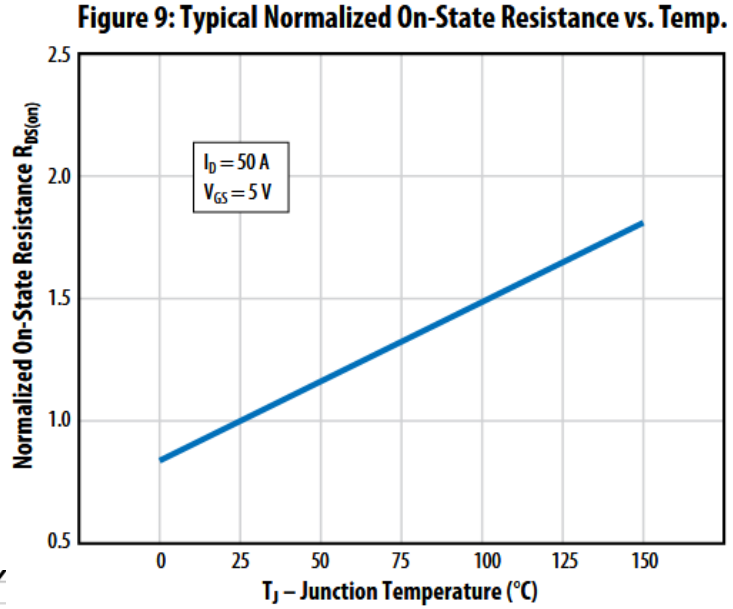
- Graph of Rds,on vs. Junction Temp
  - Normalized curves make it easy to calculate and compare



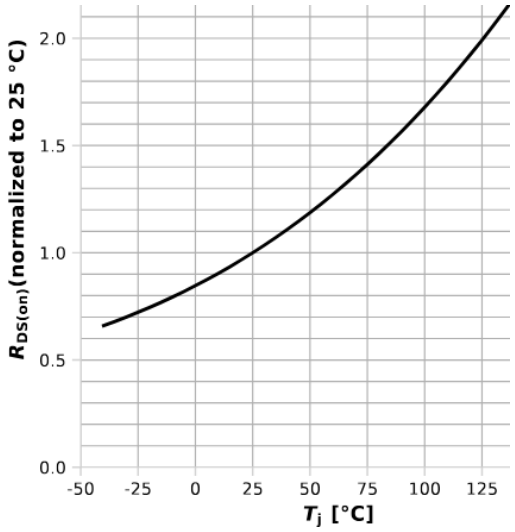
Conduction Loss Variation Examples

Let's look at larger, newer FETs
- Measure: 125°C Rds,on / 25°C Rds,on

- EPC's packaged FETs
  - EPC2361 100 V, 0.75 mΩ (typ), 3x5 mm: 1.7 x
  - EPC2366 40 V, 0.8 mΩ (typ) 3.3x2.6 mm: 1.55 x
  - EPC2304 200 V, 3.5 mΩ (typ): 1.65 x
  - EPC2050 350 V, chip scale: 1.75 x
- MOSFET: 100 V Infineon Optimos 6:
  - ISC022N10NM6: 1.7 x
- Infineon GaN:
  - IGC033S10S1: 100 V: 2 x
  - 60 V, 200 V: 2 x
  - 650 V: 1.9 x (IGL65R140D2)
- TI GaN 650 V: 1.75 x
- Navitas 650 V, NV6128C: 2 x



EPC2361: 100 V
0.75 mΩ typ., 3x5 mm

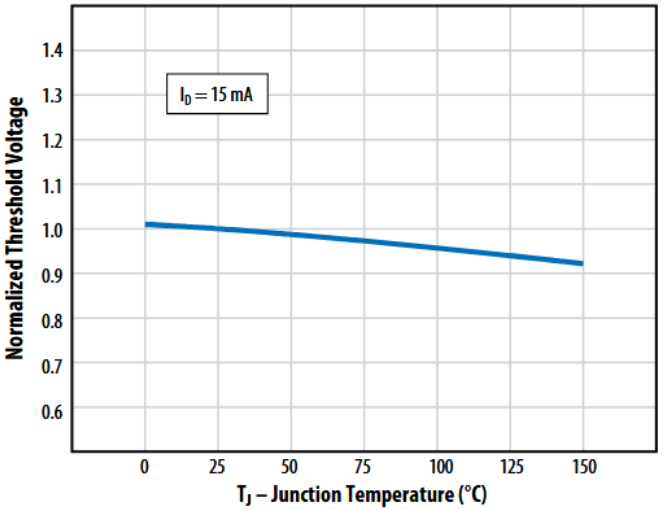


IGC033S10S1: 100 V
x mΩ typ., 3x5 mm

Switching Loss

- Switching Loss:
  - minimize loss with fast switching
- Parameters:
  - Capacitance not typically characterized at 125 °C
  - Gate Threshold Voltage is given
- Examples:
  - Top: EPC2361
  - Bottom: EPC2016 (obsolete FET): threshold *increases* with temp
  - Same for Infineon 100 V →
  - < 10% change for all
  - MOSFETs: -20 to -30% change

Figure 10: Typical Normalized Threshold Voltage vs. Temp.



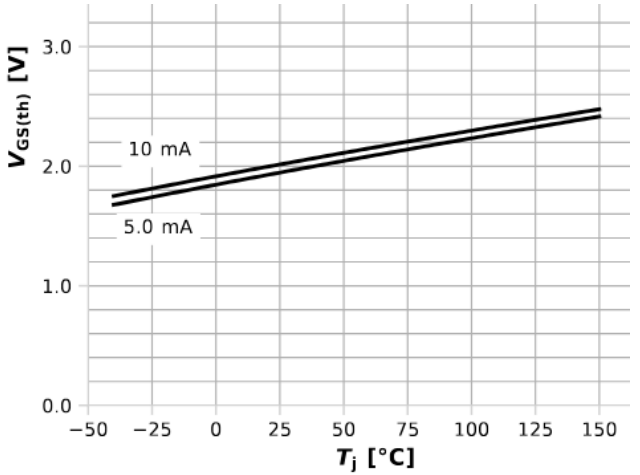
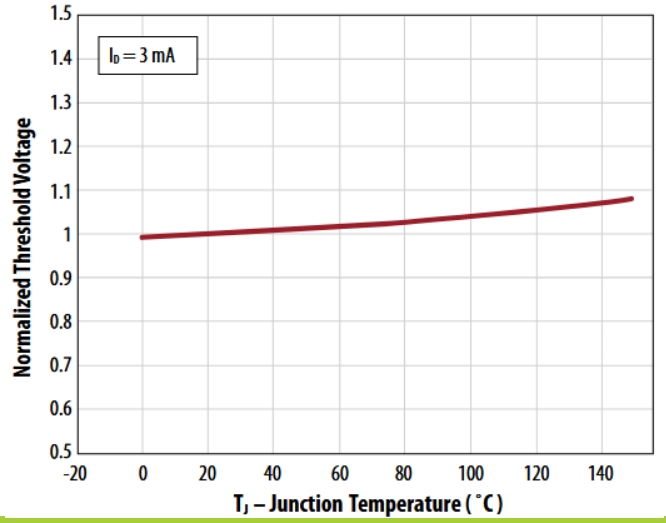


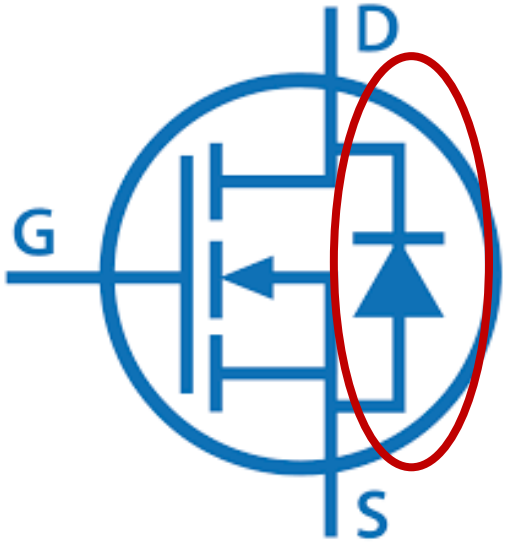
Figure 9: Normalized Threshold Voltage vs. Temperature

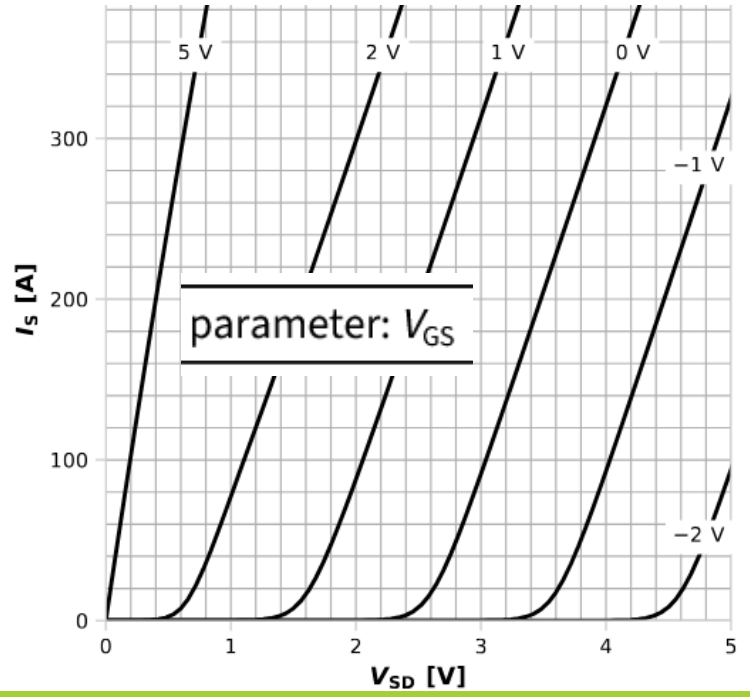


Dead Time Loss

- Vsd, Reverse conduction “Diode” Loss
  - Not a parasitic PN diode, as in MOSFETs
  - Conduction is through the main channel
- Dead Time Loss is easy to calculate
  - P = Vsd * I * Tdt * Freq.
- Parameter Vsd:
  - increases with Temperature
  - decreases as Vgs goes up
  - Increases as Vg,th goes up

- *Plot: from Infineon IGC025S08S1 data sheet*





Dead Time Loss

- Vsd (“diode” drop):
  - **Temperature**: increases with Temperature
    - Channel resistance goes up with temperature
  - **Gate Threshold**: Decreases if Vg,th decreases
    - So, ideally Vg,th will decrease with increasing voltage
  - **Current**: increases with current

- Putting it all together: data sheet curves

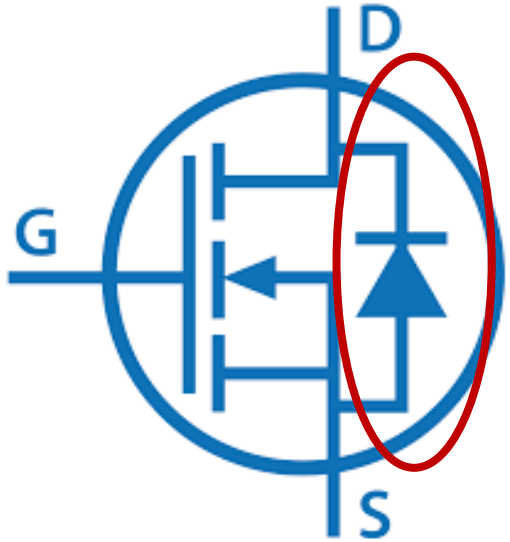
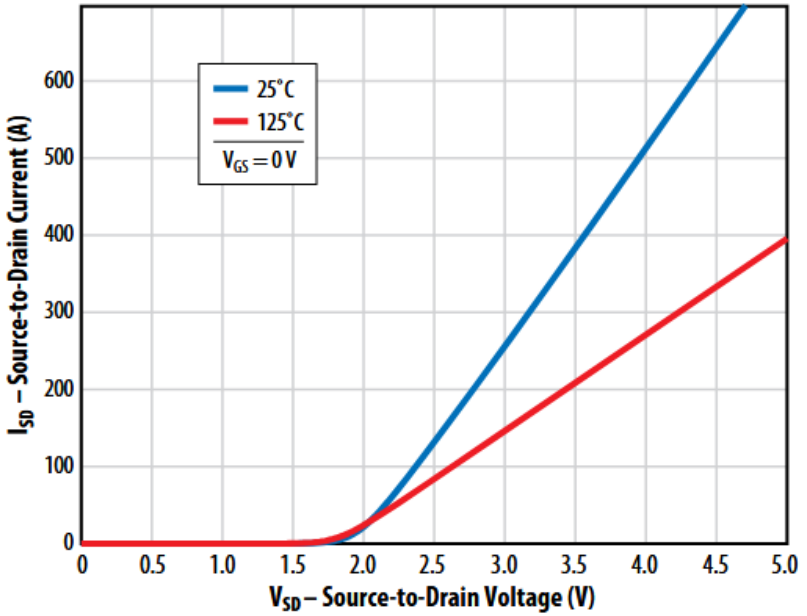


Figure 8: Typical Reverse Drain-Source Characteristics*

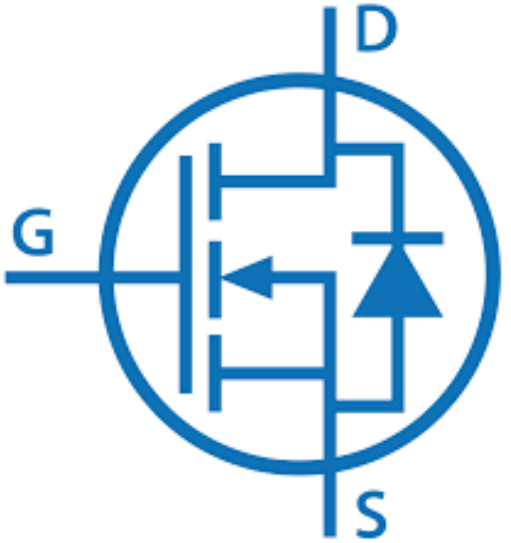


Note: Negative gate drive voltage increases the reverse drain-source voltage. EPC recommends 0 V for OFF.

Dead Time Loss

- Dead Time Loss is easy to calculate
  - P = Vsd * I * Tdt * Freq.

- To Minimize Dead Time:
  - Zero Dead Time controller:
    - examples: ADI's LTC7890, -91
  - Gate Driver: propagation time matching
    - To minimize dead time safely
    - Not all half-bridge gate drivers have the same propagation time matching specs



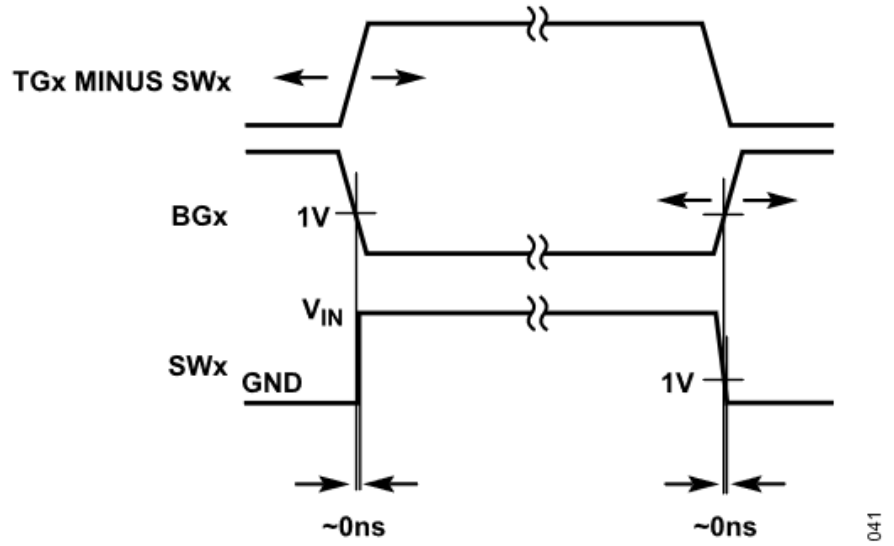
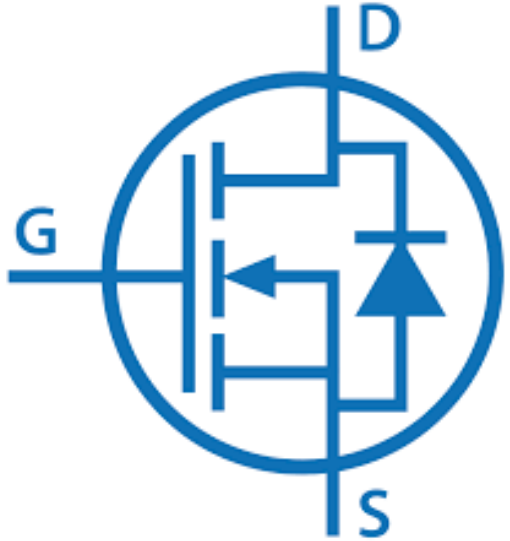


Figure 41. DTCx Pins Tied to $INTV_{CC}$—Smart Near Zero Dead Time Control

Reliability

Reliability Background

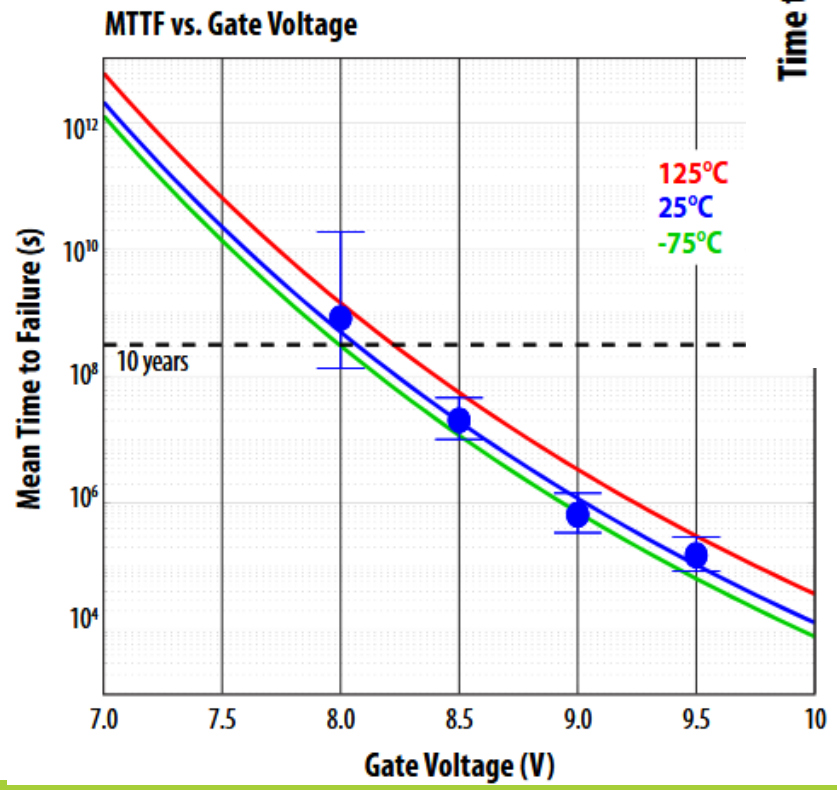
- Most engineers' experience starts with Silicon MOSFETs
- "everyone knows": as Temperature goes up, Reliability goes down
- How about GaN FETs
  - How do they fail?
  - How bad is the situation at 125 °C?



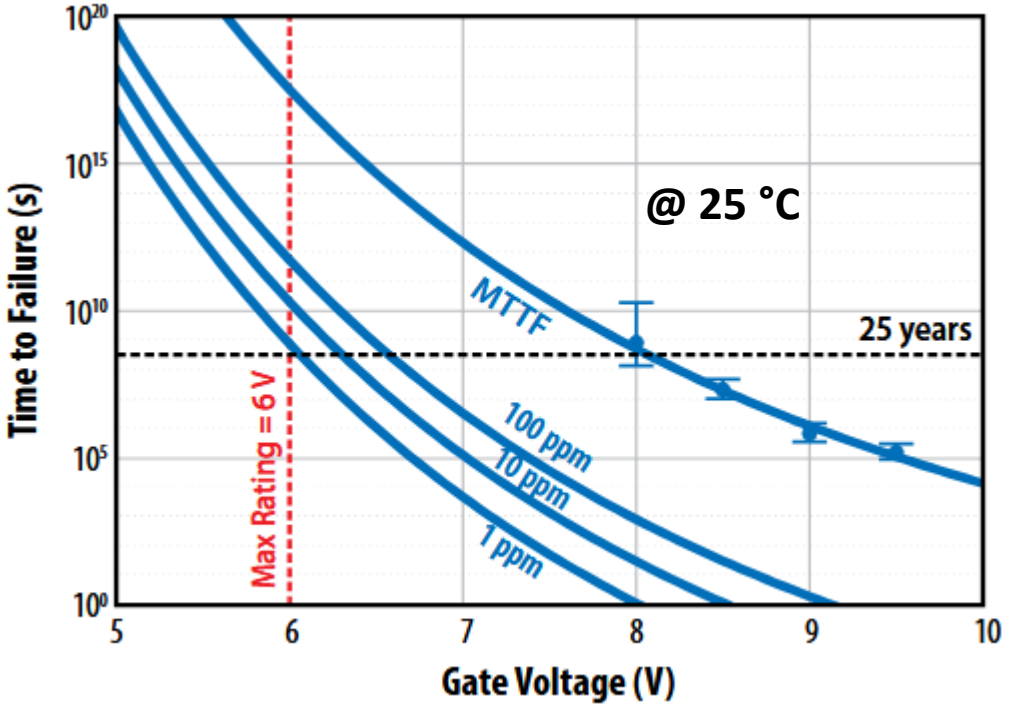
Gate Reliability (EPC GaN FETs)

- Various GaN FETs have different gate structures
- EPC info. shown here
  - Absolute max = 6 V
- What about 125 °C?
  - Red line = 125 °C
  - Slightly *better*
  - Worst-case -75 °C

- *Phase 17 has most recent update, section 4.1.2*



Reference: EPC Reliability Report Phase 16, Fig. 3-3



Reference: EPC Reliability Report Phase 17, Fig. 4-2

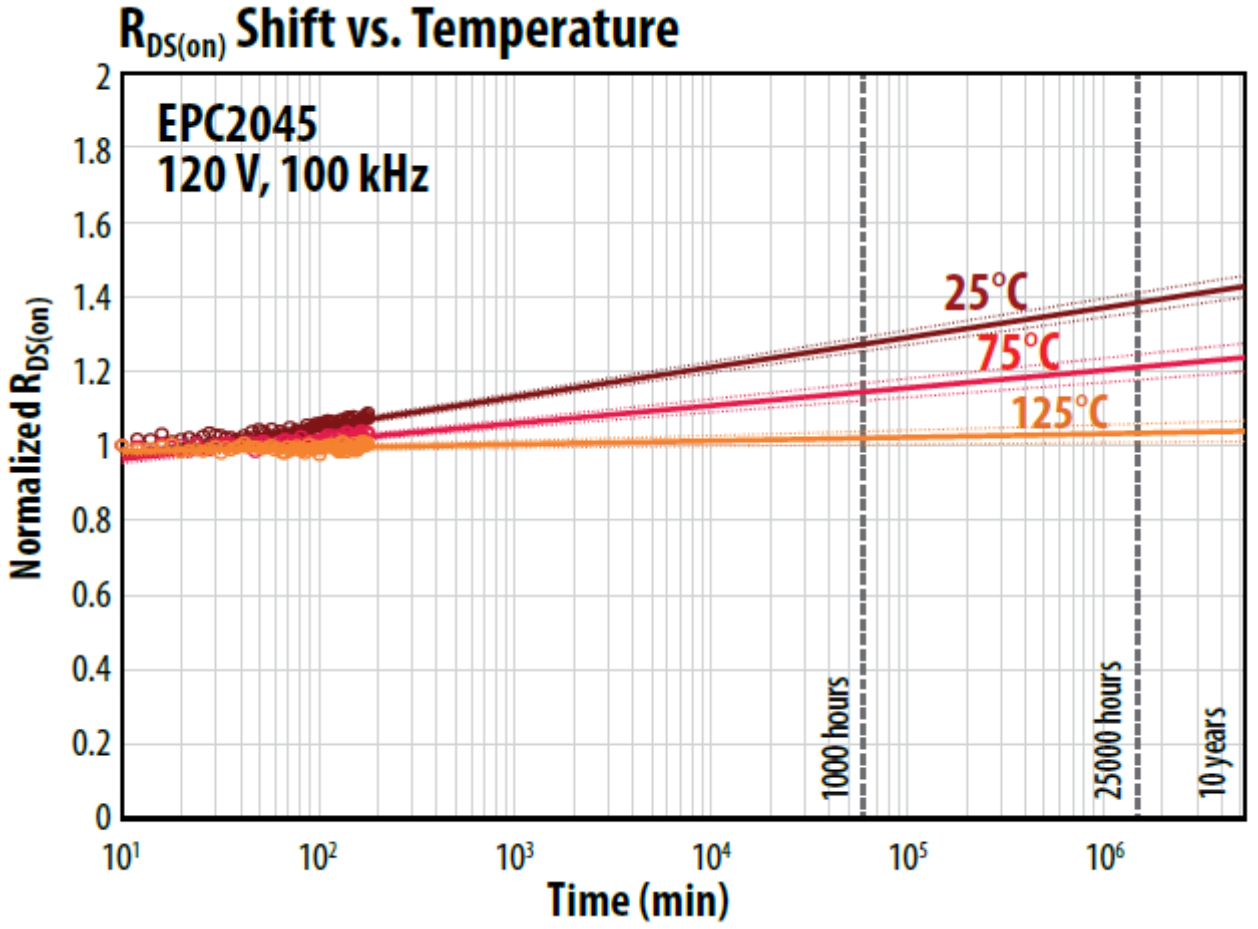
What is a Drain-Source FET Failure?

- Seems obvious: FET doesn't function

- But long term reliability is mostly less dramatic:
  - No longer meets data sheet limits
  - Rds,on specifications; slow increase in Rds,on
  - When above max. limit = failure
  - Typical is 20% increase

Example Plots (Drain-Source)

- Run a 100 V-rated FET at 25 °C
  - **120 V**, **100 V**, **80 V**, **60 V**
  - **120 V**: To accelerate the slow increase of Rds,on
  - And to show no catastrophic failure just above 100 V
- Now, run the test at various temperatures (still 120 V)
  - Surprising! For this condition:
  - **25 °C** has the shortest lifetime
  - **75 °C** is better
  - **125 °C** is best



Reference: EPC Reliability Report Phase 16, Fig. 3-6

Reliability Details

- GaN FETs are more reliable at 90 °C vs. 25 °C
- Why is this?
- 2 factors
  - One factor *decreases* reliability with rising temp
  - The other factor *increases* reliability with rising temp
  - Non-linear
  - Combine to create a peak
- Practical aspects
  - Reliability testing: MOSFET test at high temp
  - GaN FETs: perhaps test at low temp?

- *Reference: EPC Reliability Report Phase 16*

Summary

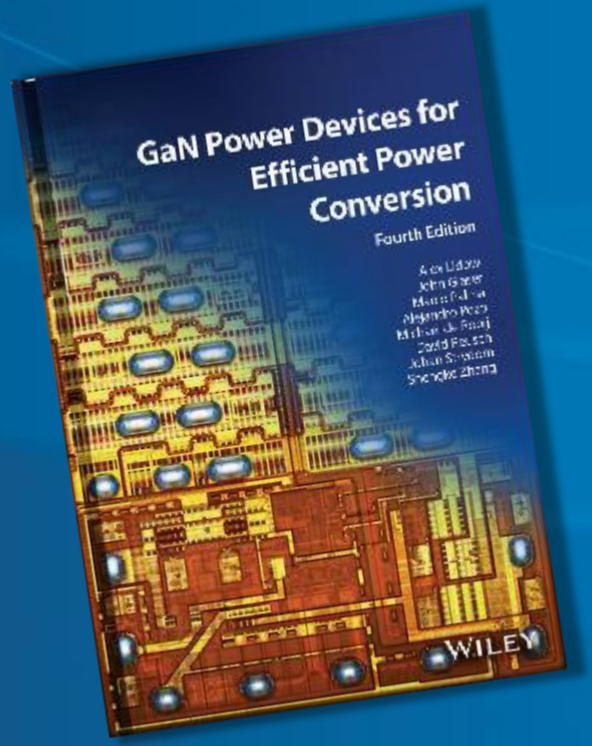
- 125 deg. C is OK for GaN FETs
- Efficiency:
  - Look for specified parameters
  - Efficiency loss can be minimized
- Reliability
  - Unexpected good news: GaN FET reliability is very good at elevated junction temperature
  - Studies and plots
  - Experimental peak survivable temperatures

- *GaN FETs: reliable and relatively efficient at 125 °C*

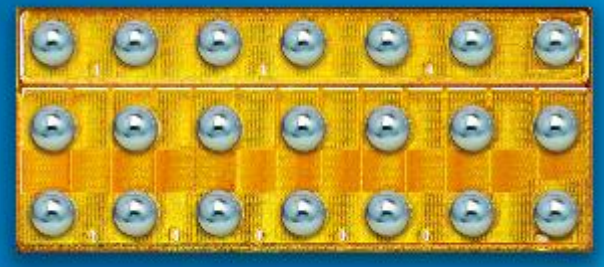
EFFICIENT POWER CONVERSION

Click on images to learn more

How To GaN Video Series

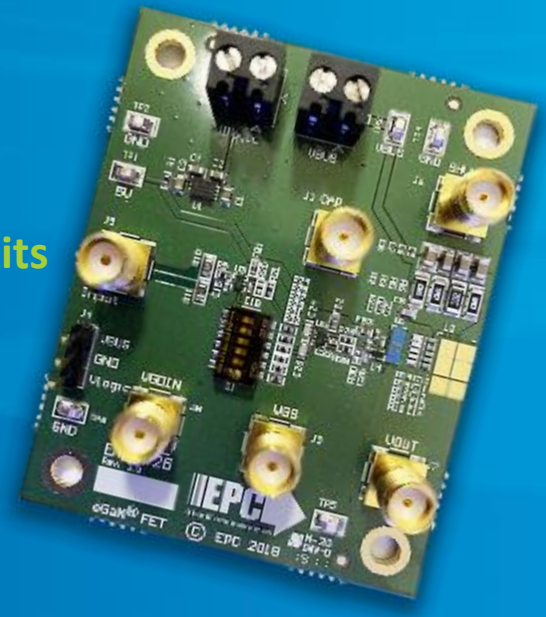


4th Edition Textbook



eGaN® FETs and ICs

Evaluation Kits



epc-co.com