Create Robust Circuit and System Designs with Advanced Techniques

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Design Process with Massive Benefits

What is a Robust Design?

- Design that works no matter what
- First pass success
- Insensitive to process variation
- Insensitive to external factors
- Low variability (consistency)
- High performance; High yield

Agenda

1. Introduction
   - Examples of “DOE based” Robust designs
     - *X-Band MMIC amp*
     - *K Band up converter macro cell*
2. Low variability / “Robust Design Methodology”
3. Design of Experiments (DOE)
4. System Level Examples
   - *DOE on system tray with cascaded modules*
   - *“DOE and Yield Sensitivity Histograms on a MMIC Power Amplifier*
5. Success Story - Dual Band HBT PA (Skyworks)
6. Conclusion

Tools in ADS Pinpoint Design Yield Problems

Design of Experiments (DOE)

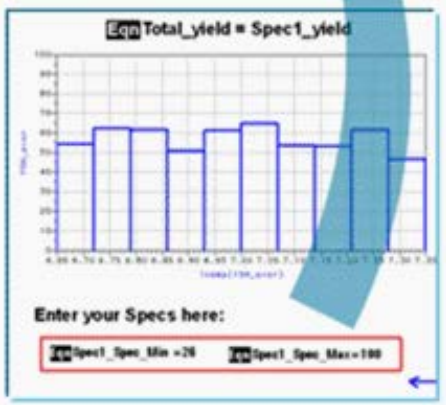
Yield Sensitivity Histograms (YSH)

DOE detects
- Sensitive components
- Sensitive matching networks
- Interactions problems

YSH detect
- Sensitive components
- Sensitive Specs - YSH allows for Specs trade-off study without having to re-perform yield analysis

Pinpoint the problem & fix it

W	R	C	Gain
-1	-1	-1	12.85
1	-1	-1	13.01
-1	1	-1	14.52
1	1	-1	14.71
-1	-1	1	12.93
1	-1	1	13.09
-1	1	1	14.61
1	1	1	14.81



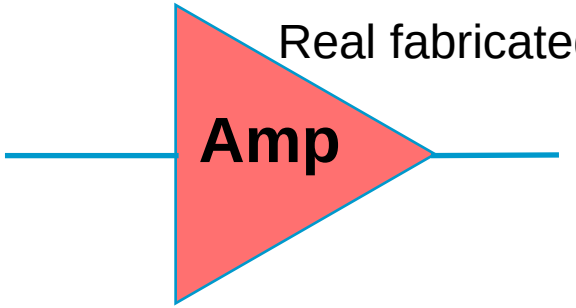
Design of Experiments (DOE)

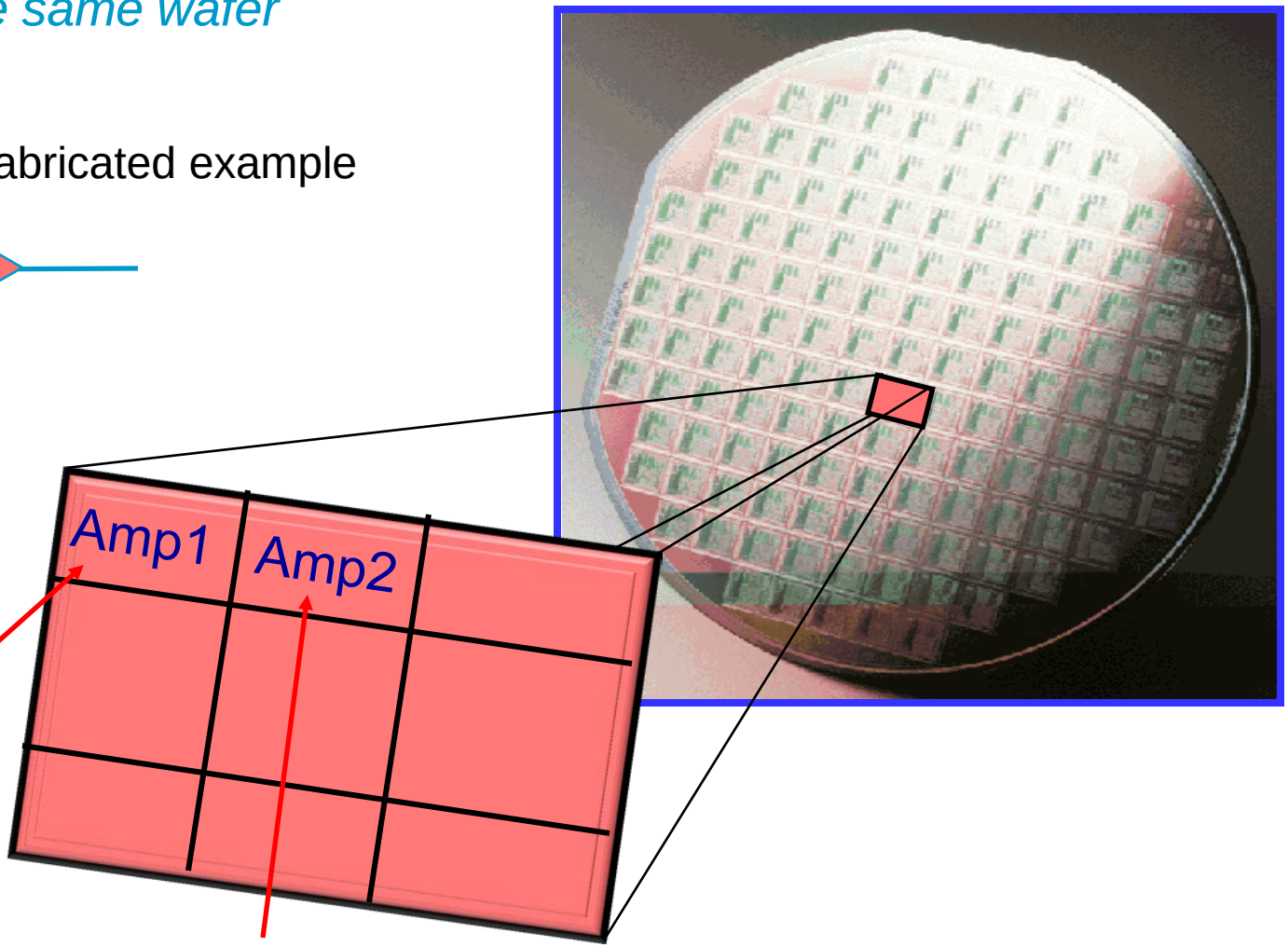
Yield Sensitivity Histograms

Two MMIC X-band Amplifiers

Fabricated on the same wafer

Real fabricated example





1) Used a standard design technique

2) Used a robust Design of Experiments (DOE) based design technique

Real MMIC Designs

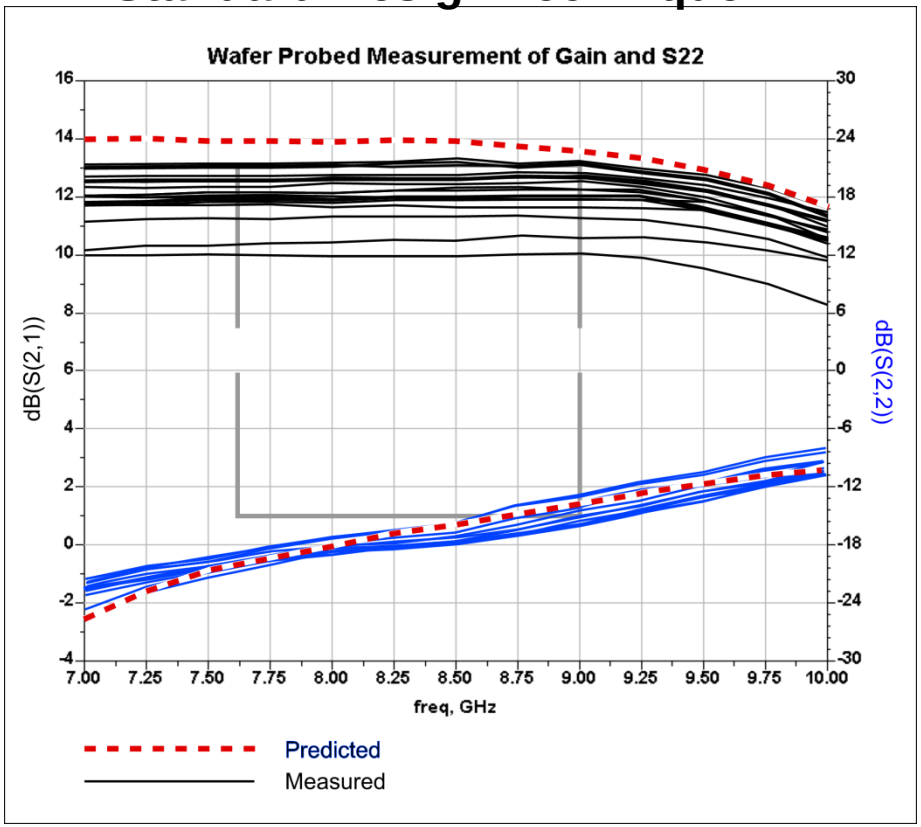
Fabricated on the same wafer – Wafer Probed Results

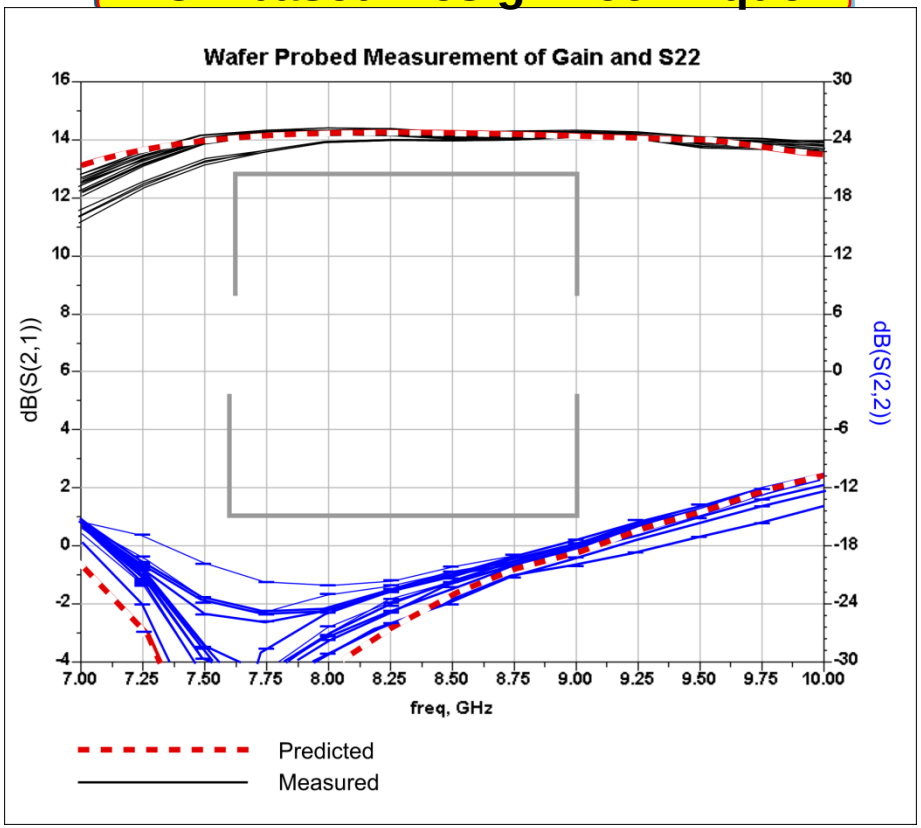
Amp1

Amp2

Standard Design Technique

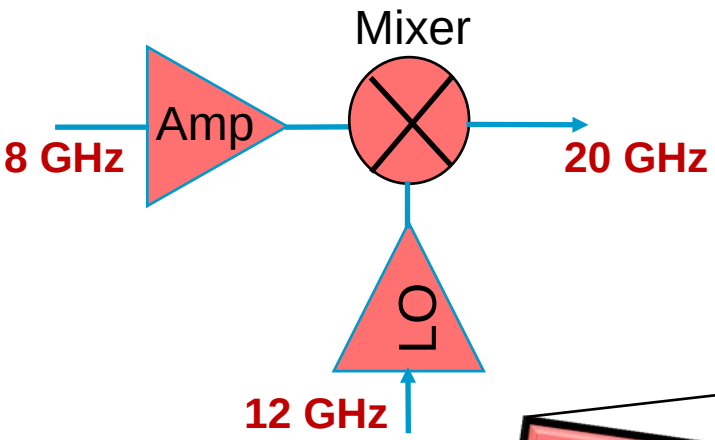
DOE based Design Technique

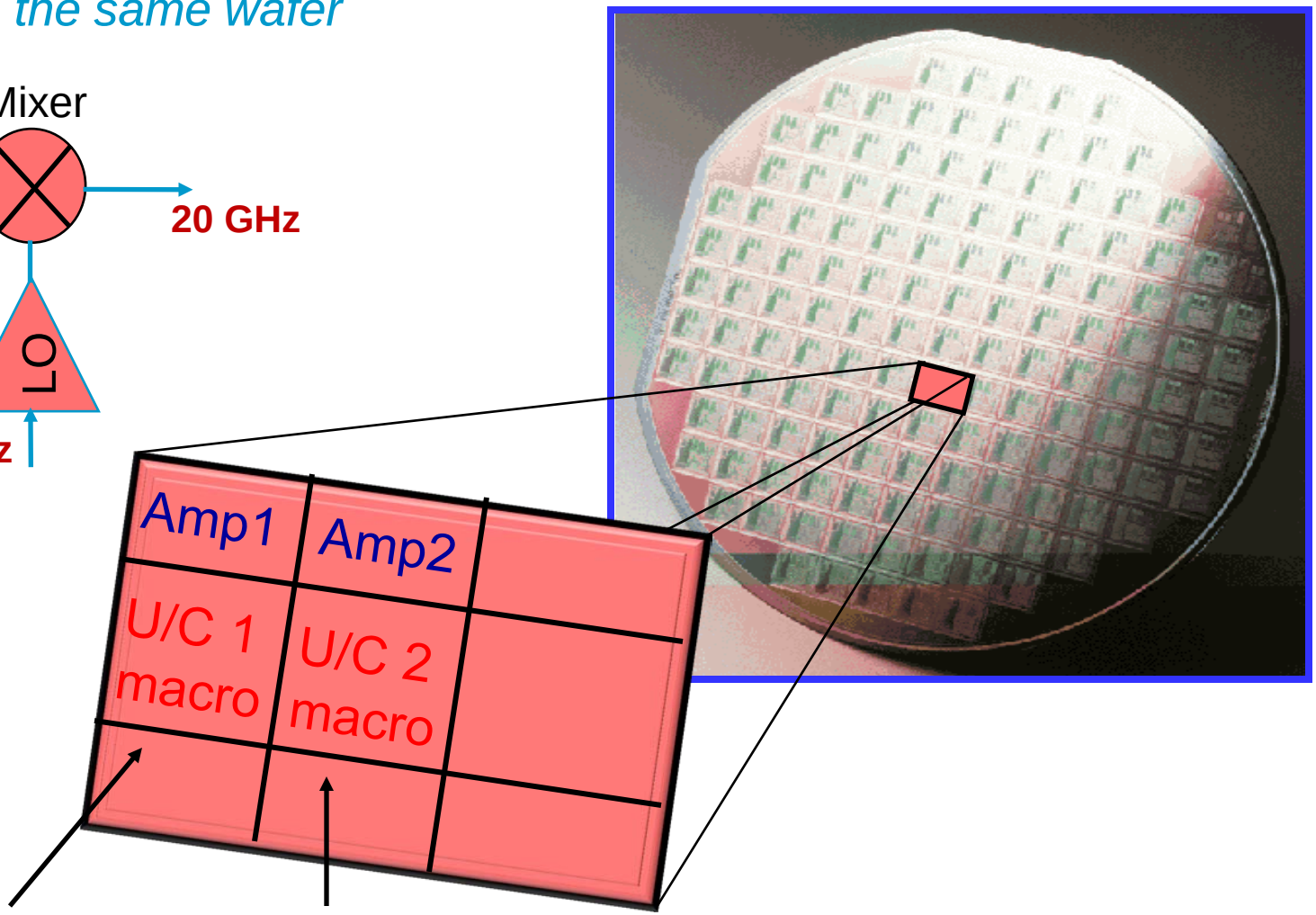




Two MMIC Up Converter Macro-cell Designs

Fabricated on the same wafer



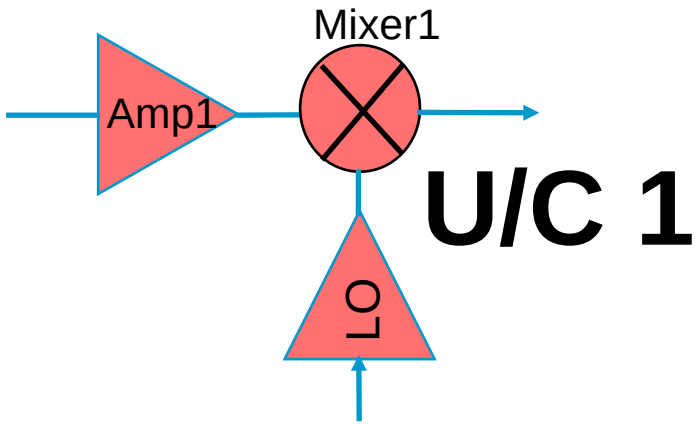


1) Used a standard design technique

2) Used a robust Design of Experiments (DOE) based design technique

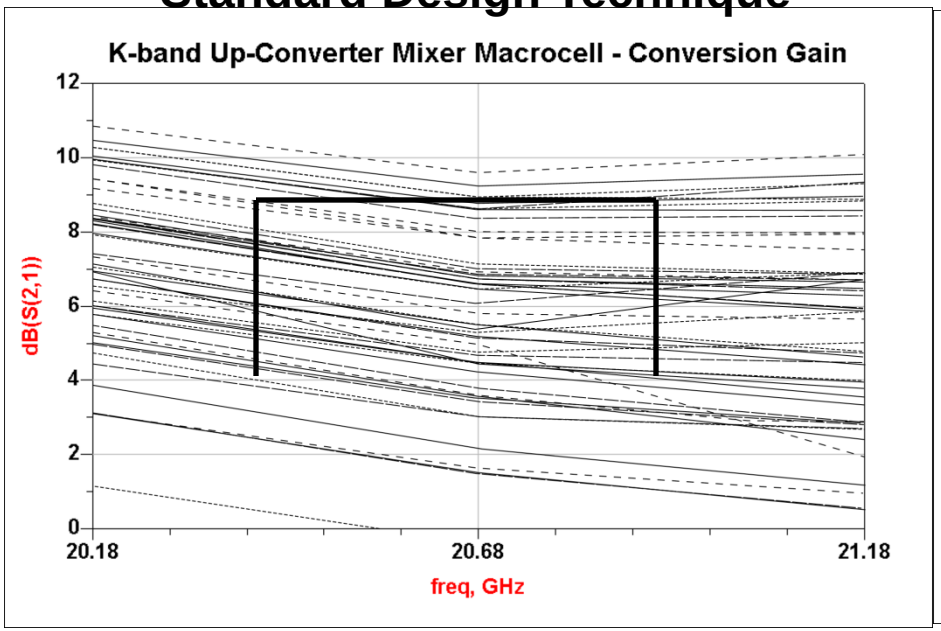
Two MMIC Designs

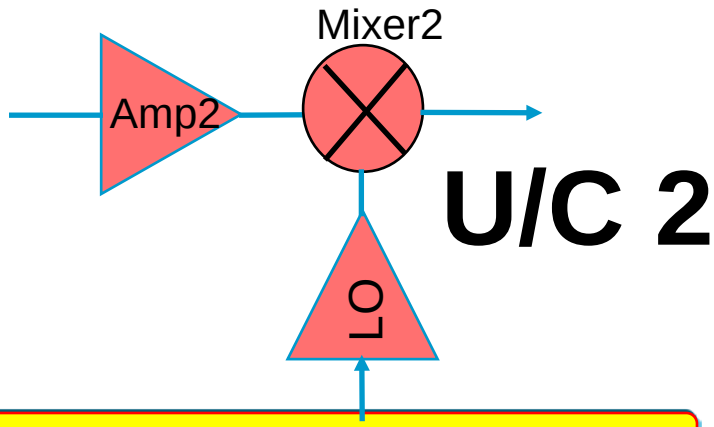
Fabricated on the same wafer – Wafer Probed Results



U/C 1

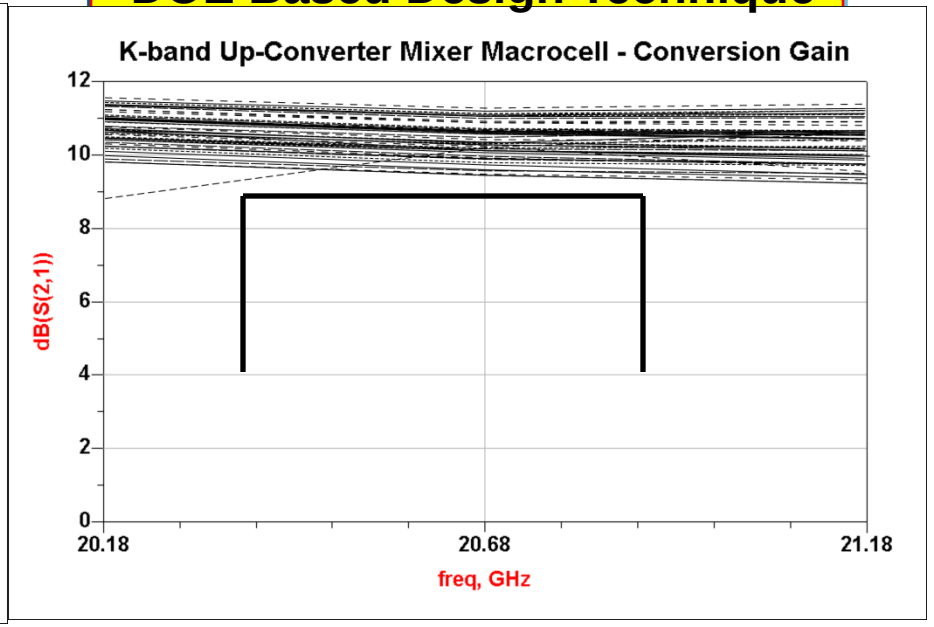
Standard Design Technique





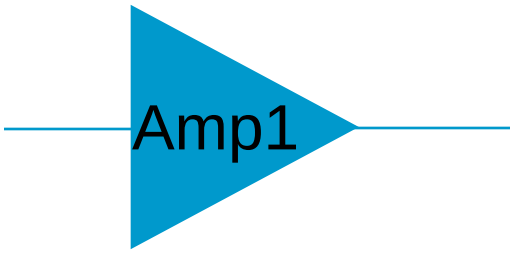
U/C 2

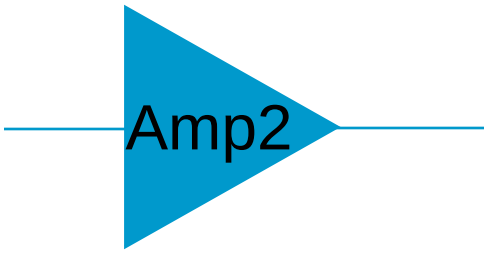
DOE Based Design Technique

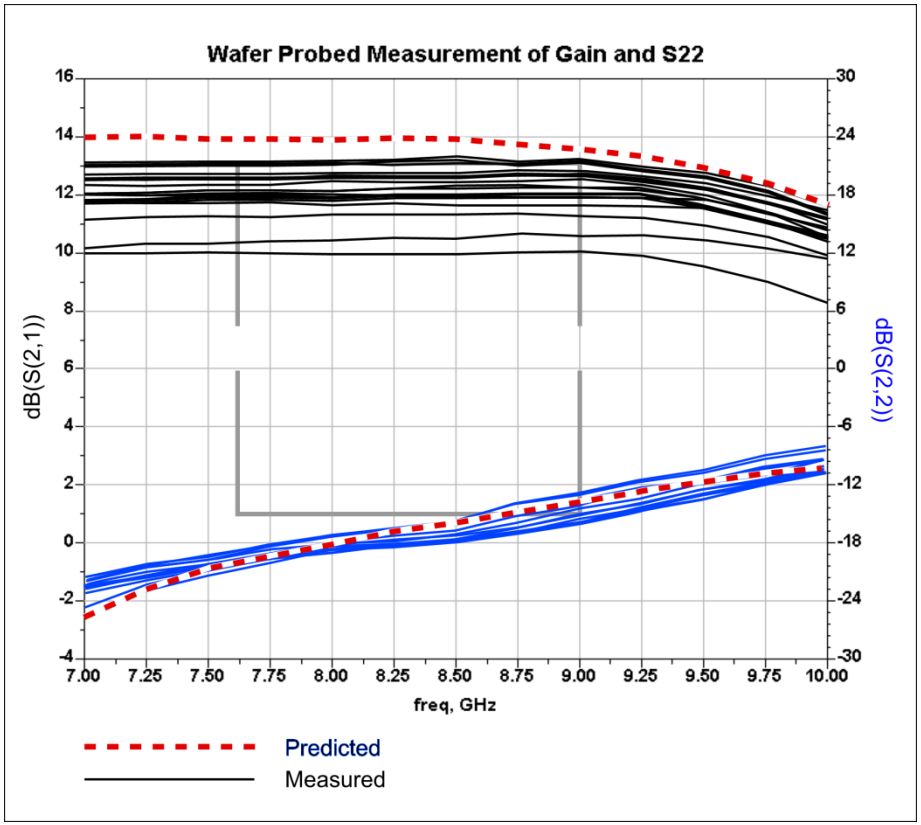


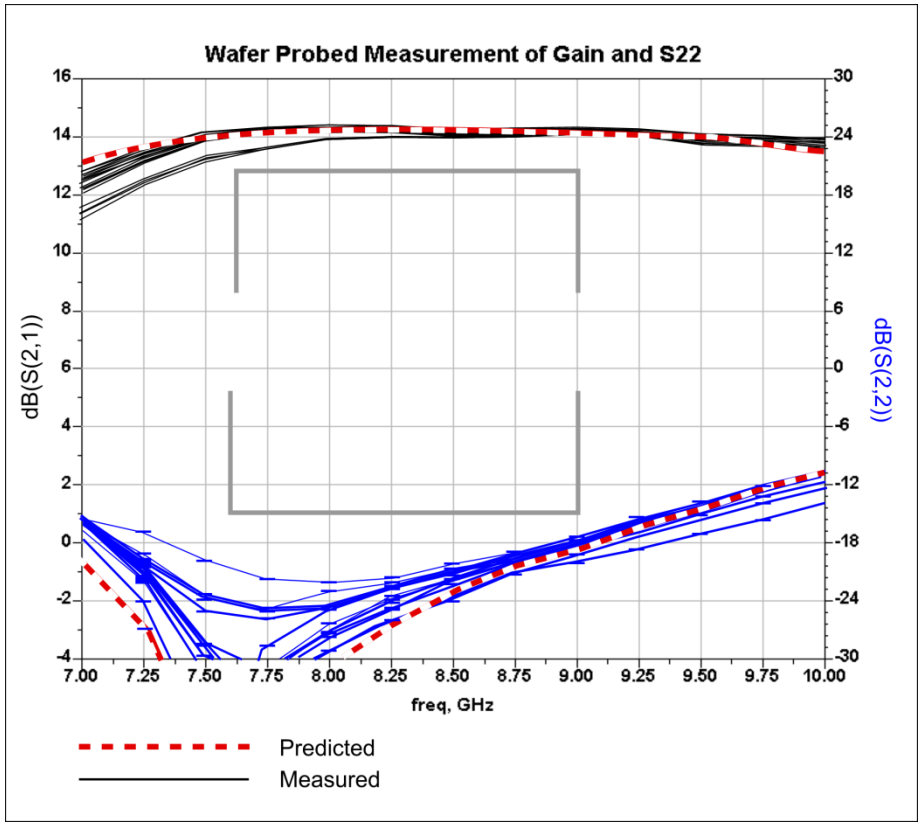
Understanding the Difference in the Results

Amp2 has a Narrower Process Yield Curve

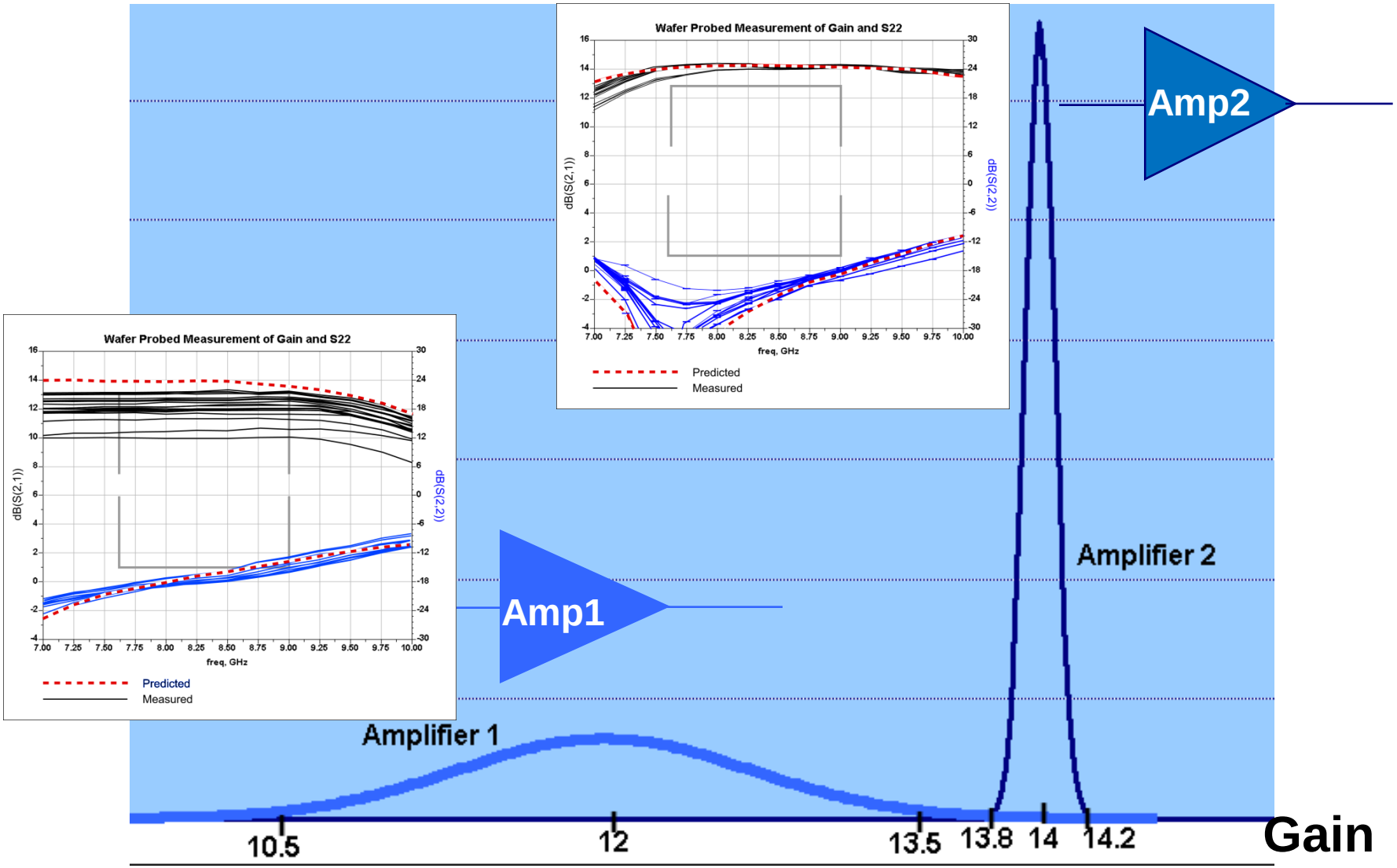








Amp1 & Amp2 "Yield Distributions"



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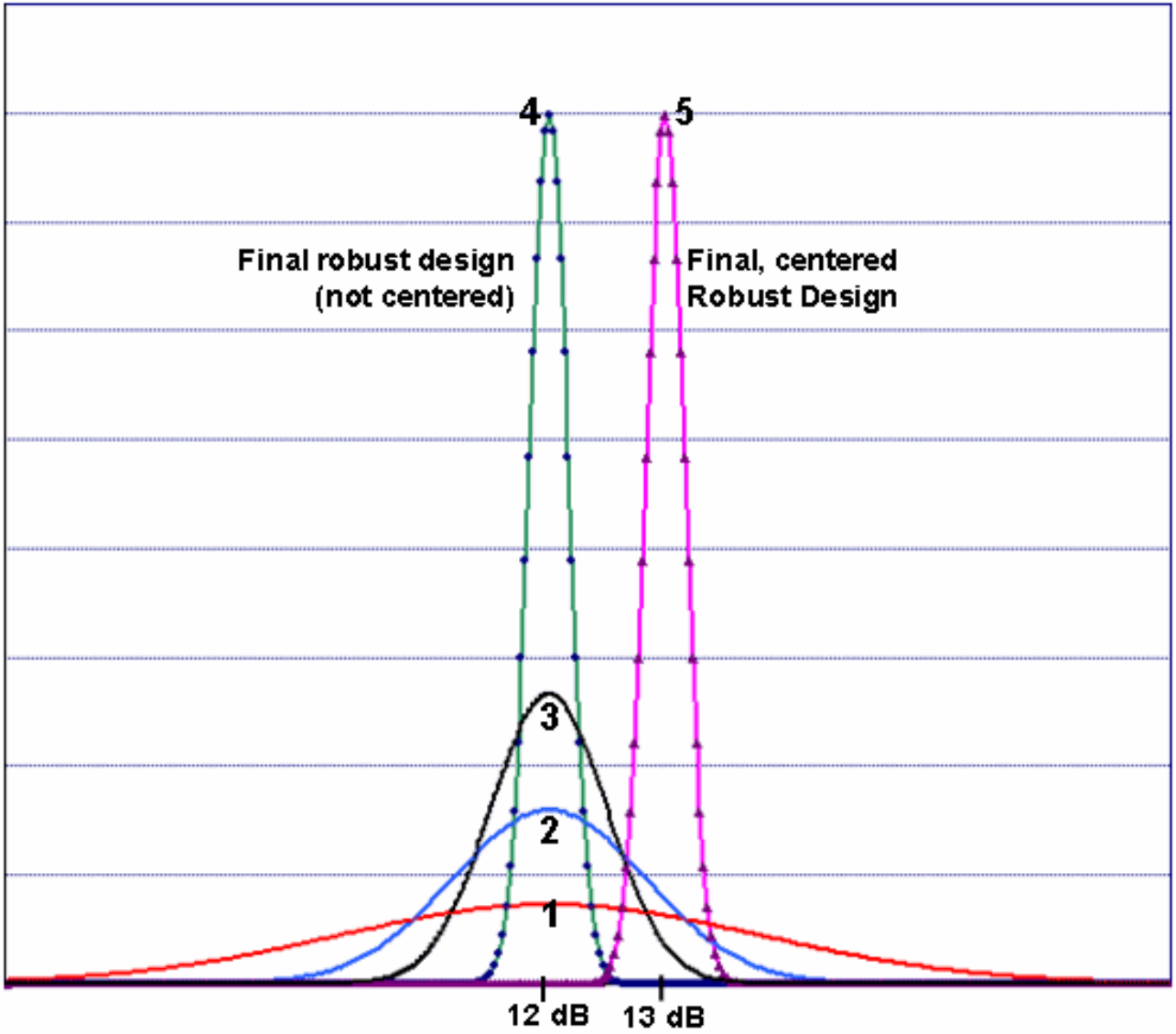
Design Process for Robustness



Curve 1
Initial Design

Curve 2
Fixing problem #1 to achieve Robustness

Curve 3
Fixing problem #2 to achieve Robustness

Curves 4
Further improvement towards achieving Robustness

Curve 5
Finally shift the Response meet Specs by using Design Centering

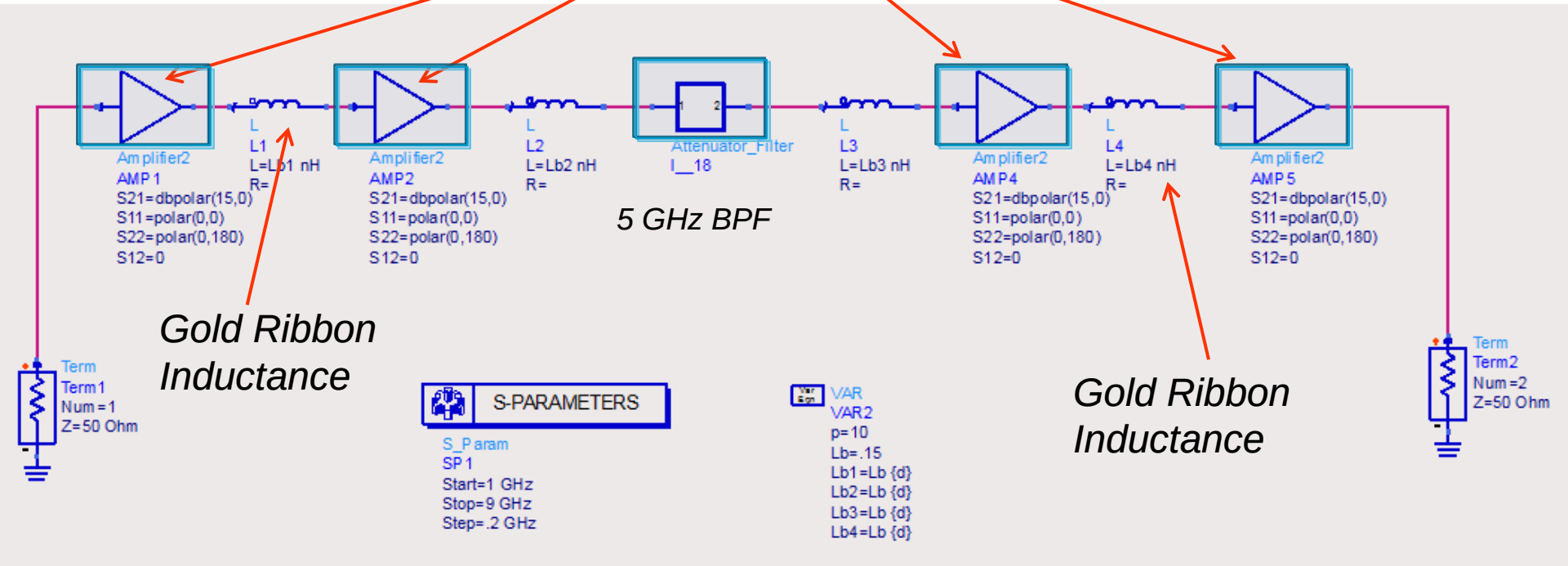
Design of Experiments
A Quick Overview

Using a System-Level Example

Explaining How DOE Works

System with 50 ohm cascaded modules

C-band Amplifiers

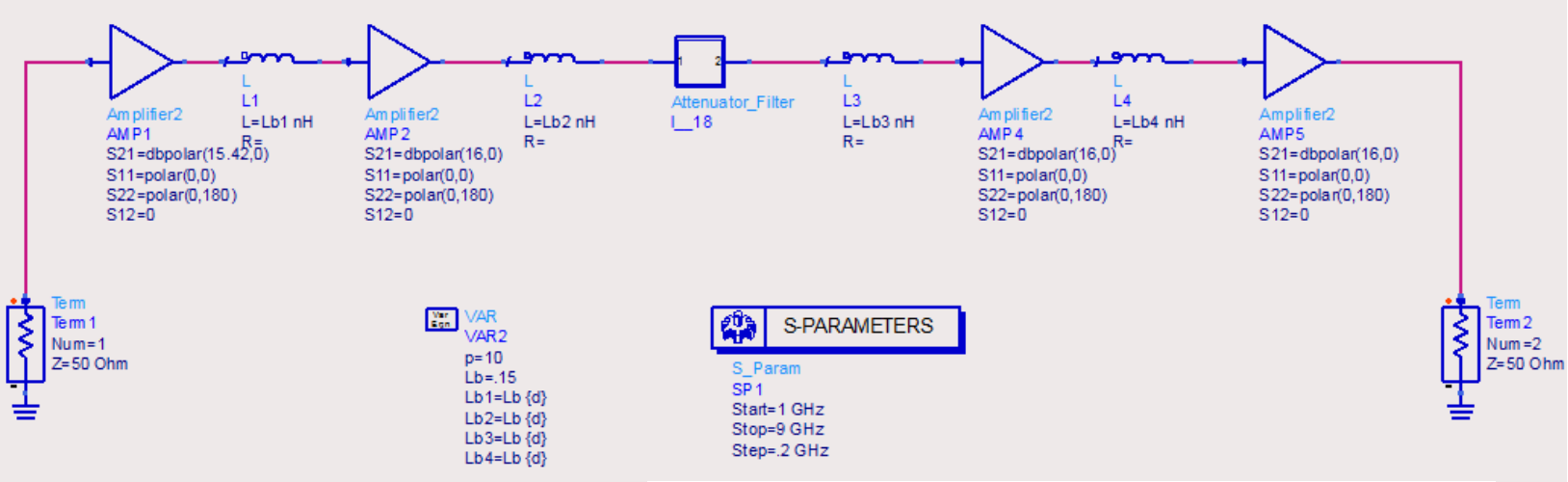


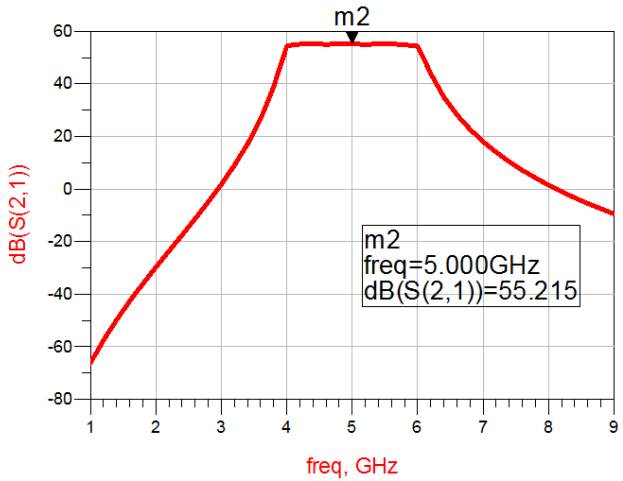
Gold Ribbon Inductance = .15 nH +/- 10%

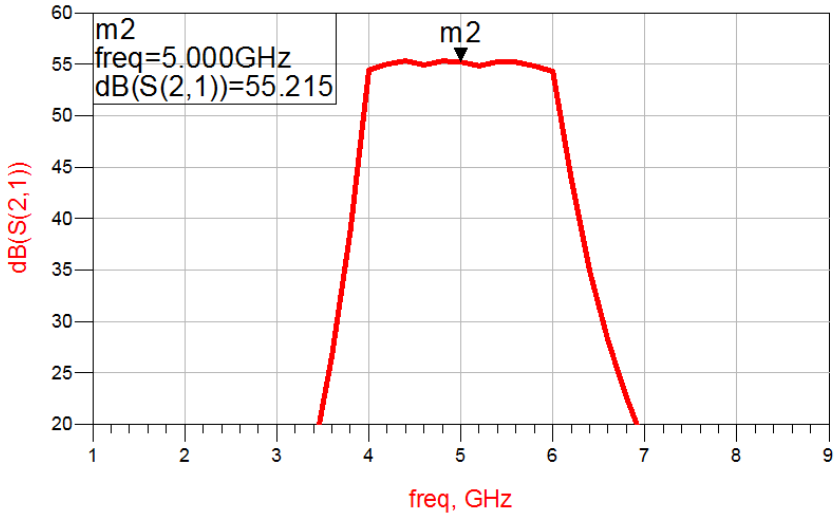
Bond wires Nominal Value – Gain=55.2 dB

50 ohm cascaded modules

4 variables that could affect the output:
Bond wires L1, L2, L3, L4







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Vary the Four Bond Wires +/- 10%

Cover all combinations - 16 experiments

Bond wire Inductance = .15 nH +/- 10%

L1	L2	L3	L4	Gain
0	0	0	0	55.215
-1	-1	-1	-1	59.24
1	-1	-1	-1	59.2
-1	1	-1	-1	58.44
1	1	-1	-1	58.4
-1	-1	1	-1	52.36
1	-1	1	-1	52.16
-1	1	1	-1	51.72
1	1	1	-1	51.6
-1	-1	-1	1	58.84
1	-1	-1	1	58.76
-1	1	-1	1	58.08
1	1	-1	1	58.04
-1	-1	1	1	52.04
1	-1	1	1	51.88
-1	1	1	1	51.4
1	1	1	1	51.28

Run 16 experiments
2^4 variables = 16

<u>Bond wire inductance value</u>
0 nominal value = .15 nH
-1 nominal –10% = .135 nH
+1 nominal +10% = .165 nH

Determining Variation due to L4 Only

Effect of bond wire inductance L4

L1	L2	L3	L4		Gain
0	0	0	0		55.215
-1	-1	-1	-1		59.24
1	-1	-1	-1		59.2
-1	1	-1	-1		58.44
1	1	-1	-1		58.4
-1	-1	1	-1		52.36
1	-1	1	-1		52.16
-1	1	1	-1		51.72
1	1	1	-1		51.6
-1	-1	-1	1		58.84
1	-1	-1	1		58.76
-1	1	-1	1		58.08
1	1	-1	1		58.04
-1	-1	1	1		52.04
1	-1	1	1		51.88
-1	1	1	1		51.4
1	1	1	1		51.28

Average gain of (-1) =
55.39 dB

Average gain of (+1) =
55.04 dB

Change in gain = .35 dB

Determining Variation due to L3 Only

Effect of bond wire inductance L3

L1	L2	L3	L4	Gain
0	0	0	0	55.215
-1	-1	-1	-1	59.24
1	-1	-1	-1	59.2
-1	1	-1	-1	58.44
1	1	-1	-1	58.4
-1	-1	1	-1	52.36
1	-1	1	-1	52.16
-1	1	1	-1	51.72
1	1	1	-1	51.6
-1	-1	-1	1	58.84
1	-1	-1	1	58.76
-1	1	-1	1	58.08
1	1	-1	1	58.04
-1	-1	1	1	52.04
1	-1	1	1	51.88
-1	1	1	1	51.4
1	1	1	1	51.28

Average gain of (-1) =
58.6 dB

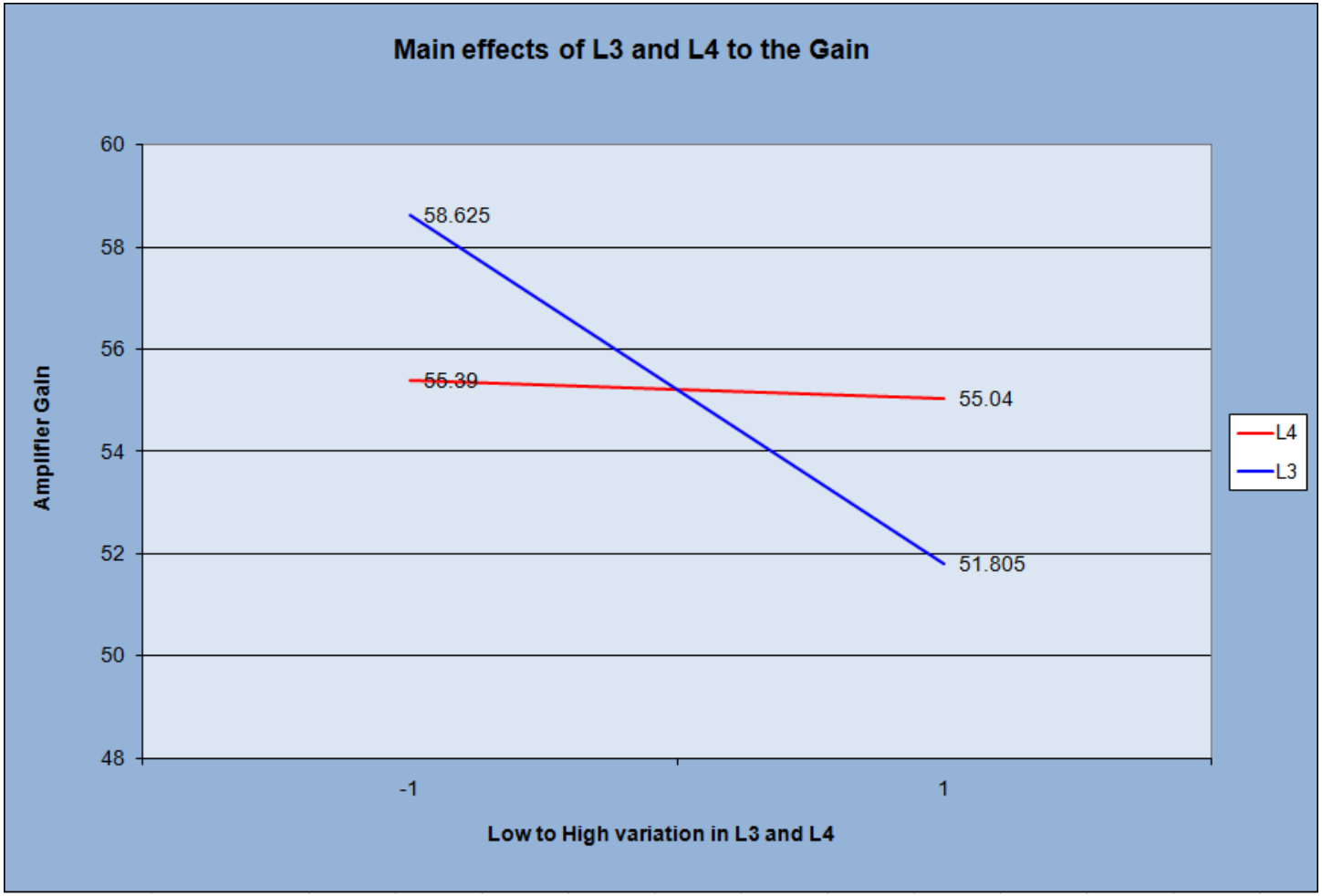
Average gain of (+1) =
51.8 dB

Change in gain = 6.8 dB

Large variation in Gain due to L3

Plotting the Effects of L3 and L4 on Gain

Effects Plots



Determining Variation due to L1*L3 Interaction

Effect/Interaction of bond wire inductance L1*L3

L1	L2	L3	L4	Gain
0	0	0	0	55.215
-1	-1	-1	-1	59.24
1	-1	-1	-1	59.2
-1	1	-1	-1	58.44
1	1	-1	-1	58.4
-1	-1	1	-1	52.36
1	-1	1	-1	52.16
-1	1	1	-1	51.72
1	1	1	-1	51.6
-1	-1	-1	1	58.84
1	-1	-1	1	58.76
-1	1	-1	1	58.08
1	1	-1	1	58.04
-1	-1	1	1	52.04
1	-1	1	1	51.88
-1	1	1	1	51.4
1	1	1	1	51.28

Average gain of (-1) = 55.24 dB

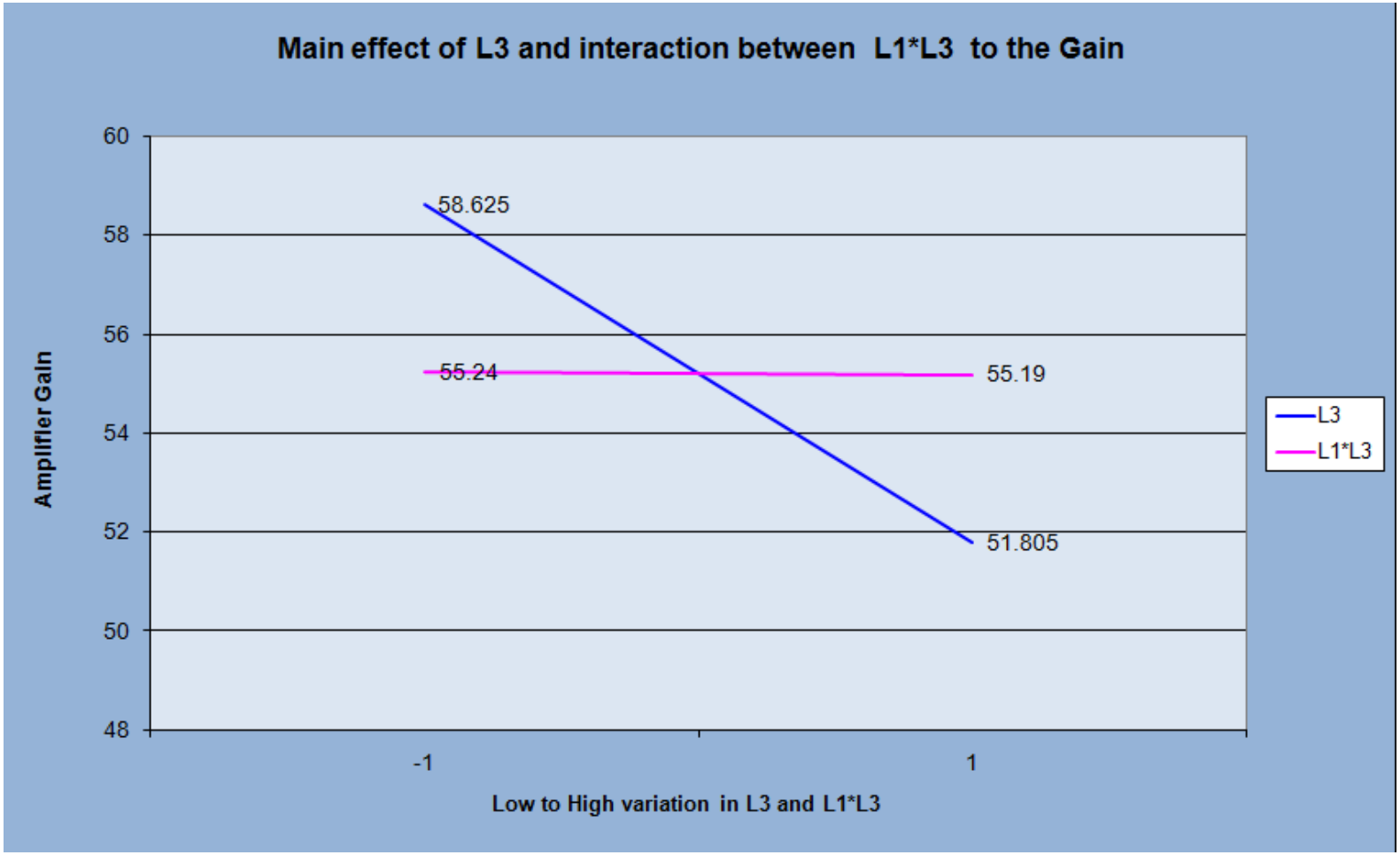
Average gain of (+1) = 55.19 dB

Change in gain = .05 dB

Very small interaction effect from L1*L3

Plotting the Effects of L3 and L1*L3 on Gain

Effects Plots



Perform Effects on all L's Combinations

Write an Equation for Gain due to all effects

Gain = 55.215 -.05 L1 - .345 L2 - 3.41 L3 - .175 L4

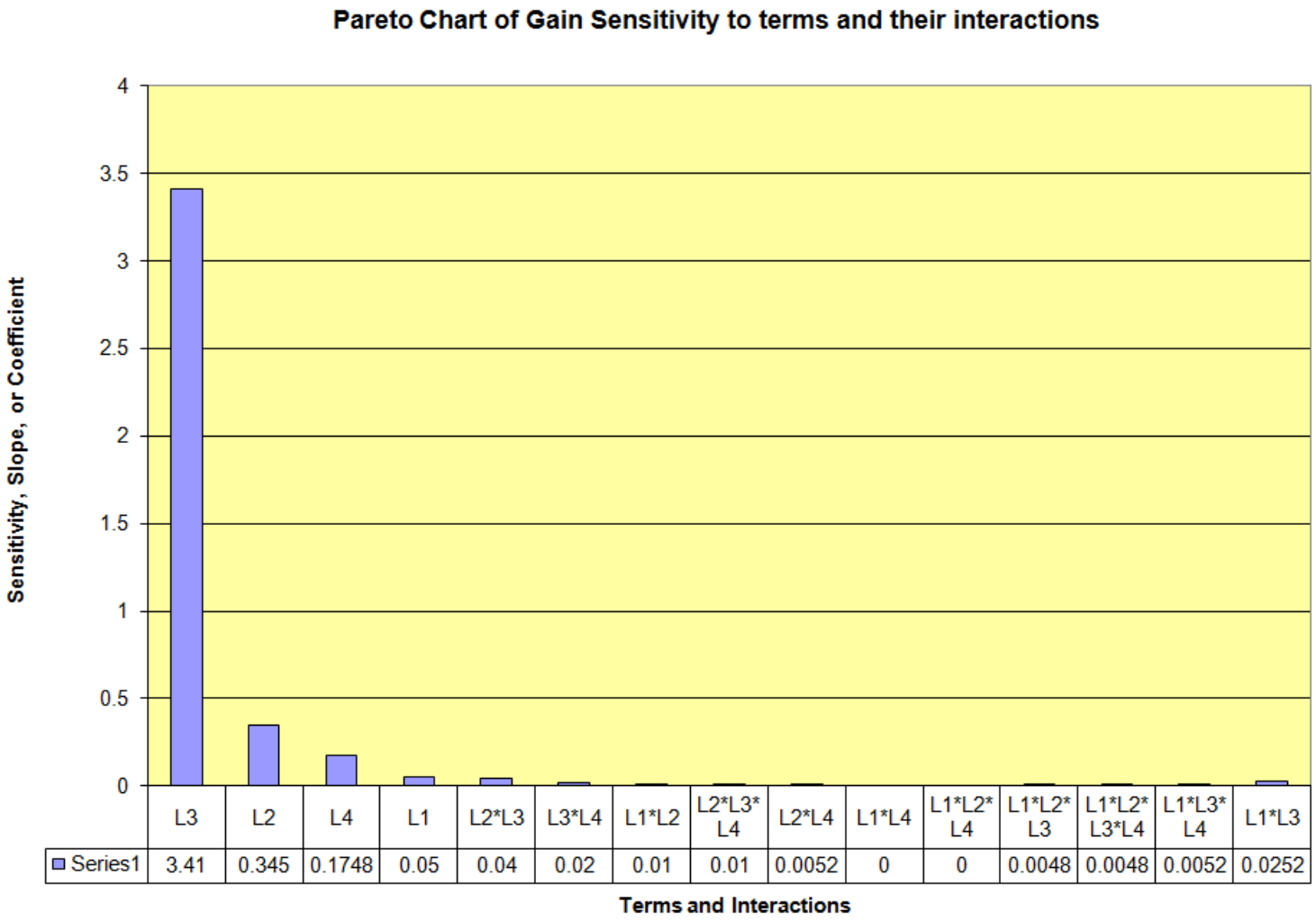
+ .01 L1*L2 - .0252 L1*L3 - 0.0 L1*L4 + .04 L2*L3
+.0052 L2*L4 + .02 L3*L4

-.0048 L1*L2*L3 + 0.00 L1*L2*L4 -.0052 L1*L3*L4 +.01 L2*L3*L4

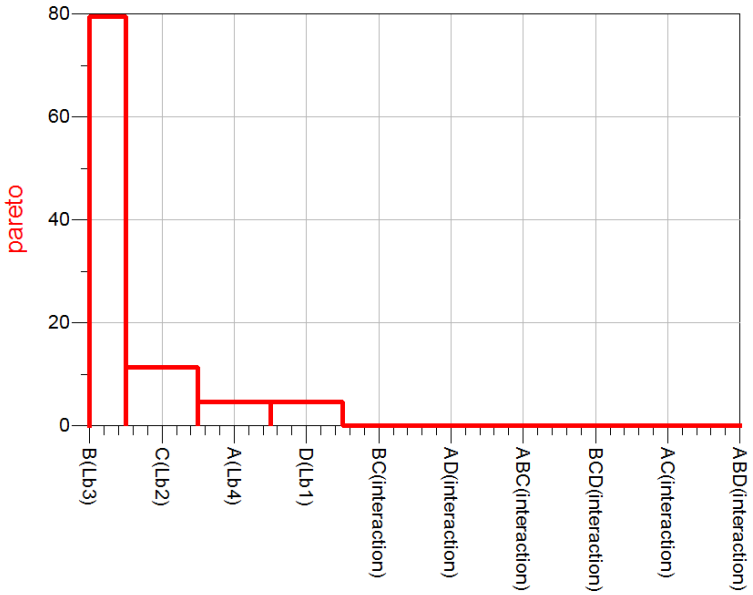
-.0048 L1*L2*L3*L4

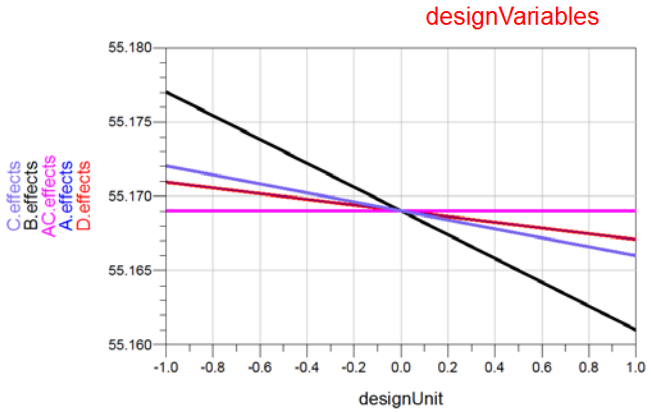
Plotting the Effects on Pareto Chart

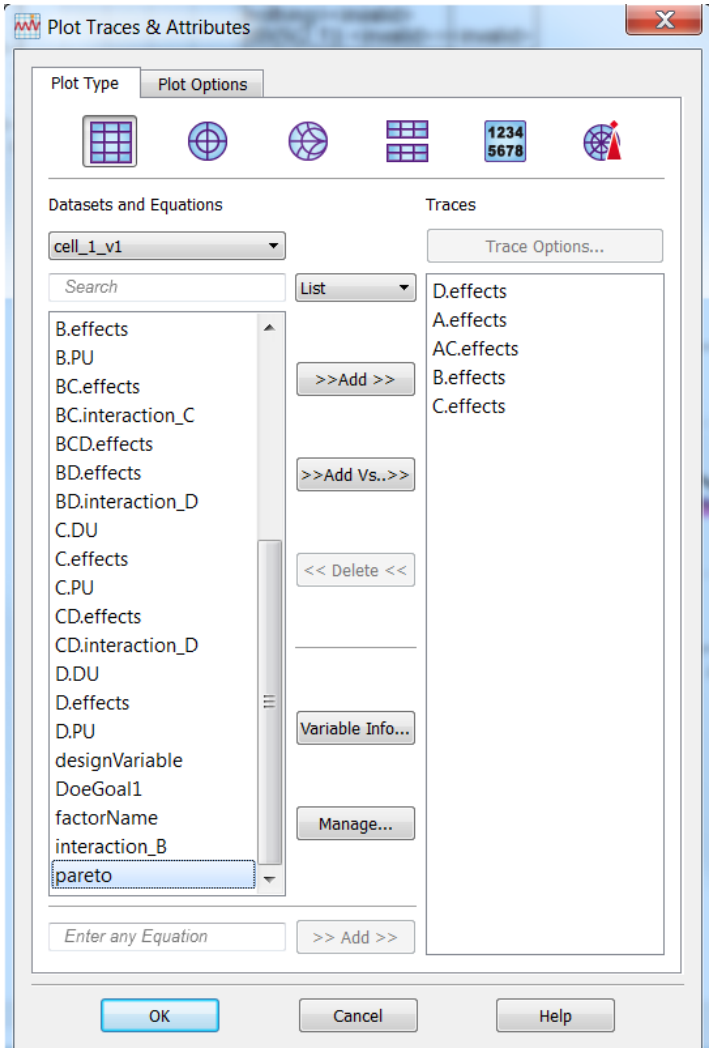
L3 is the biggest contributor to the Gain fluctuation in the system



DOE Analysis, Effects Plots, Pareto Charts are automatically produced in ADS







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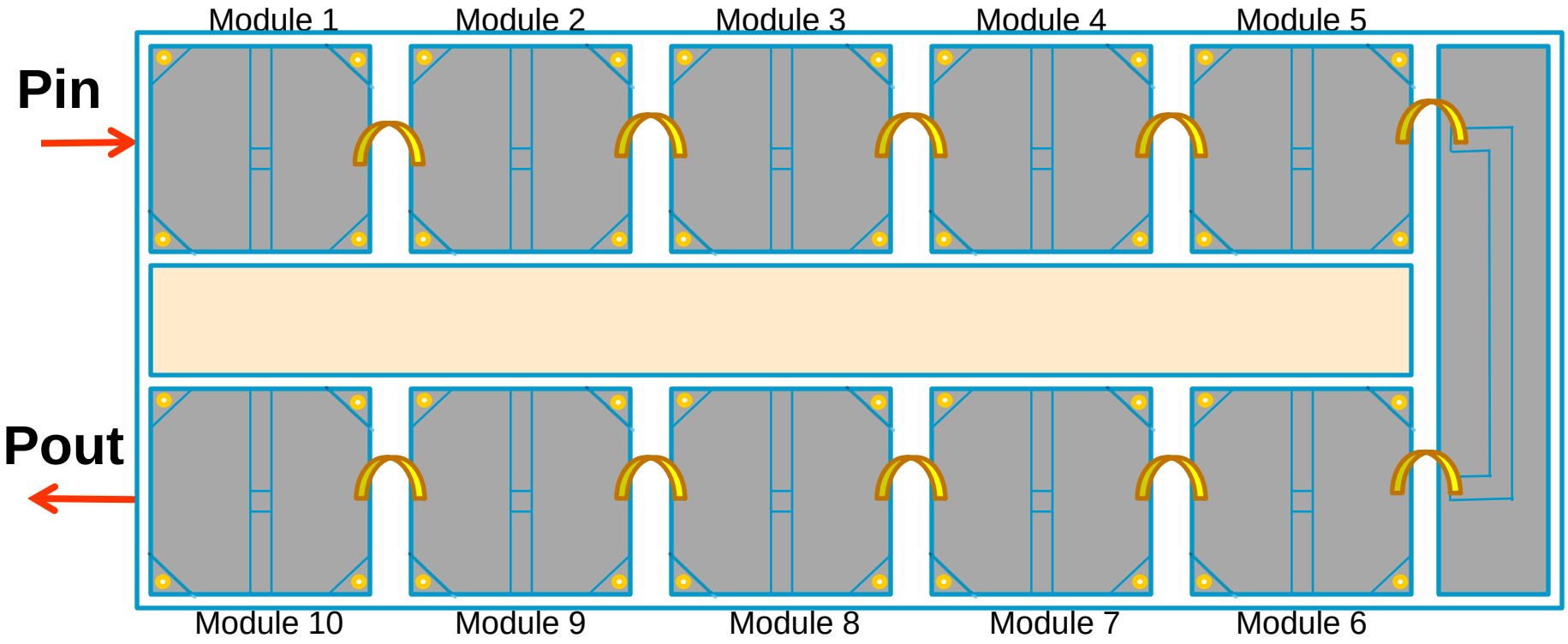
Real Example
System Level DOE

DOE at the System Level

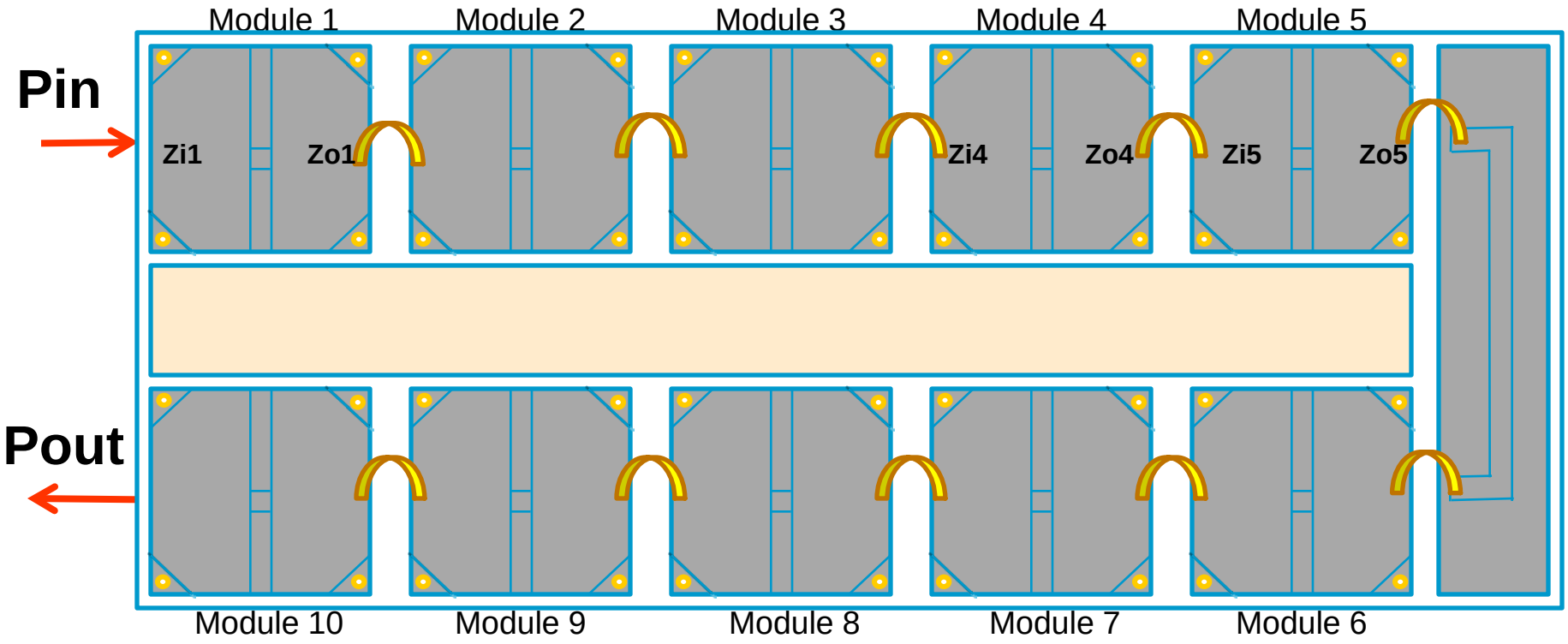
50 ohm cascaded modules



Each module was fully tested and met all of its specs
The whole integrated system failed; Gain and Pout fell short

DOE at the System Level

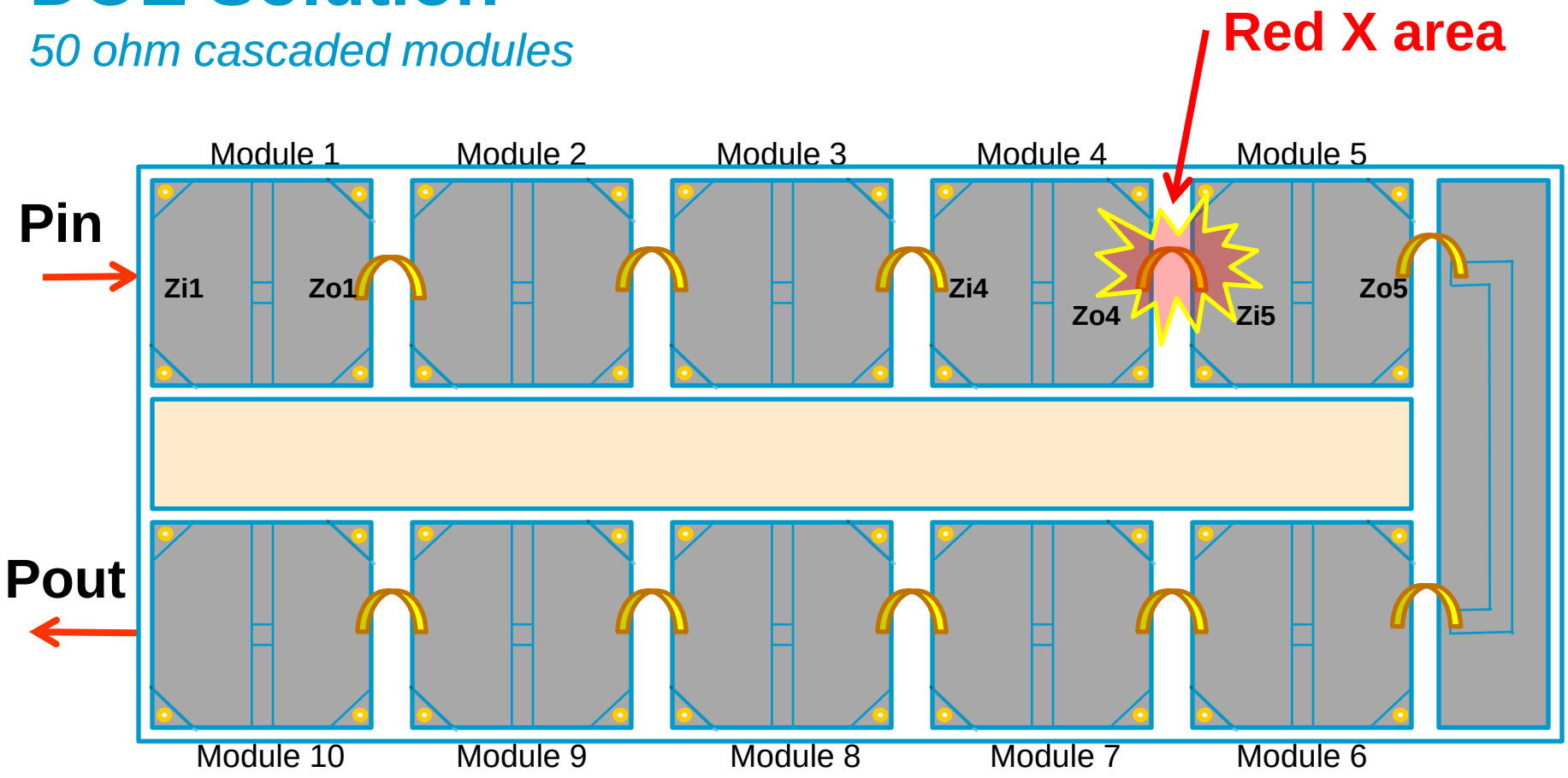
50 ohm cascaded modules



Use Zin and Zout on each module as our DOE variables (20 variables)
Zi1, Zo1, Zi2, Zo2, Zi3, Zo3, …….. Zi10, Zo10

DOE Solution

50 ohm cascaded modules



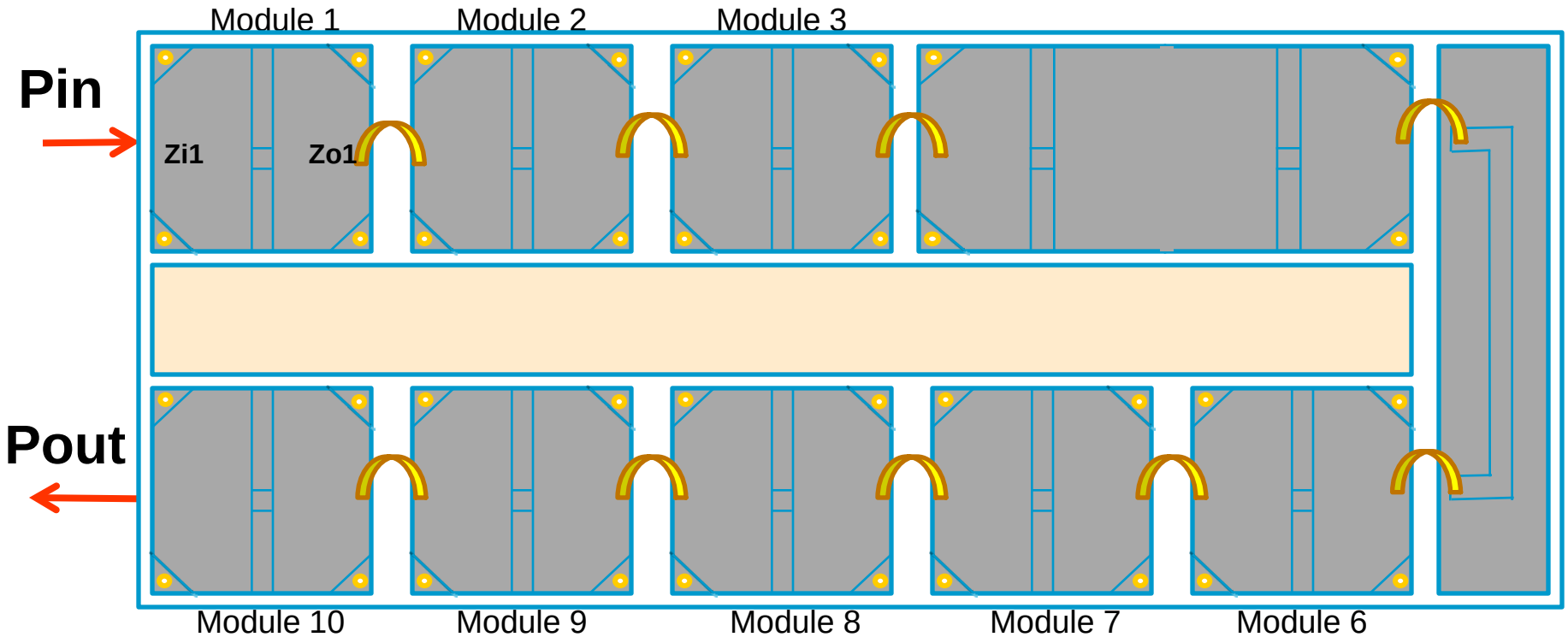
DOE Results:

Zo4, Zi5 turned out to be the most sensitive variables to Pout

DOE Solution

50 ohm cascaded modules

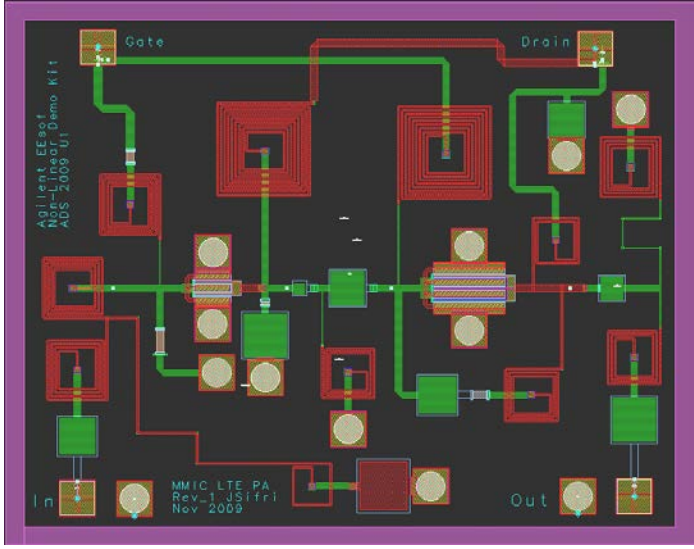
Module 4,5 combined into one module eliminates variability



Quick Fix Solution:
Eliminated Zo4, Zi5 sensitivity to bond wire; combined them into a one module

DOE at the Circuit /Module Level

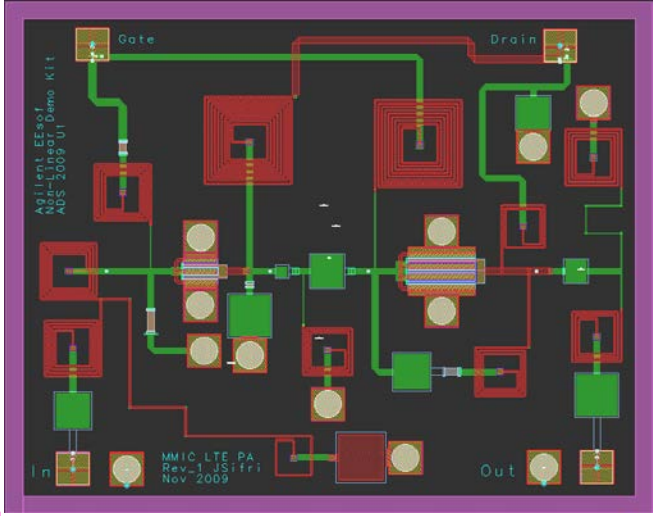
Demo: 2-Stage MMIC PA

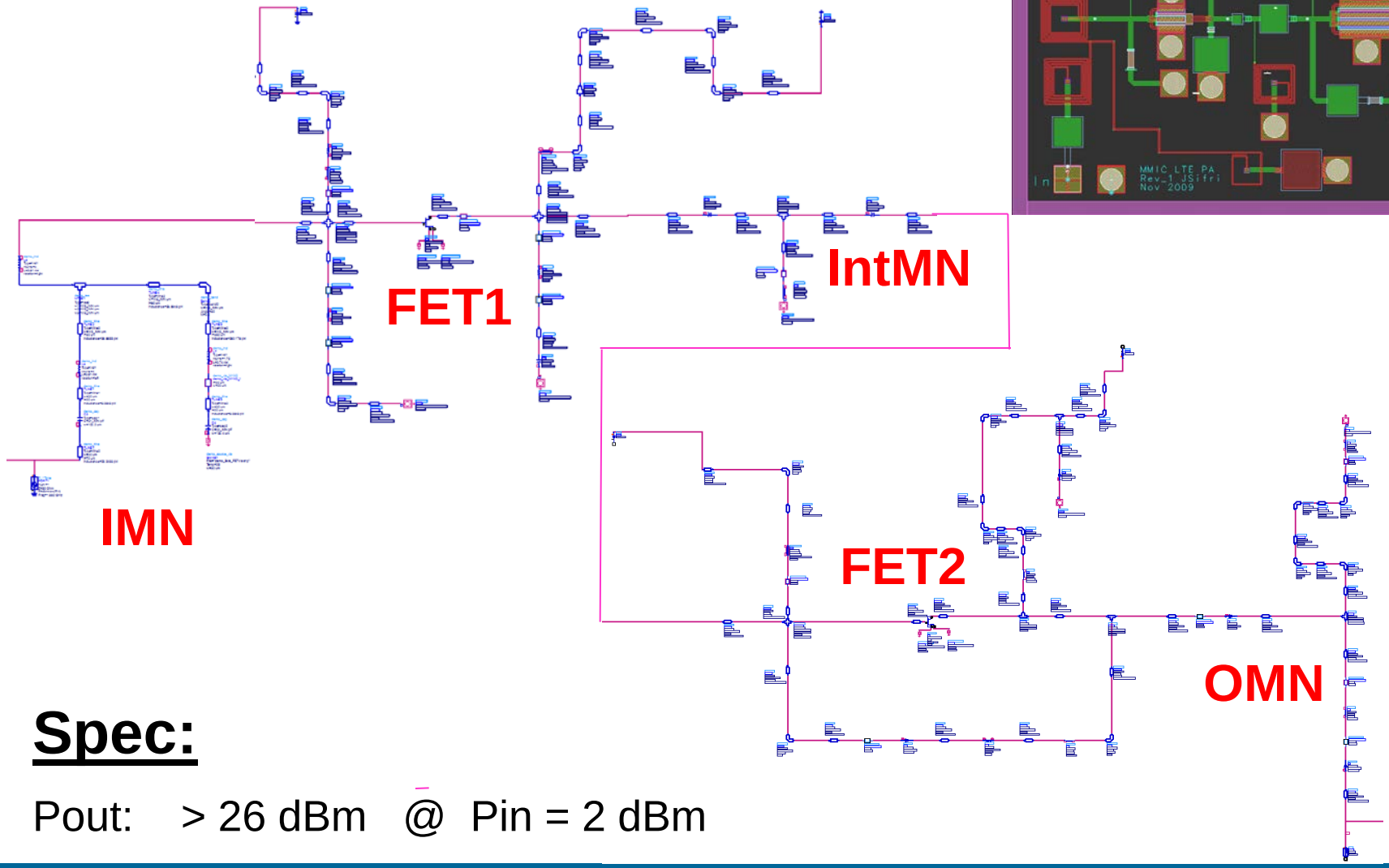


Spec:

Pout: > 26 dBm @ Pin = 2 dBm

2-Stage MMIC PA

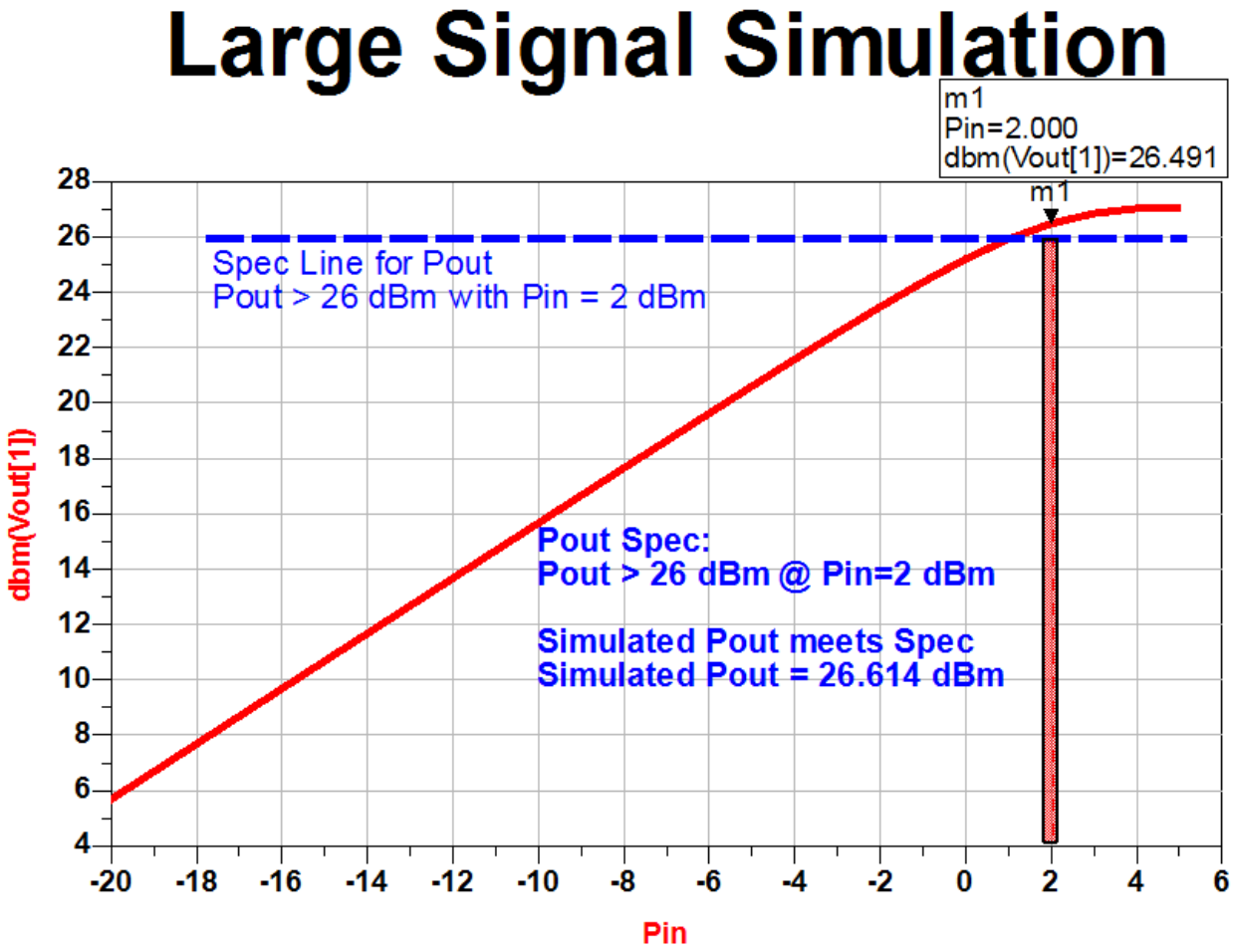




Spec:

Pout: > 26 dBm @ Pin = 2 dBm

2-Stage MMIC PA - Pin / Pout

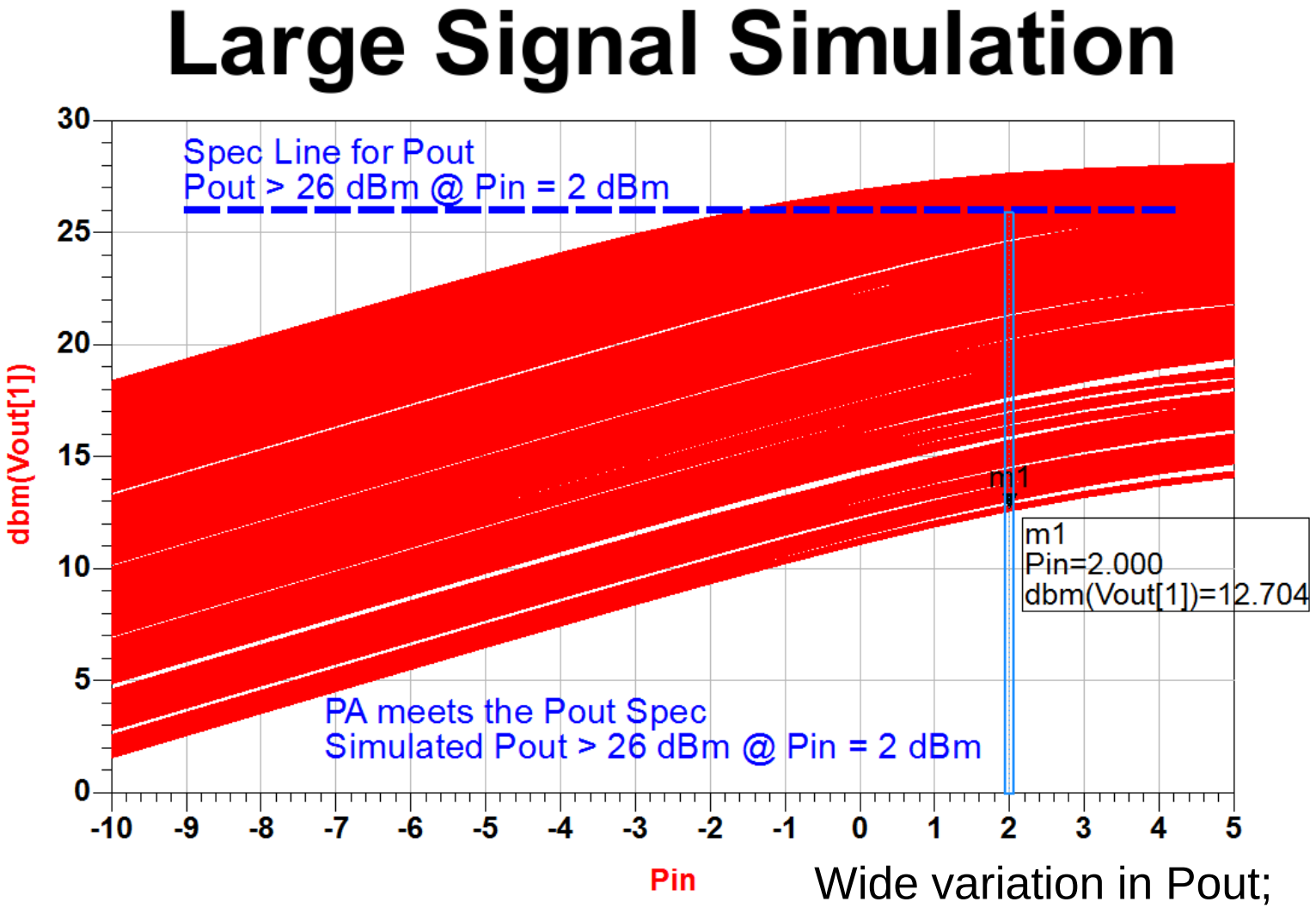


Spec:

Pout: > 26 dBm @ Pin = 2 dBm

Nominal simulation meets the spec

2-Stage MMIC PA - Yield Results



Spec:

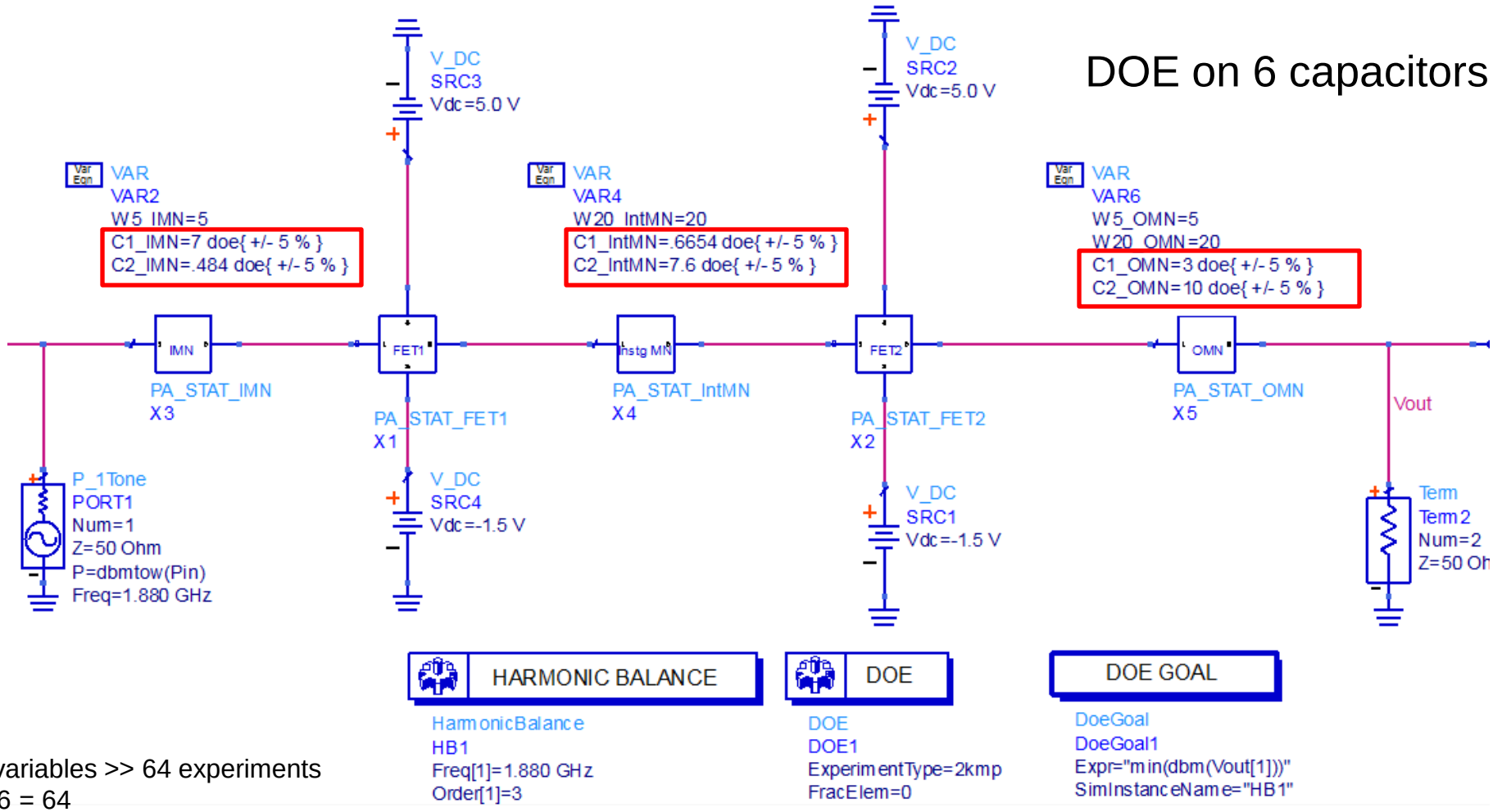
Pout: > 26 dBm @ Pin = 2 dBm

Wide variation in Pout;
Poor yield

Design of Experiments - DOE

Demo in ADS

Performing DOE Analysis on all Caps to pin point the source of the problem in Yield

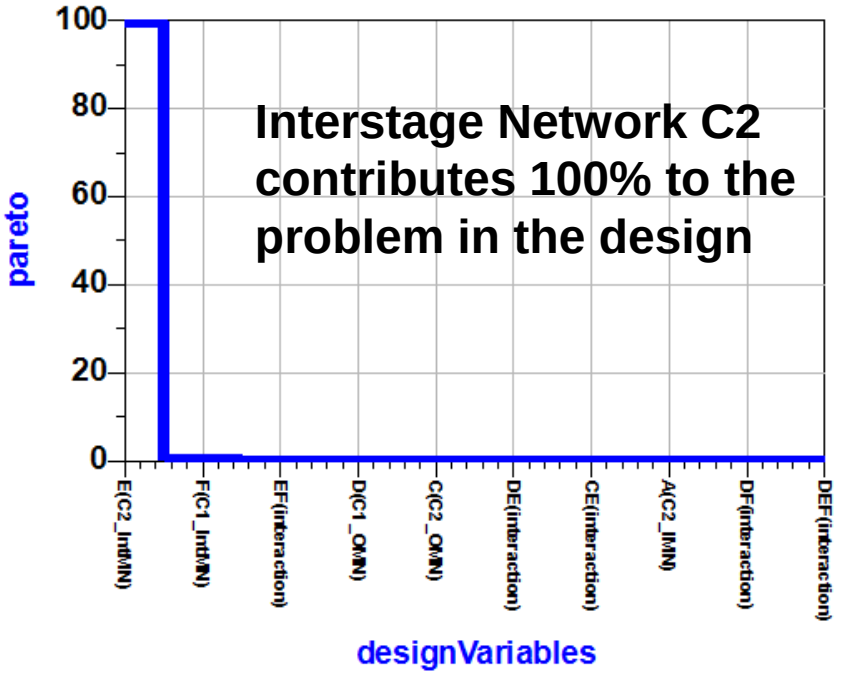


6 variables >> 64 experiments
2^6 = 64

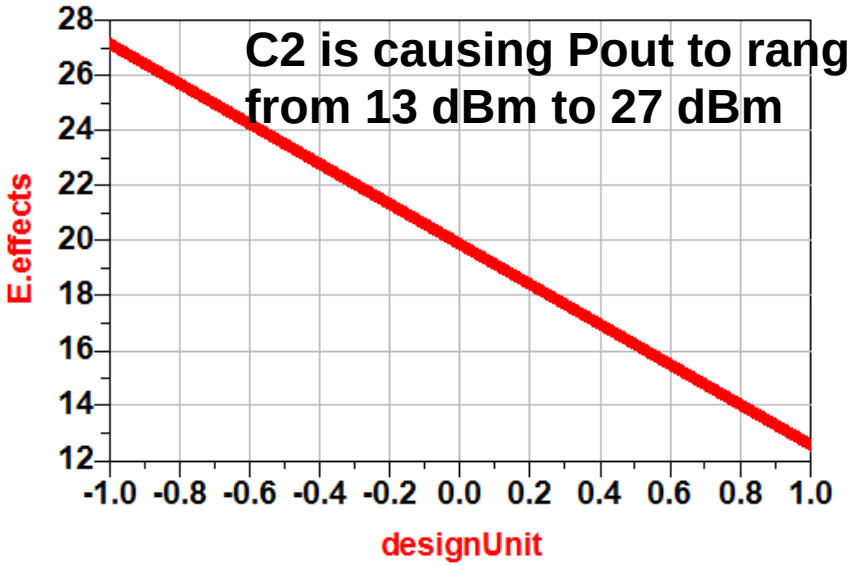
Design of Experiments - DOE

Design of Experiments (DOE) Results on 6 Capacitors

1- Pareto analysis on the factors
2- Effects plots on the factors

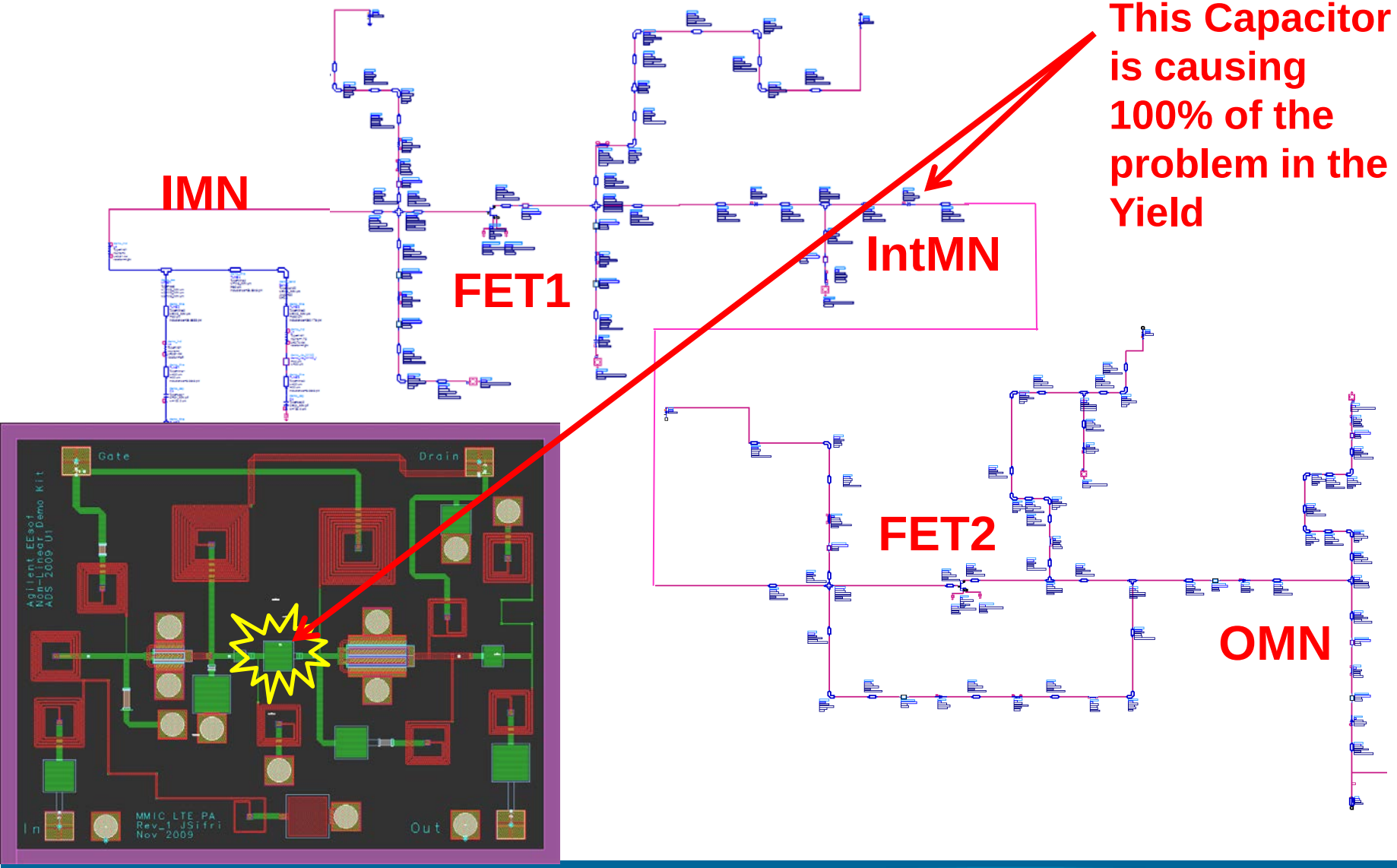


C2_IntMN (in the Interstage Matching Network) is contributing 100% to the huge variation in Pout. Therefore, the problem in our design is coming only from C2 in the Interstage Matching Network



This plot displays the absolute value of the variation in Pout coming from C2 in the Interstage Network; 13 to 27 dBm, identical to the results variation we got from MonteCarlo analysis

Demo: 2-Stage MMIC PA Schematic



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Design of Experiments - DOE

Design of Experiments told us:

100% of the problem is due to the Interstage Matching Network

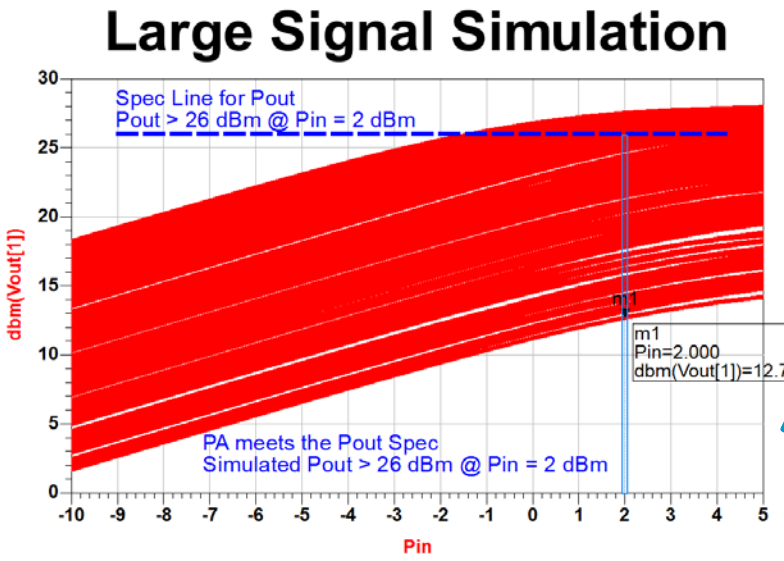
Specifically, it is due to Capacitor C2 in the Interstage Matching Network

Yield Sensitivity Histograms

Before I decide whether or not I should discard the Interstage Network and redesign a new one, let me do further investigation using the tool:

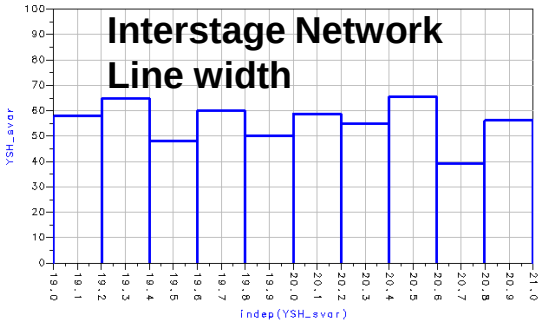
Yield Sensitivity Histograms

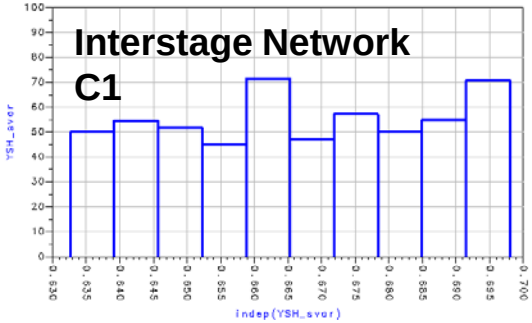
Back to our Two Stage MMIC PA

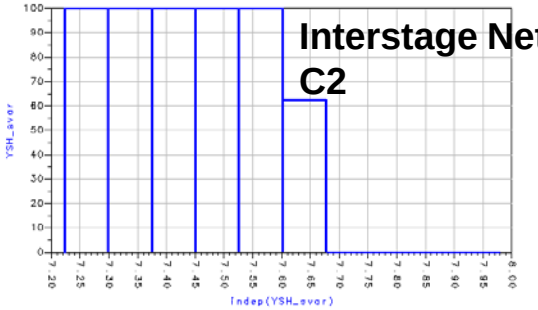


Post Process the Yield Data and Generate Yield Sensitivity Histograms (YSH)

Lowering C2 nominal value makes Yield go up to 100%

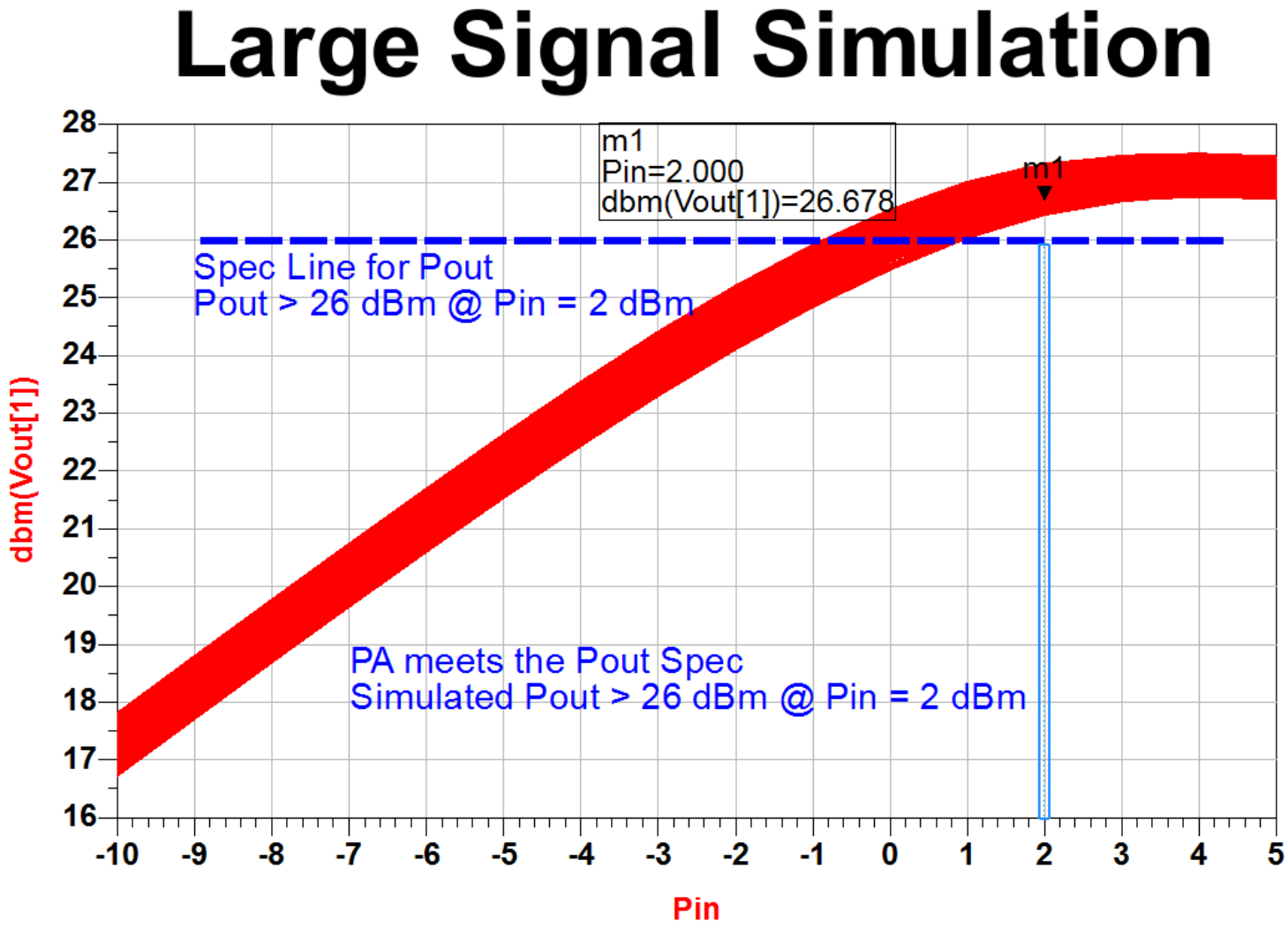






Lowering Interstage C2 from 7.6 pf to 5 pf

DOE quickly found the problem and fixed it



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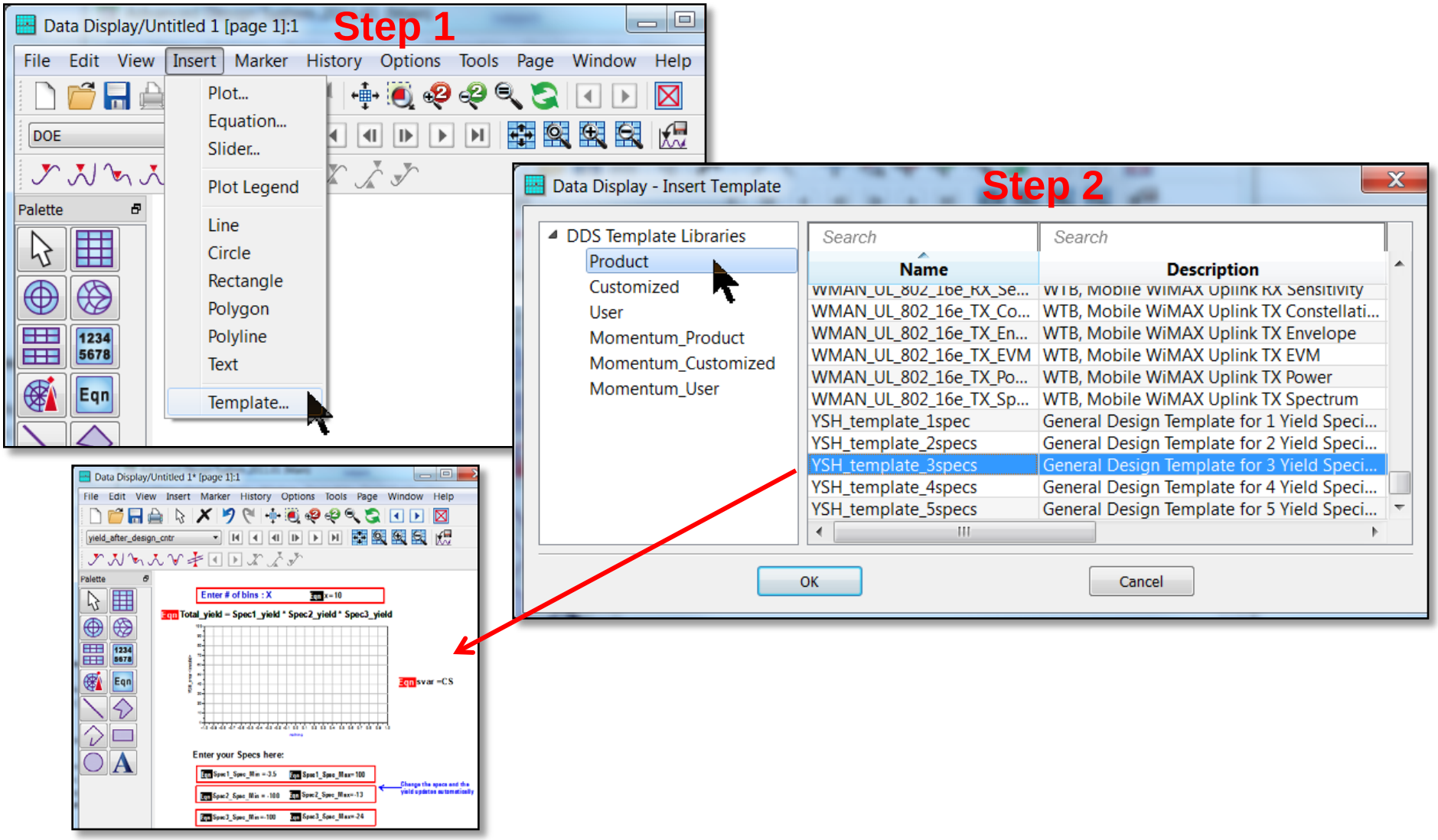
Yield Sensitivity Histogram Templates are available in ADS

This is how to access them



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Success Story on a Dual Band PA – using DOE approach

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September 2008 Issue: Technical Feature

An Innovative And Integrated Approach to III-V Circuit Design

From: Vol. 51 | No. 9 | **September 2008** | 136

by Y. Yang, P. Zampardi, M. Fredriksson, J. Xu, S Chen and G. Zhang, Skyworks Solutions Inc.; J. Sifri, Agilent Technologies / Agilent EEsof EDA

In wireless handset design, specifically power amplifiers (PA), there is constant pressure to improve time-to-market while maintaining high yields. To meet these demands, designers need to evaluate current design practices and identify areas for improvement. Presently, most PA designers spend a great deal of time bench-tuning to optimize circuits. Since this is very time consuming, the main consideration is obtaining the best "nominal" performance, and process variation (or whether the wafer used for tuning is optimal) is generally an afterthought.

http://cp.literature.agilent.com/litweb/pdf/5990-7135EN.pdf

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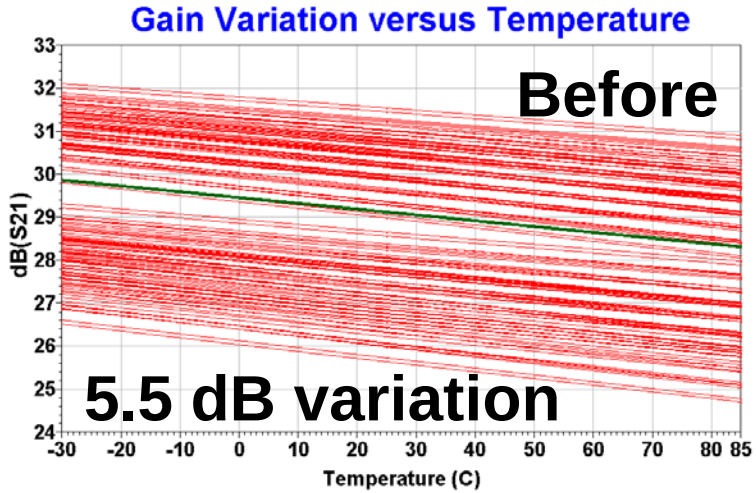
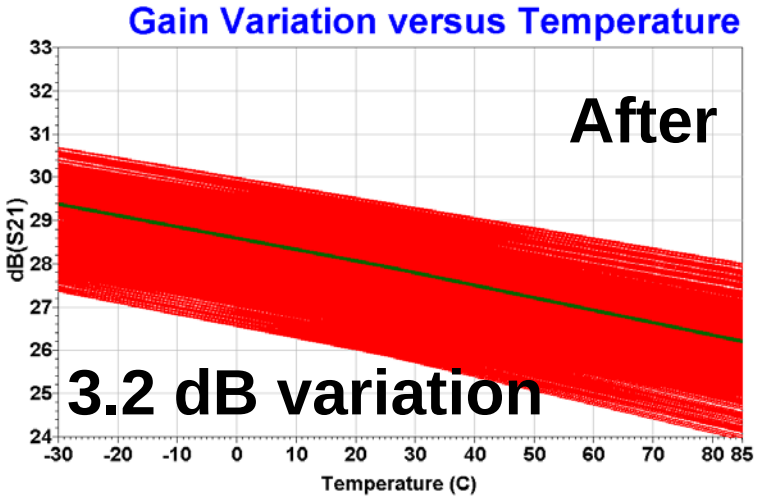
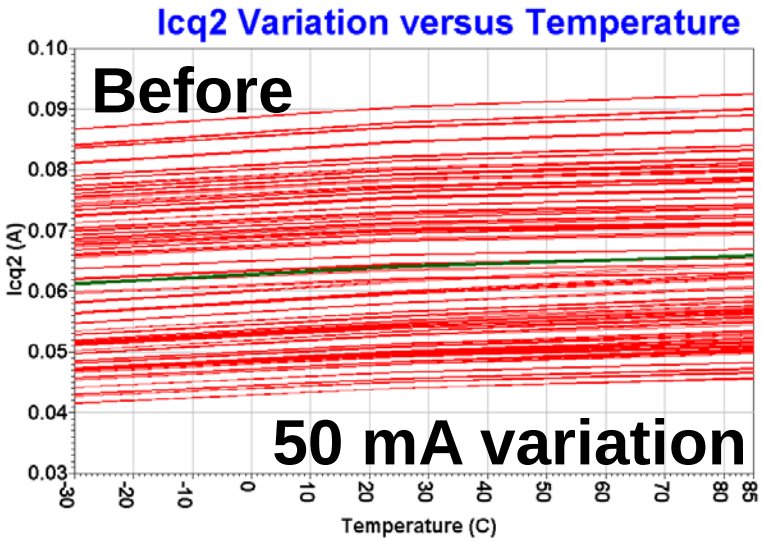
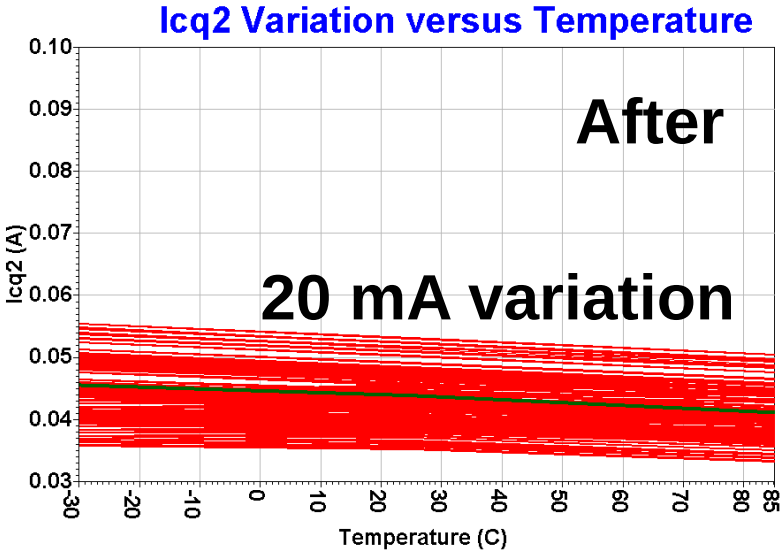
Skyworks Solutions Inc.

Dual Band PA – using Design of Experiments (DOE)approach









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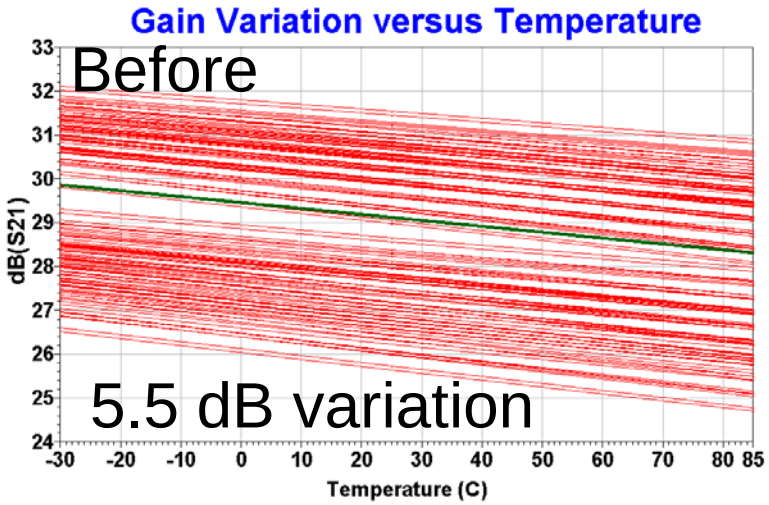
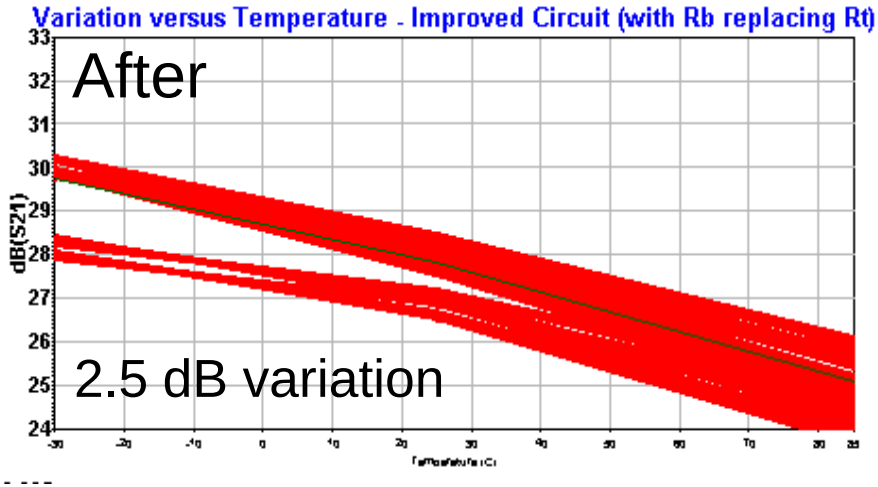
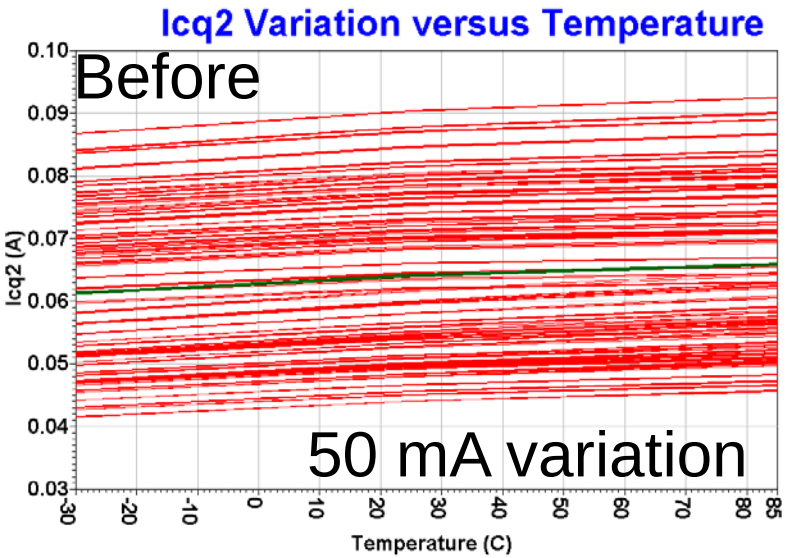
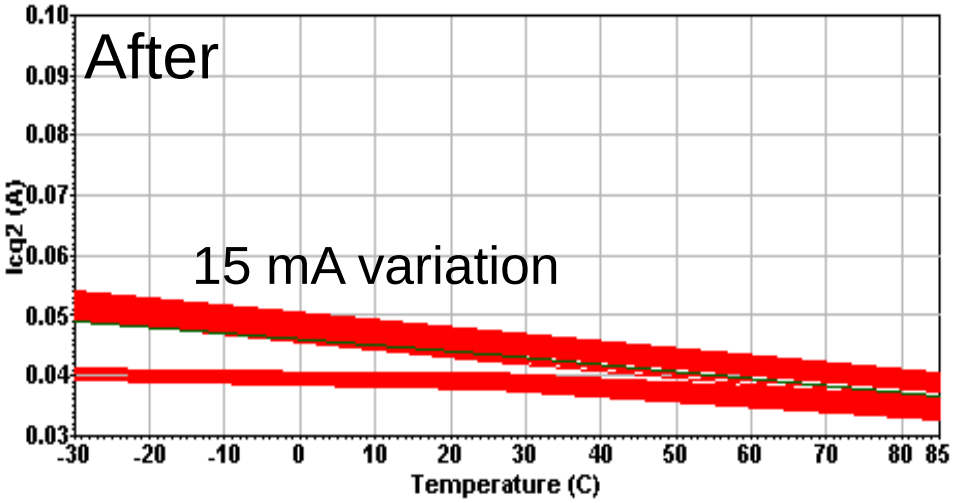
DOE - 2nd round

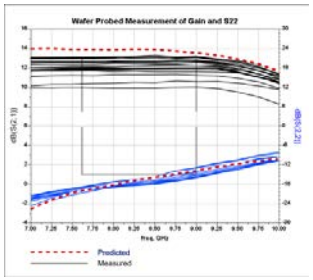


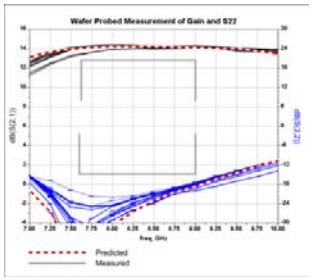






Conclusion





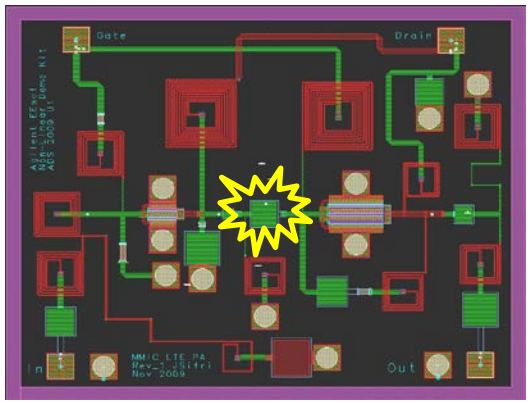
Different Topologies produce different yield

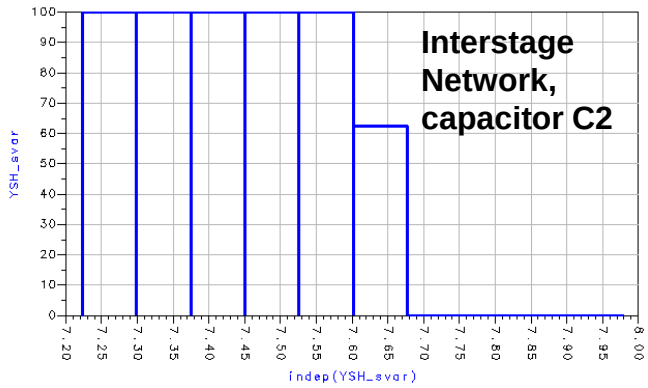
- DOE determines the robustness of your topology
- ADS Impedance Matching Utility helps create robust topologies

DOE runs very fast

- Provides similar information as Yield analysis at a fraction of the time
- Finds the sensitive components and networks and interactions between them

YSH pin points all sensitive RED X components in your design





All tools are available to you in ADS most basic core

Resource Material

YouTube videos (including ADS2011 videos)
http://www.youtube.com/user/AgilentEEsof

MMIC Design Seminar Web Page
www.agilent.com/find/eesof-mmic-seminar

MMIC Design Overview Page
http://www.agilent.com/find/eesof-mmic-overview

My e-mail address: jack_sifri@agilent.com
Let me know if you have any question on this Webcast