Analog, RF and EMC Considerations in Printed Wiring Board (PWB) Design

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Introduction
Overview

- **Printed Wiring Board (PWB)**
  - Also known as Printed Circuit Board (PCB)
  - Provides a means of interconnecting various electronic components
  - Provides a mounting platform for these components
  - In some cases, provides a path for thermal management

- **When designing electronic circuits, physical properties of the PWB interconnects are often put aside**
  - Series Inductance
  - Shunt Capacitance
  - Propagation Delay and Dispersion
  - Dielectric Loss & Resistivity
  - DC Resistance and $I^2R$ Losses
  - Skin Depth
  - Voltage Breakdown
  - Coupling
As technology migrates to extremes, PWB characteristics must be taken into account

<table>
<thead>
<tr>
<th>Circuit Types</th>
<th>Potential Focus Areas</th>
</tr>
</thead>
<tbody>
<tr>
<td>High Speed Digital or Fast $t_r$ and $t_f$ Digital</td>
<td>Dielectric constant and loss, resistive loss, dispersion, impedance matching, propagation delay</td>
</tr>
<tr>
<td>RF</td>
<td>Dielectric constant and loss, resistive loss, dispersion, impedance matching</td>
</tr>
<tr>
<td>High Current</td>
<td>Resistance ($I^2R$ losses and regulation), thermal management</td>
</tr>
<tr>
<td>High Voltage</td>
<td>Dielectric breakdown, clearances, creepage distances, trace geometries (to reduce HV gradients), partial discharge (voids)</td>
</tr>
<tr>
<td>Critical Analog</td>
<td>Trace/pad inductance, capacitance</td>
</tr>
<tr>
<td>High Impedance</td>
<td>Dielectric resistivity, coupling</td>
</tr>
</tbody>
</table>
Other Considerations

- Low Size Weight & Power (SWaP) Footprints (e.g. avionics, consumer electronics)
- Electromagnetic Environment of the Circuit Card Assembly (CCA)
- Escape routing on high I/O count, fine pitch packages (e.g. 1.0 mm, 0.8 mm and 0.5 mm BGAs)
- PWB design often involves collaboration among multiple disciplines
  - Electrical
  - Mechanical/Thermal
  - Manufacturing
  - Design/Drafting
  - PWB Supplier
  - Program Management (cost, schedule)
PWB Construction

Wide variety of construction options.
PWB/CCA Examples

Aramid/Polyimide, 10 Layer Dual Digitizer/Demodulator

FR-4 Laminate, 24 Layer Radar Signal Processor Backplane

High Thermal Conductivity Laminate, 4 Layer Servo Amplifier

Flex, 4 Layer Signal Distribution

Metal Core, RT/duroid 6010LM, 2 Layer RF Power Amplifier

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Types of Rigid PWB

- Type 1: Rigid, One Layer
- Type 2: Rigid, Two Layer
- Type 3: Rigid, Multi Layer, w/o blind or buried vias
- Type 4: Rigid, Multi Layer, w/ blind and/or buried vias
- Type 5: Rigid, Metal Core, w/o blind or buried vias
- Type 6: Rigid, Metal Core, w/ blind and/or buried vias

(Per IPC-2222 standard, section 1.6.1)
Types of Flex PWB

- Type 1: Flex, One Layer
- Type 2: Flex, Two Layer
- Type 3: Flex, Multi Layer
- Type 4: Multilayer rigid and flexible material combinations containing three or more conductive layers with plated-through holes
- Type 5: Flex or rigid-flex containing two or more conductive layers without plated-through holes

(Per IPC-2223 Standard, section 1.2.1)
Footnotes on Flex PWBs

- Used as alternative to a wiring harness
- Many similarities to rigid PWBs
- Typically higher development cost than harness
- Typically cheaper than harness in production
- Improved repeatability
- Typically much less real estate needed
PWB Stack-Ups (1 and 2 Layer)

**One Sided**
- Least expensive (assuming no plated through holes)
- Applicable to straightforward circuits
- Difficult to control EMI without external shielding
- Difficult to control impedance

**Two Sided**
- Inexpensive
- Applicable to more complex circuits
- EMI can be mitigated by use of a ground plane
- Impedance control is simplified by use of a ground plane

Signals, Grounds and Supply Traces

Ground Plane and/or Traces for signals and supply
More routing resources for signals, power and ground (reference plane)

Option for dedicating layer(s) to ground
- Forms reference planes for signals
- Mitigates EMI Control
- Simpler impedance control

Option for dedicating layer(s) to Supply Rail(s)
- Low ESL/ESR power distribution

Layers are interconnected with vias
- Through-hole vias
- Buried vias
- Blind vias
- Micro vias
- Back-Drilled via
**Vias**

- Needed to interconnect layers
  - Introduce discontinuities
  - “Choke-off” routing
  - Perforate Ground/Supply Planes
  - Ground vias can aid in signal integrity

- Traditionally implemented with Plated Through Holes (PTHs)
  - Most disruptive as they impact all layers, and are the longest via type
  - Typically not suitable for use under high density components (e.g. 0.8 mm pitch BGAs) because of pad size

- Blind, Buried or Micro Vias
  - Less disruptive as they impact fewer layers
  - Aid in escape routing of high density components (e.g. BGAs)
  - Additional processing cost can be offset by reduction in layers
### Via Parameters

<table>
<thead>
<tr>
<th>Via Dia</th>
<th>10</th>
<th>12</th>
<th>15</th>
<th>25</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pad Dia</td>
<td>22</td>
<td>24</td>
<td>27</td>
<td>37</td>
</tr>
<tr>
<td>Anti-Pad Dia</td>
<td>30</td>
<td>32</td>
<td>35</td>
<td>45</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>R</th>
<th>L</th>
<th>C</th>
<th>R</th>
<th>L</th>
<th>C</th>
<th>R</th>
<th>L</th>
<th>C</th>
<th>R</th>
<th>L</th>
<th>C</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.55</td>
<td>0.78</td>
<td>0.48</td>
<td>1.25</td>
<td>0.74</td>
<td>0.53</td>
<td>0.97</td>
<td>0.68</td>
<td>0.60</td>
<td>0.57</td>
<td>0.53</td>
<td>0.83</td>
</tr>
</tbody>
</table>

**Length: 60 Planes: 5**

<table>
<thead>
<tr>
<th>R</th>
<th>L</th>
<th>C</th>
<th>R</th>
<th>L</th>
<th>C</th>
<th>R</th>
<th>L</th>
<th>C</th>
<th>R</th>
<th>L</th>
<th>C</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.3</td>
<td>1.33</td>
<td>0.66</td>
<td>1.88</td>
<td>1.24</td>
<td>0.69</td>
<td>1.45</td>
<td>1.15</td>
<td>0.78</td>
<td>0.85</td>
<td>0.92</td>
<td>1.08</td>
</tr>
</tbody>
</table>

**Length: 90 Planes: 7**

Notes:
1. R in mΩ, L in nH, C in pF
2. Dimensions are in mils.
3. Planes are evenly spaced.
4. Via inductance can be approximated by:  \( L = 5.08h \left[ \ln \left( \frac{4h}{d} \right) - 0.75 \right] \) (h and d are in inches, L is in nH)
Core Construction
- As shown

Foil Construction
- Reverse core and pre-preg
Multi-Layer Stack-Up Examples

- **PWB Example #1**
  - Simple High Speed Digital Application
  - Six Layers
  - Moderate Density
  - Two Microstrip Routing Layers
  - Two Buried Microstrip Routing Layers
  - Single Supply Plane

- **PWB Example #2**
  - Moderate High Speed Digital Application
  - Ten Layers
  - High Density
  - Two Microstrip Routing Layers
  - Four Asymmetrical Stripline Routing Layers
  - Single Supply Plane

- **PWB Example #3**
  - Mixed Analog/RF/Digital Application
  - Ten Layers
  - Moderate Density
  - Two Microstrip Routing Layers
  - Four Asymmetrical Stripline Routing Layers
  - Single Digital Supply Plane
  - Analog supplies on inner layers

**Note:** For all examples, consider ground and power pours on all unused areas, especially on outer layers as density and vias allow.
PWB Stack-Up Guidelines

- Maximize symmetry to simply manufacturing and to mitigate warping
- Even number of layers preferred by PWB manufacturers
- Asymmetrical stripline has higher routing efficiency than symmetrical stripline
- Supply planes can be used as reference planes for controlled Z (but not preferred for analog or RF)
- Ideally, supply planes should be run adjacent to ground planes with a thin dialectic separation
- Signals on adjacent layers should be run orthogonally
  - Minimizes coupling between lines
PWB Materials

Wide variety of options available for laminates, conductor thickness, finish and conductor material.
Dozens of dielectric material suppliers to choose from:
- Arlon
- Bergquist
- Isola
- Panasonic
- Park Nelco
- Rogers
- Taconic
- Numerous others

Several standard dielectric thickness options

Metal Options
- Virtually all PWBs use copper as the conductor material but other materials (such as aluminum) can also be used
- Wide variety of copper thickness options available

Two copper plating options
- Rolled
- Electro-Deposited (multiple variants)
Electrical Considerations in Selecting Dielectric (Laminate) Material

- **Permittivity**
  - Typically expressed relative to free space ($\varepsilon_r$)
  - The more stable, the better
  - Lower values may be more suitable for high layer counts
  - Higher values may be more suitable for some RF structures

- **Loss**
  - Typically expressed as loss tangent ($\tan\delta$)
  - The lower, the better
  - Becomes more of an issue at higher frequencies

- **Moisture Absorption**
  - The lower, the better
  - Can affect dielectric constant and loss tangent
  - Can be mitigated with conformal coating

- **Voltage Breakdown**
  - The higher, the better
  - Typically not an issue, except in high voltage applications

- **Resistivity**
  - Typically expressed in M$\Omega$ for surface resistivity and M$\Omega$-cm for volume resistivity
  - The higher, the better
  - Typically not an issue, except in low leakage, high impedance and/or HV applications
Mechanical Considerations in Selecting Dielectric (Laminate) Material

- Peel Strength
  - The higher, the better
- Flammability Rating
  - UL Standards
- Glass Transition Temperature (Tg)
- Thermal Conductivity
  - Typically PWB material is considered a thermal insulator
  - Some laminates are available with enhanced thermal conductivity
  - Planes & vias contribute to thermal conductivity
- Coefficient of Expansion
  - XY matching to components, solder joint stress (LCC)
  - Z axis expansion, via stress
- Weight (density)
- Flexibility
  - Very low Flexural Modulus materials might require extensive support to prevent component damage
  - Very low Flexural Modulus materials might require extensive support to prevent PWB damage (cracking)
## PWB Material Examples

<table>
<thead>
<tr>
<th>Material</th>
<th>Dielectric Constant ($\varepsilon_r$)</th>
<th>Loss Tangent ($\tan\delta$)</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>FR-4, Woven Glass/Epoxy</td>
<td>4.7 (1 MHz) 4.3 (1 GHz)</td>
<td>0.030 (1 MHz) 0.020 (1 GHz)</td>
<td>Inexpensive, available, unstable $\varepsilon_r$, high loss</td>
</tr>
<tr>
<td>N7000-1 Polyimide</td>
<td>3.9 (2.5 GHz) 3.8 (10 GHz)</td>
<td>0.015 (2.5 GHz) 0.016 (10 GHz)</td>
<td>High $T_g$ (260 °C)</td>
</tr>
<tr>
<td>Park-Nelco</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CLTE Arlon</td>
<td>2.94 (10 GHz)</td>
<td>0.0025 (10 GHz)</td>
<td>Stable $\varepsilon_r$, low loss</td>
</tr>
<tr>
<td>RT6010LM Rogers</td>
<td>10.2 (10 GHz)</td>
<td>0.002 (10 GHz)</td>
<td>High $\varepsilon_r$, high loss</td>
</tr>
<tr>
<td>RO4350B Rogers</td>
<td>3.48 (10 GHz)</td>
<td>0.004 (10 GHz)</td>
<td>Stable $\varepsilon_r$, low loss, processing is similar to FR4</td>
</tr>
<tr>
<td>RT6002 Rogers</td>
<td>2.94 (10 GHz)</td>
<td>0.0012 (10 GHz)</td>
<td>Stable and accurate $\varepsilon_r$, low loss</td>
</tr>
</tbody>
</table>
Dielectric, Common Thickness

- **Core Material (depending on material type)**
  - 0.002, 0.003, 0.004, 0.005, 0.006, 0.007, 0.008, 0.009"
  - 0.010, 0.012, 0.014, 0.015, 0.018, 0.020, 0.031"
  - Typically RF laminates have fewer thickness options
  - Some laminates (e.g. FR-4) are available in 0.5 mil increments

- **Pre-Preg (depending on material type)**
  - 0.002, 0.003, 0.004, 0.005, 0.008"
  - Pre-preg can be stacked to some extent for thicker layers

- Use standard thickness in designing stack-up

- Work with anticipated PWB vendor(s) when designing stack-up and selecting material especially on complex PWB designs
## Common Thickness Options

<table>
<thead>
<tr>
<th>Weight</th>
<th>Thickness</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.25 oz</td>
<td>0.4 mil (9 µm)</td>
</tr>
<tr>
<td>0.5 oz</td>
<td>0.7 mil (18 µm)</td>
</tr>
<tr>
<td>1.0 oz</td>
<td>1.4 mil (35 µm)</td>
</tr>
<tr>
<td>2.0 oz</td>
<td>2.8 mil (70 µm)</td>
</tr>
</tbody>
</table>

## Plating Options

<table>
<thead>
<tr>
<th>Option</th>
<th>Top Side Surface Roughness</th>
<th>Dielectric Side Surface Roughness</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rolled</td>
<td>0.3 µm (12 µ”)</td>
<td>0.4 µm (16 µ”)</td>
<td>Typically lower loss at high frequency (&gt;1 GHz) than ED variants. This option is typically available on Teflon based laminates. Useful in flex circuits.</td>
</tr>
<tr>
<td>Electro Deposited</td>
<td>0.4-2.0 µm (16-79 µ”)</td>
<td>0.5-3.5 µm (20-138 µ”)</td>
<td>In general, ED is less prone to pealing. Roughness depends on copper thickness and specific type of ED process (Standard, Reverse Treated, VLP, HVLP).</td>
</tr>
</tbody>
</table>
All foils below are 18 μm (0.7 mils or 0.5 oz)
Considerations in Selecting Copper Thickness & Plating

- **Power**
  - Current capacity
  - Temperature rise (due to $i^2R$ heating)
  - Trace failure due to short
  - Voltage drop (supply voltage regulation)

- **Signal Loss**
  - Thicker/wider lines reduce resistive loss
  - Higher surface roughness increases loss (>1 GHz)

- **Etch Factor**
- Actual trace shape is trapezoidal
- Thinner copper produces more precise geometries with narrow line widths
- For traces >5 mils, 1 oz or thinner is acceptable
- For traces <5 mils, 0.5 oz or thinner copper should be used
- Guidelines are fabricator and application dependent

0.005” Trace on 1 oz Copper

0.003” Trace on 1 oz Copper
Etch Factor Effects

- Critical in some RF applications
  - Directional Couplers, Interdigital Filters
- Critical in some narrow line width geometries
  - Significantly effects current capacity of trace
  - Significantly effects trace resistance and loss
- In many applications, effects on $Z_0$, $L$, $C$ can be ignored (Buried Microstrip Example)

<table>
<thead>
<tr>
<th>$\theta$ (°)</th>
<th>L (nH/in)</th>
<th>C (pF/in)</th>
<th>$Z_0$ (Ω)</th>
</tr>
</thead>
<tbody>
<tr>
<td>90</td>
<td>8.5</td>
<td>3.4</td>
<td>50.0</td>
</tr>
<tr>
<td>79</td>
<td>8.6</td>
<td>3.3</td>
<td>50.7</td>
</tr>
<tr>
<td>72</td>
<td>8.6</td>
<td>3.3</td>
<td>51.0</td>
</tr>
<tr>
<td>60</td>
<td>8.7</td>
<td>3.3</td>
<td>51.5</td>
</tr>
<tr>
<td>45</td>
<td>8.8</td>
<td>3.2</td>
<td>52.2</td>
</tr>
</tbody>
</table>
Signal Distribution and Signal Integrity (SI)

SI is a set of measures to ensure the quality of an electrical signal.
Single Ended Structure Examples

Microstrip

- Signal Trace
- Ground Plane
- Dielectric
- W
- t
- h

Buried Microstrip

Asymmetrical Stripl ine

Symmetrical Stripl ine
Single Ended Structure Examples (continued)
Differential Structure Examples

**Edge Coupled**
- Edge-Coupled Microstrip
- Edge-Coupled Asymmetrical Stripline
- Edge-Coupled Symmetrical Stripline
- Edge-Coupled Imbedded Microstrip

**Broadside Coupled**
- Broadside-Coupled Stripline
- Offset Broadside-Coupled Stripline
Trace Parameters

<table>
<thead>
<tr>
<th></th>
<th>10 mil trace</th>
<th>20 mil trace</th>
<th>100 mil trace</th>
</tr>
</thead>
<tbody>
<tr>
<td>Capacitance</td>
<td>2.2 pF/in</td>
<td>3.3 pF/in</td>
<td>11.6 pF/in</td>
</tr>
<tr>
<td>Inductance</td>
<td>9.9 nH/in</td>
<td>7.2 nH/in</td>
<td>2.4 nH/in</td>
</tr>
</tbody>
</table>

Notes:
1. Trace is 1 oz electrodeposited copper, microstrip.
2. FR-4 dielectric, $\varepsilon_r = 4.5$, $h = 10$ mils.

When are traces considered transmission lines and when are they considered lumped elements?
At low frequencies, traces are treated as lumped elements
- Signal voltages are essentially at the same potential at any point on the PWB
  - e.g. 6x12 cm cell phone, wavelength of 20 kHz audio is 15 km

High frequencies, traces are treated as transmission lines
- Signal wavelength is close to (or smaller than) the physical PWB size
- Signal voltage is no longer uniform across PWB
- PWB traces must be viewed as transmission lines
  - e.g. 6x12 cm cell phone, wavelength of 28 GHz 5G carrier is 11 mm

Size and wavelengths are not to scale given in example
When rise and fall times \((t_r \text{ and } t_f)\) are slow, traces and pads are treated as lumped elements

- \(t_r \text{ and } t_f \gg 2t_d\) (\(t_d\) is the delay time from source to end of line)
- Reflected waves are “lost” in the rising and falling edges
- Impedance matching may be less critical for signal integrity

Fast rise and fall times, traces are treated as transmission lines

- \(t_r \text{ and } t_f << 2t_d\)
- Impedance matching is more critical for signal integrity

Example

- Three cascaded traces, each 1 ns delay (\(2t_d=6\) ns)
- High Z load taps
- Plots show waveforms at each tap

Fast rise and fall times \((t_r \text{ and } t_f = 0.1 \text{ ns})\)

Slow rise and fall times \((t_r \text{ and } t_f = 25 \text{ ns})\)
PWB Traces as Transmission Lines

- PWB trace transmission line model
  - Dielectric Loss (G) per unit length
  - Trace Copper Loss (R) per unit length
  - Trace series inductance (L) per unit length
  - Trace capacitance (C) per unit length

- Schematic representation

- Characteristic Impedance

\[ Z_0 = \sqrt{\frac{R + j\omega L}{G + j\omega C}} \]

or when \( R \to 0 \) and \( G \to 0 \)

\[ Z_0 = \sqrt{\frac{L}{C}} \]
Impedance Determined By
- Topology (Stripline, Microstrip, Coplanar Waveguide, etc.)
- Dielectric constant of PWB material ($\varepsilon_r$)
- Dielectric height ($h$)
- Conductor width ($w$)
- To a small extend, conductor thickness ($t$)

Impedance Control Considerations
- Delivering max power to load
- Maintaining signal integrity
- Prevent excessive driver loading
Stripline & Microstrip Impedance

For Micro-Strip:

\[ Z_0 = \frac{87}{\sqrt{\varepsilon_r + 1.41}} \ln \left( \frac{5.98h}{0.8w + t} \right) \]

when \( 0.1 \frac{w}{h} < 2.0 \) and \( 1 < \varepsilon_r < 15 \)

For Strip-Line:

\[ Z_0 = \frac{60}{\sqrt{\varepsilon_r}} \ln \left( \frac{1.9b}{0.8w + t} \right) \]

when \( \frac{w}{h} < 0.35 \) and \( \frac{t}{h} < 0.25 \)
Asymmetrical Stripline Impedance

\[
\begin{align*}
Z_0 &= \sqrt{\frac{\mu_0}{\varepsilon_0}} \frac{\cosh^{-1}\left[\sin\left(\frac{\pi(b-s)}{2b}\right)\coth\left(\frac{\pi d_0}{2b}\right)\right]}{2\pi\sqrt{\varepsilon_r}} \\
&= \sqrt{\frac{\mu_0}{\varepsilon_0}} \frac{\cosh^{-1}\left[\sin\left(\frac{\pi(b-s)}{2b}\right)\coth\left(\frac{\pi d_0}{2b}\right)\right]}{2\pi\sqrt{\varepsilon_r}} \\
d_0 &= w\left(0.5008 + 1.0235\left(\frac{t}{w}\right) - 1.0230\left(\frac{t}{w}\right)^2 + 1.1564\left(\frac{t}{w}\right)^3 - 0.4749\left(\frac{t}{w}\right)^4\right) \\
\text{when } \frac{w}{b-t} < 0.35
\end{align*}
\]
Impedance Examples

- **Symmetrical Stripline**
  50 Ω, 11 mils wide
  (15+15=30 mil dielectric)

- **Asymmetrical Stripline**
  50 Ω, 9 mils wide
  (10+20=30 mil dielectric)

- **Microstrip**
  50 Ω Microstrip, 54 mils wide
  (30 mil dielectric)

*Notes:*
1. Copper: 1 oz, electro-deposited
2. FR4 dielectric constant: 4.50
AC Loss

- AC loss due to three mechanisms
  - Dielectric Loss (loss tangent of PWB material)
  - Conductor Loss (resistive, skin effect, roughness)
  - Radiation Loss (typically negligible portion of loss)
- Loss can be a concern in digital applications
  - High speed
  - Long trace runs
  - and/or fine width lines
- Loss can be a concern in analog/RF applications
  - Gain/loss budgets in RF and IF paths
  - LO distribution loss
  - Video, ADC or DAC scaling
## Dielectric and Copper Loss Examples

<table>
<thead>
<tr>
<th>Frequency</th>
<th>FR4 Copper Loss</th>
<th>FR4 Dielectric Loss</th>
<th>FR4 Total Loss</th>
<th>Rogers RO4350B Copper Loss</th>
<th>Rogers RO4350B Dielectric Loss</th>
<th>Rogers RO4350B Total Loss</th>
</tr>
</thead>
<tbody>
<tr>
<td>10 MHz</td>
<td>0.005</td>
<td>0.001</td>
<td>0.006</td>
<td>0.005</td>
<td>0.000</td>
<td>0.005</td>
</tr>
<tr>
<td>100 MHz</td>
<td>0.017</td>
<td>0.012</td>
<td>0.029</td>
<td>0.017</td>
<td>0.002</td>
<td>0.019</td>
</tr>
<tr>
<td>1 GHz</td>
<td>0.068</td>
<td>0.123</td>
<td>0.191</td>
<td>0.070</td>
<td>0.016</td>
<td>0.086</td>
</tr>
<tr>
<td>10 GHz</td>
<td>0.309</td>
<td>1.227</td>
<td>1.536</td>
<td>0.322</td>
<td>0.160</td>
<td>0.482</td>
</tr>
</tbody>
</table>

*FR4 dielectric loss exceeds copper loss at 1 GHz*

*The fundamental of a 10 GHz clock will be attenuated by >6 dB over a 4” trace length*

**Notes:**
1. Copper: 1 oz, electrodeposited, 10 mil width, 50 Ohms, stripline
2. FR4 dielectric constant: 4.50, loss tangent 0.025, height 28 mils
3. 4350 dielectric constant: 3.48, loss tangent 0.0037, height 22 mils
4. Loss units are dB/inch
**Conductor Loss**

- **DC Resistance**
  - Function of conductivity, length and cross sectional area
  \[
  R_{DC} = \rho \frac{l}{tw} = \rho \frac{l}{A}
  \]
  \[
  R_{DC} = 0.679 \mu \Omega \frac{12\text{in}}{(0.0014\text{in})(0.010\text{in})} = 0.6\Omega
  \]
  \[
  R_{DC} = 0.679 \mu \Omega \frac{12\text{in}}{(0.0007\text{in})(0.005\text{in})} = 2.3\Omega
  \]

- **Skin Depth**
  - Function of frequency, conductivity & permeability (copper permeability \(\mu_r \approx 1\))
  - Effects AC resistance
  - Defined as point where current density drops to 37% (1/e)
  - Typically can be ignored if \(t<2\delta\)
  \[
  \delta = \sqrt{\frac{\rho}{\pi f \mu_0 \mu_r}}
  \]
  \[
  \delta = \sqrt{\frac{0.0172 \mu \Omega m}{\pi(10\text{MHz}) \left(4\pi \times 10^{-7} \frac{\Omega}{\text{m}}\right)}} = 21\mu\text{m} = 0.8\text{mils}
  \]
  \[
  \delta = \sqrt{\frac{0.0172 \mu \Omega m}{\pi(10\text{GHz}) \left(4\pi \times 10^{-7} \frac{\Omega}{\text{m}}\right)}} = 660\text{nm} = 0.03\text{mils}
  \]

Current Density Distribution at DC

Current Density Distribution at High Freq

Low | | | High

Current Density
Loss due to Skin Effect & Roughness

Loss per Inch Over Frequency for Various Copper Thickness Values

- 1.00 oz
- 0.50 oz
- 0.25 oz

Loss per Inch Over Frequency for Various Copper Roughness Values

- 0.000” RMS
- 0.016” RMS
- 0.130” RMS

Stripline

- \( \varepsilon_r = 4.6 \)
- \( \delta = 0.011 \)
- \( h = 30 \) mils
- \( w = 10.5 \) mils
- \( R = 0.055” \) RMS

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Time Delay

\[ t_d = \sqrt{\frac{L_0 C_0}{c}} = 85 \sqrt{\varepsilon_{\text{r-effective}}} \text{ ps/inch} \]

Where:
- \( t_d \): time delay per unit length
- \( \varepsilon_{\text{r-effective}} \): Effective Relative Dielectric constant
- \( c \): Speed of Light

- \( L_0 \): Inductance per unit length
- \( C_0 \): Capacitance per unit length

**Effective Relative Dielectric Constant**

\[ \varepsilon_{\text{r-effective}} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2} \left( \frac{1}{\sqrt{1 + \frac{12h}{w}}} \right) \]

when \( \frac{w}{h} \geq 1 \)

**FR4 Example**
- \( \varepsilon_r = 4.5, w = 18 \text{ mils}, h = 10 \text{ mils} \)
- \( t_d = 112 \text{ ps/inch} \)

**Microstrip**

**Buried Microstrip**

**Stripline**

\[ \varepsilon_{\text{r-effective}(\text{microstrip})} < \varepsilon_{\text{r-effective}(\text{buried microstrip})} < \varepsilon_r \]

\[ t_d = 85 \sqrt{\varepsilon_r} \text{ ps/inch} \]

**FR4 Example**
- \( \varepsilon_r = 4.5 \)
- \( t_d = 180 \text{ ps/inch} \)
Signal Dispersion

- Frequency Dependent Dielectric Constant
  - Propagation velocity is frequency dependent
  - PWB acts as a dispersive medium
- Becomes an issue
  - Long Trace Runs
  - High Speed Data/Clocks
  - Critical Analog
- Constant time delay is necessary to ensure that signals arrive undistorted at the destination
- Issue further exasperated by frequency dependent attenuation
Eye Diagram
- Provides a visual means to quickly evaluate signal integrity
- Generated by superimposing successive digital waveforms to create a composite image (i.e. an oscilloscope image with infinite persistence)

Eye Diagram Example
- 4.8 Gbps
- 36” trace length
- Three different PWB dielectrics

FR4  
Rogers 4350  
Arlon CLTE
Mitigation of Dispersion and Attenuation

- More Stable Dielectric
- Wider Traces
- Pre-Emphasis Filter at the source
- Equalizer at the destination
  - e.g. Maxim MAX3784 (40” length, 6 mil, FR4, 5 Gbps)
A standardized serial interface between data converters (ADCs and DACs) and logic devices (FPGAs or ASICs) to reduce the number of I/O between devices

Accomplished by serializing large amounts of parallel data with 8b/10b Encoding (data rates up to 12.5 Gbps)

Advantages include

- Greatly reduced I/O count
- Reduced number of meandering traces to ensure alignment

32-bit data bus on 4 layers with meandering lines to equalize delay

Courtesy TI
Example
- I/Q 16-bit data on two receiver channels sampling at 80 MHz
- \(2 \times 16 \times 2 \times 80 \text{ MHz} \times \frac{10}{8} = 6.4 \text{ GHz}\) (one serial signal replaces \(2 \times 16 \times 2 = 64\))

JESD204B receiver includes an equalizer to reduce dispersion effects and frequency dependent attenuation both of which are deterministic.

Relatively easy to achieve high data rates between devices on the same PWB especially on the same side.
- No vias, minimal discontinuities

However, the equalizer cannot effectively compensate for impedance discontinuities
- Care must be taken to ensure a consistent impedance from the JESD204B transmitter to receiver especially in cases where the signals must propagate through multiple connectors.
Traces run in close proximity will couple

Coupling is determined by geometry
- Trace separation, distance to ground(s) & parallel length

Most efficient coupling occurs at $\lambda/4$
- For lower frequencies (wavelength longer than $\lambda/4$) coupling diminishes with a slope of 20 dB/decade
- For higher frequencies (wavelength shorter than $\lambda/4$) coupling will reach a minimum and maximum every $\lambda/4$, with the peak couplings never exceeding that at $\lambda/4$.

Notes:
1. Material FR4, $\varepsilon_r = 4.5$
2. Parallel length = $\lambda/4 = 1.39$" at 1 GHz
3. $t = 1.4$ mils
4. $h = 30$ mils (15 + 15)
5. $s = 30$ mils
6. $w = 11$ mils
7. Both lines 50 $\Omega$ terminated at both ends
Quarter Wave Coupling/Isolation
Examples

- **Stripline**
  11 mil width
  \( \lambda/4 \approx 1.39'' \)

- **Microstrip**
  54 mil width
  \( \lambda/4 \approx 1.60'' \)

<table>
<thead>
<tr>
<th>s</th>
<th>Coupling/Isolation</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.011''</td>
<td>18 dB</td>
</tr>
<tr>
<td>0.030''</td>
<td>35 dB</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>s</th>
<th>Coupling/Isolation</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.030''</td>
<td>18 dB</td>
</tr>
<tr>
<td>0.150''</td>
<td>35 dB</td>
</tr>
</tbody>
</table>

To achieve same level of isolation much greater separation is required with microstrip.

In both the above cases, copper is 1 oz electrodeposited, FR4 dielectric (\( \varepsilon_r = 4.50, h = 0.030'' \)) and \( F = 1.0 \text{ GHz} \).
Mitigation of Coupling

- Separation of traces
- Reduce length of parallel run (to a point, $\lambda$ dependent)
- On adjacent layers, run traces orthogonally
- Run traces on separate non-adjacent layers
  - Preferably with a ground plane in between
- Run guard trace
  - Ground trace between lines
- Shield (for microstrip)
- Dielectric height allocation

Most Coupling

Least Coupling
For differential pairs, tight coupling is desired

- Lower cross-talk, lower radiation
- Common mode noise rejection
- Reduces ground reference problems
- Useful in high dynamic range analog applications
  - Log Amplifiers
  - High Resolution ADC/DAC
  - Transducers
- Useful in high speed digital applications
  - Low amplitude clocks
  - Low jitter requirements
Differential Pair Routing Options

- Geometry and spacing defined by artwork
- High differential impedance easily achievable
- Impedance reduced as “s” is reduced
- As “s” is increased, impedance approaches 2x single ended impedance
- Difficult to rout through fine pitch holes

- Geometry is effected by layer registration
- Low differential impedance easily achievable
- Easy to route, easy to maintain matched lengths
Differential Impedance Definitions

- **Single-Ended Impedance** \((Z_0)\)
  Impedance on a single line with respect to ground when not coupled to another line
  \[ Z_0 = \sqrt{Z_{Odd} Z_{Even}} \]

- **Differential Impedance** \((Z_{DIF})\)
  The impedance on one line with respect to the coupled line, when the lines are driven by equal and opposite signals
  \(Z_{DIF} = 2Z_{Odd}\)

- **Odd Mode Impedance** \((Z_{Odd})\)
  Impedance on a single line with respect to ground when the other coupled line is driven by equal and opposite signals
  \(Z_{DIF} = 2Z_{Odd}\)

- **Common Mode Impedance** \((Z_{CM})\)
  Impedance of the two lines combined with respect to ground

- **Even Mode Impedance** \((Z_{Even})\)
  The impedance on one line with respect to ground when the coupled line is driven by an equal and in-phase signal
  \(Z_{Even} = 2Z_{CM}\)
Differential Impedance Examples

<table>
<thead>
<tr>
<th>S</th>
<th>Z_{Even}</th>
<th>Z_{Odd}</th>
<th>Z_0</th>
<th>Z_{Diff}</th>
</tr>
</thead>
<tbody>
<tr>
<td>100</td>
<td>49.4</td>
<td>49.4</td>
<td>49.4</td>
<td>98.8</td>
</tr>
<tr>
<td>25</td>
<td>50.9</td>
<td>47.9</td>
<td>49.4</td>
<td>95.8</td>
</tr>
<tr>
<td>10</td>
<td>56.4</td>
<td>41.9</td>
<td>48.6</td>
<td>83.8</td>
</tr>
</tbody>
</table>

Edge Coupled

<table>
<thead>
<tr>
<th>S</th>
<th>Z_{Even}</th>
<th>Z_{Odd}</th>
<th>Z_0</th>
<th>Z_{Diff}</th>
</tr>
</thead>
<tbody>
<tr>
<td>20</td>
<td>41.3</td>
<td>34.7</td>
<td>37.8</td>
<td>69.4</td>
</tr>
<tr>
<td>10</td>
<td>68.6</td>
<td>34.7</td>
<td>48.8</td>
<td>69.4</td>
</tr>
</tbody>
</table>

Broadside Coupled

Even mode

Odd mode

Reduced Spacing

Ohms
Near Field Stripline Differential Pair

- **Lines are far apart**
  - Most of the electric field is concentrated between ground planes and conductors
  - Little magnetic field interaction
  - Most or all current is returned through the ground plane

- **Lines are very close**
  - Most of the electric field is concentrated between the conductors
  - Less of the field is concentrated between the ground planes and the conductors
  - In practice, this can be difficult to achieve on PWBs (because of the high dielectric height, close trace proximity and/or thin lines required)

- **As the lines are brought closer and/or the ground planes are brought further apart**
  - More of the electric field is concentrated between the conductors
  - Less of the field is concentrated between the ground planes and the conductors

Magnetic Field

Electric Field
### Pad Parameter Examples

<table>
<thead>
<tr>
<th>Imperial Size Des</th>
<th>Metric Size Des</th>
<th>Component Size (LxW)</th>
<th>Pad Size (LxW)</th>
<th>Pad Cap (pF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>01005</td>
<td>0402</td>
<td>0.016x0.008 in 0.40x0.20 mm</td>
<td>0.010x0.008 in 0.25x0.20 mm</td>
<td>0.03</td>
</tr>
<tr>
<td>0201</td>
<td>0603</td>
<td>0.02x0.01 in 0.60x0.30 mm</td>
<td>0.018x0.017 in 0.46x0.42 mm</td>
<td>0.09</td>
</tr>
<tr>
<td>0402</td>
<td>1005</td>
<td>0.04x0.02 in 1.00x0.50 mm</td>
<td>0.024x0.024 in 0.62x0.62 mm</td>
<td>0.15</td>
</tr>
<tr>
<td>0603</td>
<td>1608</td>
<td>0.06x0.03 in 1.60x0.80 mm</td>
<td>0.037x0.039 in 0.95x1.00 mm</td>
<td>0.35</td>
</tr>
<tr>
<td>0805</td>
<td>2012</td>
<td>0.08x0.05 in 2.00x1.25 mm</td>
<td>0.045x0.057 in 1.15x1.45 mm</td>
<td>0.60</td>
</tr>
<tr>
<td>1206</td>
<td>3216</td>
<td>0.12x0.06 in 3.20x1.60 mm</td>
<td>0.045x0.07 in 1.15x1.80 mm</td>
<td>0.74</td>
</tr>
<tr>
<td>1210</td>
<td>3225</td>
<td>0.12x0.10 in 3.20x2.50 mm</td>
<td>0.045x0.11 in 1.15x2.70 mm</td>
<td>1.14</td>
</tr>
<tr>
<td>1812</td>
<td>4532</td>
<td>0.18x0.12 in 4.50x3.20 mm</td>
<td>0.055x0.14 in 1.40x3.50 mm</td>
<td>1.75</td>
</tr>
<tr>
<td>2220</td>
<td>5650</td>
<td>0.22x0.20 in 5.70x5.00 mm</td>
<td>0.059x0.21 in 1.50x5.40 mm</td>
<td>2.80</td>
</tr>
<tr>
<td>2225</td>
<td>5664</td>
<td>0.22x0.25 in 5.60x6.40 mm</td>
<td>0.059x0.27 in 1.50x6.80 mm</td>
<td>3.60</td>
</tr>
</tbody>
</table>

- Pads are typically larger in X and Y dimensions than the component contact areas.
- Sensitive applications may require that the pad characteristics be considered.
- Land size is in accordance with IPC-7351, Density Level B.
- Pad capacitance is based on 1 oz copper, stripline on FR4 ($\varepsilon_r = 4.50, h = 5$mils).

Increasing pad capacitance
0.8 mm Pitch BGA (FCBGA) Package Example

- DAC38RF83
- 144 contact points
- 0.8 mm (0.031”) pitch
- Overall size is 10.15 mm sq (0.400” square)

Courtesy of TI
1 mm Pitch BGA (FFVH1760) Package Example

- 1,760 contact points
- 1 mm (0.0394") pitch
- Overall size is 42.5 mm sq (1.673" square)

Courtesy of Xilinx
Reduces peak current demands on the driver
Driving waveform is halved by the series resistor at the start of propagation (assuming $R_s=Z_0$)
Driving signal propagates at half amplitude to end of line
At end reflection coefficient is +1
Eventually all points reach full amplitude as the reflected wave propagates back to the source
Driving waveform propagates at full intensity over trace facilitating first-incident switching

Reflections dampened by end termination

Received voltage is equal to transmitting voltage at all points (ignoring losses)

Increased peak current demands on driver

Steady-state drive current can be reduced by the use of a Thevenin termination
“Intentional” Mismatch Example

- Five selectable sources
- Four destinations
- Modeled signal paths
  - CCA PWB
  - Back Plane PWB
  - Connectors
  - Driver
- Took advantage of relatively slow clock (30 MHz)
“Intentional” Mismatch Example

- Allow reflections to dissipate before clocking data (Clocks distributed point-to-point)
Power Distribution, Power Integrity (PI) and Grounding

PI is a set of measures to ensure the required voltage and current are distributed from the source to the load(s).
Power Distribution Purpose

- To distribute the supply voltages necessary to all components within the required regulation
- To provide a reliable reference (ground) for all circuitry
  - Which is also a part of Signal Integrity
Supply Power Loss Budget

- Distribution loss contributes to supply voltage error delivered to CCA components
- Complete loss budget needs to be established, especially in high power applications
  - Power Supply Voltage Tolerance
  - Harnessing Loss
  - Connector Loss
  - Backplane Loss
  - PWB Loss on CCA

- Remote Sensing
  - Compensate for some losses
  - Location important
  - “Open Sense” protection
Backplane PWB DC Loss Model

Voltage drop across backplane is simulated with PSpice grid model (shown for reference)

PSpice simulation results showing voltage distribution across backplane
Dedicated adjacent planes for ground and supply voltage
- Establishes low inductance distribution
- Parallel planes create distributed capacitance (which supplement decoupling capacitors)
- e.g. DuPont HK04M
  - 12 µm (0.5 mil)
  - $\varepsilon_r = 4.0$
  - Yields 240 pF/cm$^2$
  - By virtue of thin material, distributed inductance is minimized

Through-holes perforate planes
- Increases resistance

Distributing supplies for analog/RF
- Rout power traces between ground planes
Plane Capacitance, Inductance, Resistance

**Inductance**

\[ L = \mu_0 \mu_r \frac{h}{W} \quad \mu_0 = 4\pi \times 10^{-7} \frac{H}{m} = 0.32 \frac{nH}{in} \]

**Resistance**

\[ R_{DC} = \rho \frac{l}{tw} = \rho \frac{l}{A} \quad \rho = 0.0172 \mu \Omega - m = 0.679 \mu \Omega - \text{in} \]

Allowing \( l = w \) permits calculation of Resistance per square

\[ R_{DC \text{ per Square}} = \rho \frac{1}{t} = (0.679 \mu \Omega - \text{in}) \frac{1}{0.0014 \text{ in}} = 485 \mu \Omega / \text{Square} \]

Example is for 1 ounce copper which is 0.0014” thick

**Capacitance**

\[ C = \varepsilon_0 \varepsilon_r \frac{LW}{h} = \varepsilon_0 \varepsilon_r \frac{A}{h} \quad \varepsilon_0 = 8.85 \times 10^{-12} \frac{F}{m} = 225 \times 10^{-15} \frac{F}{\text{in}} \]

### FR4 Dielectric Thickness (mils)

<table>
<thead>
<tr>
<th>FR4 Dielectric Thickness (mils)</th>
<th>Plane Inductance (pH/square)</th>
<th>Plane Capacitance (pF/inch²)</th>
</tr>
</thead>
<tbody>
<tr>
<td>8</td>
<td>260</td>
<td>127</td>
</tr>
<tr>
<td>4</td>
<td>130</td>
<td>253</td>
</tr>
<tr>
<td>2</td>
<td>65</td>
<td>506</td>
</tr>
</tbody>
</table>
Physical capacitors have parasitic elements that limit their ability to stabilize supply lines.

For power integrity, a simplified capacitor model is normally adequate:
- Equivalent series inductance (ESL)
- Equivalent Series Resistance (ESR)
- Actual capacitance (C)

Capacitor model showing C, EPR, ESR, ESL, R_{DA}, C_{DA} and C_{PAD} - may be more suitable for signal integrity and analog circuit analysis.

Simplified capacitor model showing C, ESR and ESL is typically adequate for power integrity analysis.
## Capacitor Parameters

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Type</th>
<th>Package</th>
<th>Cap (uF)</th>
<th>Voltage (V)</th>
<th>ESL (nH)</th>
<th>ESR (mΩ)</th>
<th>SRF (MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>C0603X7S1A104K030BC, TDK</td>
<td>X7S Ceramic</td>
<td>0201</td>
<td>1.0</td>
<td>10</td>
<td>0.06</td>
<td>50</td>
<td>20.0</td>
</tr>
<tr>
<td>C0402C104K3RACTU, Kemet</td>
<td>X7R Ceramic</td>
<td>0402</td>
<td>0.10</td>
<td>25</td>
<td>0.2</td>
<td>22</td>
<td>34.8</td>
</tr>
<tr>
<td>C0603C474K4RACTU, Kemet</td>
<td>X7R Ceramic</td>
<td>0603</td>
<td>0.47</td>
<td>16</td>
<td>0.4</td>
<td>13</td>
<td>11.6</td>
</tr>
<tr>
<td>C0805C224K1RACTU, Kemet</td>
<td>X7R Ceramic</td>
<td>0805</td>
<td>0.22</td>
<td>100</td>
<td>2.3</td>
<td>13</td>
<td>7.1</td>
</tr>
<tr>
<td>C1206C225K5RACTU, Kemet</td>
<td>X7R Ceramic</td>
<td>1206</td>
<td>1.0</td>
<td>50</td>
<td>4.0</td>
<td>12</td>
<td>2.5</td>
</tr>
<tr>
<td>C1812C475K5RACTU, Kemet</td>
<td>X7R Ceramic</td>
<td>1812</td>
<td>4.7</td>
<td>50</td>
<td>0.7</td>
<td>8</td>
<td>2.7</td>
</tr>
</tbody>
</table>

**Self Resonant Frequency**

\[ f_{SRF} = \frac{1}{2\pi\sqrt{LC}} \]

**Quality Factor, Dissipation Factor**

\[ Q = \frac{1}{DF} = \frac{X_C}{R} = \frac{1}{2\pi f C R} \]

**Kemet Capacitor Simulation Tool**
Variables that effect parasitic inductance of a capacitor

- Inductance increases with increasing package height
- Inductance increases with increasing length
- Inductance decreases with increasing width
- Inductance increases with increasing distance between capacitor and ground plane
- ESL parameter is actual a “Partial Inductance”

PI Guidelines to minimize parasitic inductance

- Minimize connection lengths
- Eliminate or minimize sharing of vias
- Tend towards using the shortest/lowest/widest package available
Capacitor Mounting Pads

7.2 nH/in for 20 mil trace in addition to via and pad inductance

Notes:
1. Copper: 1 oz, electrodeposited, microstrip
2. FR4 dielectric constant: 4.50, loss tangent 0.025, height 10 mils
Decoupling Examples

- 100 MHz Logic Device, 100 mA to 150 mA step load change

<table>
<thead>
<tr>
<th>Capacitance Configuration</th>
<th>Ripple Voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td>6.8 uF</td>
<td>1 Vpp</td>
</tr>
<tr>
<td>6.8 uF + 0.1 uF</td>
<td>0.3 Vpp</td>
</tr>
<tr>
<td>6.8 uF + 0.1 uF + 0.01 uF</td>
<td>0.1 Vpp</td>
</tr>
<tr>
<td>6.8 uF + 0.1 uF + 0.01 uF w/ long traces</td>
<td>1.1 Vpp</td>
</tr>
</tbody>
</table>

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Current Carrying Capability of PWB Traces

- Influenced by
  - Trace Cross section \((w, t)\)
  - Position of trace (outer layer, inner layer)
  - Maximum acceptable temperature rise

- IPC-2221, Figure 6-4, can be used as general guideline
- Thermal modeling may be needed in critical applications
**Application**

- Inner trace, 1 ounce, maximum fault current is 2 Amps
- Max CCA temp +90 °C, max PWB temp +150 °C, Margin 30 °C
- Allowable Temp rise = 150–90–30=30 °C

**Determine Cross Section from “C” is 56 sq mils**

**Determine width from “B” to be 40 mils**
References
References

- IPC-2221 Generic Standard on Printed Board Design
- IPC-2222 Sectional Design Standard for Rigid Organic Printed Boards
- IPC-2223 Sectional Design Standard for Flexible Printed Boards
- IPC-4101 Specification for Base Materials for Rigid and Multi-Layer Printed Boards
- IPC-7351 Generic Requirements for Surface Mount Design and Land Pattern Standard
- High Speed Digital Design, Howard W Johnson
  - Even Mode Impedance, Polar Instruments, Application Note AP157
- Effect of Etch Factor on Printed Wiring, Steve Monroe, 11th Annual Regional Symposium on EMC
- Transmission Line Design Handbook, Brian C Wadell
- Impact of PWB Construction on High-Speed Signals, Chad Morgan AMP/Tyco
- Transmission Line RAPIDESIGNER Operation and Applications Guide (AN-905) National Semiconductor
- PWB Design and Manufacturing Considerations for High Speed Digital Interconnection, Tom Buck, DDI
- Power Distribution System Design (XAPP623) Mark Alexander, Xilinx
- LTSpice
- DAC38RFxx Dual- or Single-Channel, Single-Ended or Differential Output, 14-Bit, 9-GSPS, DAC Datasheet
- EETimes - Channel compensation methods used in JESD204B converters
- JESD204B Overview (ti.com)
- C1206C104J3GACTU.pdf (kemet.com)
- Copper Foils for High Frequency Materials