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Editor's Note:
James Colotti coined the term dBFS in the early 1980's, during his development of evaluation techniques for high-speed A/D and D/A Converters. During this lecture, Mr. Colotti introduced the term to industry.

DIGITAL DYNAMIC ANALYSIS OF A/D CONVERSION SYSTEMS THROUGH EVALUATION SOFTWARE BASED ON FFT/DFT ANALYSIS

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INTRODUCTION

Data sheet specifications of A/D Converter Systems can be difficult to interpret when considering a device for a specific application. However, with the evaluation software described in this article, A/D Converter performance can be easily and efficiently evaluated under specific test conditions.

Applications of Analog-to-Digital (A/D) Converter Systems are growing rapidly both in quantity and sophistication. Manufacturers find themselves specifying more and more parameters for this critical link between the Analog and Digital worlds. Aperture jitter, aperture time delay, harmonic distortion, linearity and other specifications must be carefully evaluated to ensure that the correct A/D Conversion system is selected for a specific application. The sought after A/D Conversion system may consist of a separate Sample and Hold (S/H) Amplifier and A/D Converter or a single hybrid that contains both. Since overall performance of the host system is often dependent on the A/D system performance, this selection process is critical.

Unfortunately, data sheet specifications of A/D Converter Systems and components often yield insufficient characterization information for a specific application that one is interested in. For example, if the harmonic distortion of an A/D is specified at a 1 MHz sampling rate with a 10 kHz full scale input, how will the converter perform at a 409.6 kHz sampling rate with a 14 kHz input at -6 dBFS (dB below full scale) ? This characterization problem can be compounded when a separate A/D Converter and S/H are being considered.

The only effective way to resolve these uncertainties is to test the A/D Conversion System under the specific conditions that are required by the application. One method of accomplishing this test would be the Reconversion Approach depicted in figure 1, where the digital output of the A/D is fed into the digital input of a D/A for conversion back into the analog domain. The D/A output is subsequently monitored with a spectrum analyzer and true RMS voltmeter. One disadvantage to this approach is that the D/A will contribute error to the measurement process especially when evaluating high speed (over 1 MHz) A/D converters in the 12-16 bit resolution range[1]. Another problem is that measuring Intermodulation Distortion (IMD), Harmonic Distortion (HD), and narrow band noise can be cumbersome especially in the presence of foldover.

A much more effective way to test an A/D would be to monitor the A/D

output with a computer which evaluates performance through specialized evaluation software. The A/D output remains in the digital domain, thus this approach actually provides an ideal method of testing since the requirement that round off errors be significantly less than the evaluation limits, is easily met. In addition, parameters such as Wide Band Noise, Narrow band Noise, Intermodulation Distortion and Harmonic Distortion are all calculated by the Software, conveniently providing useful information that is more difficult to obtain on most spectrum analyzers.

It is this digital evaluation approach that shall now be explored in detail. Being that the A/D output remains in the digital domain, and the test is performed under dynamic conditions, this evaluation approach shall be referred to as **Digital Dynamic Evaluation.**

A Look at the Hardware

Digital Dynamic Evaluation of an A/D Conversion system begins with the hardware illustrated in Figure 2. In this test set up, an analog signal (usually one or two high quality sine waves) are inputted to the A/D Converter system. The digital data, up to 16 Bits wide, is inputted to the 4096 x 16 Buffer Memory at the required converter rate. The 16 BIT wide data bus is large enough to accommodate most A/D Converter systems presently available. The memory buffer is usually necessary since required A/D conversion rates often exceed the maximum data rate of most computer interfaces. Once the data is loaded into this buffer memory, the computer reads and processes this data and outputs the results on the plotter. Note that with this evaluation approach, the A/D output is stored and processed digitally, eliminating the need to convert back into the analog domain.

The A/D evaluation described in this article is essentially divided into two parts; harmonic-distortion/noise testing and intermodulation distortion testing. During the former test, one sine wave is inputted into the A/D. The software detects the presence of the single signal and subsequently performs the harmonic test and noise tests. During the latter test, two sine waves of similar amplitude are inputted. The software detects the presence of two signals and thus performs the intermodulation distortion test. Once the tests are completed , the results are plotted.

A Look at the Software

The block diagram of the Evaluation software shown in figure 3 summarizes the various functions of the program, while figure 4 contains the actual program listing written in HPL.

When the program is initiated, the user is given the option of modifying the default values of the sampling rate (F_S) and number of data points (N) to be read from the buffer. Since the data is read out of a buffer, usually at a data rate different then the conversion rate, the program must know the actual sampling rate to correctly scale the results. Our application usually required a 409.6 kHz sampling rate, thus I chose this as the default value. The operator also can modify the number of data points, however due to the nature of the Fast Fourier Transform (FFT) algorithm used in the program, this number is restricted to powers of 2. There also exists a practical lower limit to this number, usually 256 data points to yield meaningful results, and an upper limit

of 4096 due to the buffer memory size and the designated array size of Q[I]. This dictates that the operator's choice of number of data points is 2^8 = 256, 2^9 = 512, 2^{10}= 1024, 2^{11}= 2048 and 2^{12}=4096. A more detailed discussion of the criteria for choosing the number at data points is given later.

Once the sampling rate and number at data points are determined, the option of reading data or running a simulation is given. The simulation is useful as a reference to ascertain the program's output for the "ideal" Converter. The two 'ideal' sine waves created by the software are of amplitude and frequency chosen by the operator. While being generated, the sine waves are summed and loaded into the Q[I] array, as would the A/D Converter data. If the operator chooses to read the data from the A/D Converter under test, then the simulation is bypassed and the Converter data is inputted from the buffer to the Q[I] array. Before processing the data, the 'SATURATION TEST' subroutine is executed. If any data point is at either of the saturation limits (ie -2048 or +2047), then the r9 variable is set to 1 indicating that saturation is either imminent or present. The operator is then given the option of continuing the program or starting over. The saturation test is important especially when testing with large input signals close to the full scale limits. Under this condition inadvertent saturation can occur since slight variations in signal level can cause these limits to be exceeded. In some cases however, it may be required to saturate the A/D to analyze its saturation characteristics.

Since it is unlikely that an integer number of cycles of the input wave is contained in the sampling period, there shall exist a discontinuity at the ends of the data sample (see figure 5). This violates the FFT requirement of continuity - creating errors known as leakage or sidelobe errors. To solve the discontinuity problem the data is weighted with a Hanning Window before the FFT is executed. This eliminates the discontinuity by gradually reducing the data at the ends of the sampling period, while passing the data at the center essentially unchanged. Since the data is zero at the ends, the discontinuity and its associated errors are eliminated. See the 'Hanning' appendix for additional details.

After the Hanning Window weighting function, the FFT is performed. The primary function of the FFT subroutine is to process the N data points of the Q[I] array that represent the time domain function of the input and convert this data into a set of data points that represent the frequency domain of tne input. Each of the N points of the FFT output represents the energy in each of the N bins that subdivide the Fs/2 bandwidth (see figure 6). The size of these "bins" is a function of both the sampling frequency and the number of data points. In the default mode, the sampling frequency is 409,600 Hz and the sample length is 1024 points. This dictates that the default bin size is 400 Hz as illustrated in the equation below.

$$\frac{\text{SAMPLING RATE}}{\text{\# OF SAMPLES}} = \text{BIN SIZE} \qquad \text{Equation 1}$$

$$\frac{409600}{1024} = 400 \text{ Hz}$$

The bin size is somewhat analogous to the resolution bandwidth of an analog Spectrum Analyzer. With the FFT however, these bins are stationary, whereas the spectrum analyzer sweeps continuously across the frequency band. The stationary characteristic of these bins can have a tendency to spread the energy of the wave when the fundamental frequency is not devisable by an integral number of bins. Ideally, when the fundamental frequency is an integral number of bins, the FFT output accurately represents the amplitude and frequency of the input. When this is not the case, the FFT "spreads" the energy of the fundamental into adjacent bins creating errors. The worst error would exist when the fundamental falls exactly between two bins (i.e., $F = (n + 0.5) F_{bin}$). This is demonstrated in figures 7 and 8. Figure 7 represents the FFT of a simulated sine wave of 40 kHz, -10 dB below full scale (-10 dBFS). Since 40 kHz is an integral multiple of the 400 Hz bin size, the spectrum appears sharp and the FFT accurately represents the amplitude of the peak. Figure 8 however represents the FFT of a 40.2 kHz sine wave, also -10 dBFS. Note the spreading effect which causes the inaccurate amplitude reading. Also note that this plot indicates that the fundamental frequency is 40.4 kHz not 40.2 kHz, an error due to the 400 Hz resolution. To avoid these problems and thus obtain accurate results, the fundamental should always be an integral number of bins.

Once the FFT is completed, the amplitude vs. frequency information is stored in the Q[I] array, the same array that once stored the time domain data. The FFT results are incremented through the "Find Peak" subroutine which, as the name implies, searches for the frequency component that corresponds to the largest amplitude. Beginning the search 4 bins from 0 Hz prevents the software from erroneously considering the DC component as the peak frequency, in cases where appreciable DC offset exists. After designating the maximum peak amplitude as C[1] of corresponding frequency r1, the peak subroutine then searches for the next largest component that is within 6 dB of the maximum peak. The second peak of amplitude C[7] and frequency r7, would be present during Intermodulation Distortion testing. Note that the variable Q is incremented by 1 each time a component within 6 dB of the peak is found, indicating the number of additional peaks. If no additional peaks are found (ie Q=0), the software would execute the Harmonic Distortion and noise tests. If one additional peak is found (ie Q=1), the software would execute the intermodulation distortion test. If more then one peak is found (is Q>1), then all of these tests are bypassed.

<u>If no additional peaks are found</u>

By not locating any additional peaks the software would initiate the Harmonic Distortion (HD) Subroutine. Recall that Harmonic Distortion is caused by the nonlinearity of an A/D System that is characterized by the appearance of frequencies in the output spectrum that are an integral multiple of the fundamental frequency as illustrated in figure 9.

$$f_n = nf_f \qquad \text{Equation 2}$$

where

f_n = undesired harmonic frequencies

f_f = frequency of fundamental

n = 2,3,4.....

The HD Subroutine locates the second and third harmonics of the fundamental, and stores their amplitudes as C[2] and C[3] of frequency r2 and r3 respectively. Only these harmonics are considered since they are the most prominent in most practical applications. This is fortunate since the additional harmonics can be cumbersome to locate especially in cases of multiple foldovers about Fs/2 and DC. By limiting the analysis to the 2nd and 3rd harmonics and by limiting the maximum fundamental frequency to $F_S/2$, the maximum number of possible foldovers is two, one at $F_S/2$ and one at DC. This simplifies the Harmonic Distortion Subroutine which need only account for these two foldovers.

Wide band noise is then calculated by the next subroutine. Note that during the FFT, the variable C[6] is used to sum the total energy contained in all the bins from DC to FS/2. Calculating the wide band noise begins by subtracting the DC component, the signal component and the corresponding harmonics from C[6]. The resulting C[6] is then divided by the remaining number of bins to obtain the average noise which is then converted to dB below full scale, dBFS.

The wide band noise parameter is especially useful in determining the instantaneous dynamic range (the ratio of the full scale level to the noise floor) of an A/D Converter system. It can be shown that the theoretical noise floor of a Converter is[2];

$$CNF = 1.76 + 6.02n + 10 \text{ Log } \frac{FS/2 \text{ BW}}{\text{FFT BW}} \qquad \text{Equation 3}$$

n = number of bits

CNF = converter noise floor in dB below FS

Unfortunately, converter noise floor may vary significantly from the theoretical value due to aperture uncertainty, amplifier noise, missing codes, and other variables.

One of the limitations to the average wide band noise calculation is that it reveals little information about the noise level at a specific frequency or range of frequencies. In some cases, the wide band noise can differ significantly from the noise in a specific band, especially in applications where the A/D system includes a high gain amplifier such as in the case of a floating point A/D system. To obtain narrow band noise measurements, the Evaluation Software recalculates the amplitude of the peak and calculates the amplitude of the noise in the bin located 5 bins from the peak on each side. This is accomplished with the DFT algorithm which is run 5 times in the Narrow Band Noise Subroutine. The averaged results of these runs indicates the narrow band noise in the vicinity of the fundamental. Due to the random nature of the noise, the averaging is necessary to obtain repeatable results. Since the DFT algorithm requires fewer calculations to determine the amplitude of a specific frequency component then the FFT algorithm, the DFT analysis saves a great deal of time in the narrow band noise analysis.

If one additional peak is found

As discussed earlier, if one additional peak is found, the HD and noise tests are bypassed and the Intermodulation Distortion (IMD) test is executed. Figure 10 illustrates Intermodulation Distortion, the nonlinearity characterized by the appearance of frequencies in the output equal to the sums and differences of integral multiples of the two component frequencies F_1 and F_2 as described in the equation below;

$$f_{mn} = mf_1 \pm nf_2 \qquad \text{Equation 4}$$

where

f_{mn} = undesired intermodulation frequencies

f_1 = frequency of first input signal

f_2 = frequency of second input signal

m,n = 1,2,3.....

From the IMD equation, it is evident that there exists a limitless number of intermodulation products. However, in most practical applications, the most prominent IMD products are the two second order products located at $f_2 \pm f_1$ and the two third order products located at $f_1-\Delta$ and $f_2+\Delta$ where $\Delta = |f_2-f_1|$. The IMD Subroutine searches for these four IMD products and defines the IMD level as the largest of the four relative to the largest peak frequency component. As with the HD subroutine, any foldover is accounted for.

Next the Convert Data subroutine is executed regardless of which set of tests (HD and noise or IMD) were performed. Here the linear FFT results stored in the Q[I] array are converted into logarithmic data for plotting purposes. Recall that if more then one additional peak is found, the software skips over all of the distortion and noise tests and executes this subroutine. Following the Data Convert is the Plot subroutine which simply plots the amplitude vs frequency information and prints the FFT parameters along with the results of any noise or distortion tests that were performed.

Application Discussion

Our particular application involved choosing a 12 bit A/D Converter system for a VLF/LF (Very Low Frequency/Low Frequency) Receiver. The device that we eventually chose, based on performance, power consumption, cost, size and availability was the HAS-1201 by Analog Devices. Although the manufacturer did an excellent job characterizing its product, we could not qualify the part solely on data-sheet specifications.

Illustrated in table 1 is Analog Device's specification sheet for the HAS-1201, while table 2 details the A/D performance required by the VLF/LF receiver system. Although Analog Devices provides a great deal of useful information, for all intents and purposes it is only a start in the process of determining the converter's performance for this application, since the manufacturer characterizes its' product under very different test conditions. For example, the manufacturer specifies harmonic distortion to be a minimum of 75 dB down from full scale at any full scale input of frequency from DC to

100 kHz, at a sampling rate of 1.0 MHz. On the other hand, my specific application requires that harmonics be at least -65 dBc (referenced to the carrier) from 14 to 175 kHz at an input level of -6 dBFS, at a sampling rate of 409.6 kHz. Since the specified harmonic performance is tested under conditions that are very different then the actual application, it is difficult to conclusively determine the converter's harmonic performance for this application strictly from the data sheets. Similar problems would be encountered when considering other performance parameters such as noise floor, IMD, and the like.

Before discussing the set up, a couple of notes should be made. In order to preserve the accuracy of the converter under test, care must be taken to minimize ground loop induced errors in both the power supply and signal source connections. These considerations are discussed in detail in the appendix entitled "Minimizing the Elusive Ground Loops." Power supply decoupling is also an important consideration. Many A/D manufacturers recommend that decoupling capacitors be located directly across the power pins of the converter. Usually one set of caps on each power supply voltage consisting of a large (≈10 uF) tantalum and a smaller (≈0.1 uF) ceramic is suggested. The tantalum provides low frequency filtering while the ceramic provides high frequency filtering. Application notes are often included in manufacturers data books containing additional information.

Using the test set up shown below in figure 11, the HAS-1201 performance was evaluated. The respective outputs of the two frequency synthesizers (Bruel & Kjaer 1051) are summed before being inputted to the device under test. It should be noted that the 1051 was selected because of its high spectral purity - harmonic and spurious distortion is specified to be less then -85 dBc. If the price tag of such a spectraly pure generator is too high (the B & K 1051 for example lists for $11,210) one can resort to using a standard frequency synthesizer in conjunction with post harmonic filtering. This is discussed in greater detail in the appendix entitled " The Quest For Spectral Purity".

Careful attention to grounding and bypass capacitor considerations were observed in setting up the converter to maintain its 12 bit accuracy. The digital output of the A/D is fed into the 4096x16 RAM buffer. Since only 12 bits are used, the LSB of the converter is assigned to the LSB of the buffer, while the remaining unused MSBs are connected to the converter MSB. This maintains the sign information of the 2's complement converter output. An alternate approach would be to connect the MSB of the converter to the MSB of the buffer, while the resulting unused LSBs of the buffer are simply grounded. Although this latter approach would require modification of the present FFT scale factor, it would have the advantage of not needing further modification to accommodate various converter widths. Recall that the buffer is necessary since the 409.6 kHz sampling rate exceeds the data input rate of the HP 226 computer. Also contained within the RAM buffer assembly is the timing circuitry that provides the necessary commands to the device under test. Using DIP switches to control the timing, allows the test set to easily accommodate different devices.

Since the sampling rate is 409.6 kHz and the desired FFT bandwidth is 400 Hz, the required number of samples is 1024, as depicted earlier in equation 1. These 1024 data points are read into the computer from the buffer via the GPIO interface. The computer inturn executes the evaluation software and

outputs the results via the HPIB bus to the plotter.

During the Intermodulation Distortion tests, both of the frequency synthesizers were used and during the Harmonic Distortion/Noise tests, one was removed. The HAS-1201 was spot tested at several frequencies over the frequency range of interest, 14-175 kHz. The figures 12 and 13 represent examples of the HD/Noise and IMD test data respectively.

Summarized in table 3 are the worst case values obtained from these series of tests. Note that the converter's performance exceeds the requirements listed in table 1, demonstrating that the HAS-1201 will perform well under the specific conditions of operation - an assuring fact that would have been impossible to obtain solely from data sheet specifications. In fact, further examination of the test data reveals that the harmonic and intermodulation distortion are very close to the noise floor, indicating excellent linearity.

Limitations and Precautions

The following guidlines should be observed to ensure the accuracy and repeatability of any A/D evaluation

- The fundamental frequency should be divisible by an integral number of bins. This would ensure that the 'spreading' discussed earlier would not occur.

- Frequencies close to DC (ie within 4 bins) should not be inputted since they would be ignored by the 'Find Peak" subroutine.

- Frequencies with second or third harmonics within 4 bins of DC (due to foldover) should be avoided since these harmonics would coincide with the DC component and thus their levels could erroneously be considered much higher then they actually are. Similar problems can be encountered if the harmonics coincide with the fundamental after foldover.

- When inputting two frequencies for the IMD test, their levels must be within 6 dB of each other. If not, the software will ignore the smaller peak and run the HD and noise tests - resulting in large errors in the wide band noise calculation since the energy of the smaller peak would be averaged in with the noise. Other errors would be encountered if the smaller peak coincides with the second or third harmonics of the larger signal. In this case the software would erroneously consider the smaller peak a harmonic.

- In a similar case, three or more signals should not be inputted simultaneously unless at least three of the signals are within 6 dB of each other. This way, at least three frequencies within 6 dB are detected and the HD, IMD and noise tests are all bypassed, since the accuracy these tests can be adversely effected by the presence of the additional peaks. If it is necessary to input three or more frequencies that are not within 6 dB of each other, the FFT plot would be valid, but the noise and distortion results will probably contain significant error and thus should be ignored.

- Saturation limits should be carefully observed when inputting more than one frequency at high levels. The peak amplitudes of these combined

waves can exceed the A/D full scale limit although the individual component may not.

□ It is best to use a frequency synthesizer as the signal source and a high accuracy time base (such as a quartz crystal) for the timing circuitry within the RAM buffer. This assures that when the frequency of the signal source is an integral number of 'Bins', the sampling period will contain very close to an integral number of cycles of the input waveform - reducing the magnitude of the discontinuity that must be removed with the Hanning Window.

Conclusions

For all intents and purposes, it is impossible for manufacturers of A/D Converter Systems and components to test their products for each conceivable application. Although most manufacturers do an excellent job specifying their products, it is often up to the user to perform tests that characterize the components under the conditions of interest. Testing can be accomplished by converting the A/D digital output into an analog signal with a D/A for monitoring on a spectrum analyzer. Unfortunately, this approach can be limited in accuracy, often due to the D/A. Another drawback is the fact that determining wide band noise and narrow band noise and measuring harmonic and intermodulation distortion, especially in the presence of foldover, can be difficult on most spectrum analyzers.

Using the Digital Dynamic Evaluation approach described in this article, solves these problems. The data outputted by the A/D remains in the digital domain, and thus is not subject to the inaccuracies of the test set up. In addition, the harmonic and intermodulation distortion tests as well as the wide band and narrow band noise tests are automatically executed providing an efficient and convenient method of evaluating A/D Converter Systems.

APPENDICES

Minimizing the Elusive Ground Loops

Careful attention to grounding considerations is necessary to preserve the performance of high accuracy A/D converter systems. Stray ground loops not only cause errors due to iR voltage drops, but can also generate noise sources due to magnetic or inductive coupling.

Figure 14 represents an A/D system test set up that can be prone to many ground loop induced noise problems. To explore these shortcomings, represented in figure 15 is one possible equivalent circuit of this test set up Although the equivalent circuit is dependant on the exact physical layout, figure 15 is representative of a typical realization.

Ideally, the ground system represents an equipotental point or plane that provides a reference for an electrical circuit or system. Unfortunately, the real world ground plane exhibits a finite impedance, as represented in Figure 15 by Z_{gn}. Also represented in this figure are the shield inductance (L_S), the

shield resistance (R_S), and the mutual inductance between the shield and center conductor (M). The finite impedance of the ground plane creates voltage drops that can corrupt the input signal. For example, the ground current I_{g1} and I_{g2} flow through the ground impedances Z_{g1} and Z_{g2}, respectively. Thus the equivalent input voltage to the A/D, V_{IN}' is actually

$$V_{IN}' = V_{IN} - \underbrace{Z_{G1}I_{G1}}_{\text{undesired voltage drop}} - \underbrace{Z_{G2}I_{G2}}_{\text{undesired noise}}$$

assuming that $Z_{G1} << R_S$. The impedance Z_{G1} would only carry the return current from the signal source, so that any voltage drop across this impedance would have little impact, except perhaps for some minimal attenuation, on the equivalent input to the converter V_{IN}'. However, Z_{G2} returns both the input current and the +V analog supply current, creating a potential noise voltage. This noise contribution can be significant with high accuracy systems. For example, the LSB weight of a 12 bit Converter with 5 V input range is 1.22 mV. A typical impedance of Z_{G2} may be on the order of 0.05 Ω which dictates that a +V power supply ripple current as small as 24 mA can impact the A/D conversion performance.

Another potential problem is created by the fact that the digital circuit power supply (usually +5v) and the -V analog supply both share the ground impedance Z_{G4} in their return path. This can corrupt the -V power supply voltage at the A/D and depending upon the Power Supply Rejection Ratio (PSRR) of the converter, this can degrade overall A/D performance.

It is interesting to note that even in the ideal case, where the ground impedances (Z_{Gn}) approach 0, the ground system represented in Figure 14 is still prone to an often overlooked and less obvious problem - Electromagnetic Interference (EMI) pickup. The shield of the input cable is part of the ground system since it also provides a return path for the input signal. The input current, I_{IN}, is returned through both the shield and the ground plane. If a significant amount of I_{IN} is returned through the ground plane (or if the shield were not used) the circuit will radiate a magnetic field due to the loop area formed with the center conductor and the ground. This loop would also be susceptible to interference from ambient fields. Positioning the input line closer to the ground plane would decrease the loop area and thus reduce the susceptibility to EMI.

Alternately, if a significant amount of current is returned by the shield, then this would effectively reduce EMI susceptibility and radiated emissions, since the loop formed by the shield and center conductor is essentially zero due to the geometry of the coax.

To ensure that all the input return current flows through the shield (and thus minimize EMI susceptibility) it would be necessary to lift the signal

source from ground. Since this is not always practical, it is necessary to determine how the input return current is distributed between the shield and the ground plane. Finding this relationship begins with the loop equation around the return loop. [3]

$$0 = I_{G1}Z_{G1} - R_S I_S - jwL_S I_S + Mjw I_{IN} \qquad \text{Equation 5}$$

since:

$$I_{G1} = I_{IN} - I_S \qquad \text{Equation 6}$$

$$M = L_S \qquad \text{Equation 7}$$

the loop equation can be reduced to

$$\frac{I_S}{I_{IN}} = \frac{Z_{G1}/L_S}{\frac{Z_{G1} + R_S + jw}{L_S}} + \frac{jw}{\frac{Z_{G1} + R_S + jw}{L_S}} \qquad \text{Equation 8}$$

thus at frequencies where

$$w << \frac{R_S + Z_{G1}}{L_S} \qquad \text{Equation 9}$$

equation (8) reduces to

$$\frac{I_S}{I_{IN}} = \frac{Z_{G1}}{Z_{G1} + R_S} \qquad \text{Equation 10}$$

Thus indicating that the return current is shared between the shield and ground plane in proportion to their relative impedance.

However, when

$$w >> \frac{R_S + Z_{G1}}{L_S} \qquad \text{Equation 11}$$

the results are interesting, since equation 8 reduces to

$$\frac{I_S}{I_{IN}} = 1 \qquad \text{Equation 12}$$

In this case all of the current is returned through the shield *regardless* of the impedance of the ground plane, Z_{G1} !! Defining the cutoff frequency of the ground system as

$$w_c = \frac{R_S + Z_{G1}}{L_S} \qquad \text{Equation 13}$$

gives a valuable indication as to how the input current will be shared. At input frequencies well above this value, essentially all of the return current is routed through the shield, reducing the system's susceptibility to EMI.

However, at input frequencies well below the cutoff frequency, much of the return current can flow through the ground plane, depending upon the relative resistance of the ground plane to the shield. When operating at these frequencies, the input cable should be as close as practical to the ground plane to minimize loop area and thus EMI susceptibility.

Represented in Figure 16 is an improved approach to the set up shown in Figure 14. Ideally, the analog grounds are returned to a common point and all the digital grounds are returned to another common point. In turn the two points are joined and then connected to the chassis (or earth) ground. This approach eliminates the potential problems discussed earlier. Since there is only one return path for the signal, the coax provides minimal loop area which reduces EMI susceptibility and since the input signal return path is not shared, it is not prone to conducted interference. Similarly, the power supply connections have independent return paths, so that they will not interfere with each other.

Hanning

When evaluating A/D Converters, it is unlikely that an integral number of cycles of the input waveform are contained within the finite sampling period as depicted earlier in figure 5. Thus, there exists discontinuities at the ends of the sampling period. These discontinuities cause errors in the FFT output spectrum called leakage or side lobes, which appear as a series of spectral lines whose envelope is the (sin x)/x function. Eliminating the end point discontinuities is accomplished by multiplying f(t) with a window function w(t) that is unity at the middle of the sampling period and gradually becomes 0 at the end points. A number of these window functions, w(t), have been proposed. Bertram, 1970, has shown that the amplitude spectrum falls off at least as $1/w^2$ when f(t)w(t) is continuous, and at least as $1/w^3$ when f(t)w(t) and its first derivatives are continuous. This dictates that a w(t) that is zero and has zero derivatives at t = 0 and t = NT is desirable. The inverted cosine bell or "Hanning" window used in the evaluation program satisfies this criteria, and is defined below (see figure 17).

$$\text{Hanning Window} \quad w(t) = \frac{1}{2}\left(1 - \cos\frac{2\pi t}{NT}\right) \quad 0 \le t \le NT \qquad \text{Equation 14}$$

where;

N= number of data points

$T = 1/F_S$ = sampling period

The benefits of the Hanning Window is illustrated in the figures 18 and 19 which represent the frequency spectrum of a 40.001 kHz simulated sine wave with and without the Hanning Window respectively, sampled with 1024 data points at 409.6 kHz. Incidentally, choosing exactly 40.000 kHz would not effectively demonstrate the efficacy of the Hanning window since an integral number of cycles of the simulated sine wave would fit within the sampling period - an extremely unlikely situation in practical applications unless the

frequency synthesizer is phase locked to the sampling frequency. Using 40.001 kHz, an integral number of samples is not contained in the sampling period making the leakage reduction of the Hanning window quite noticeable. Also note the slight reduction in resolution (sharpness) of the fundamental and the reduction in amplitude of the peak with the Hanning Window, both artifacts of the weighing process. The amplitude reduction is easily compensated for in the FFT scaling factor, while the reduction in frequency resolution is negligible in most applications, allowing the benefits of the Hanning Window to greatly outweigh the disadvantages.

DFT Details and FFT Fundamentals [1,4]

Consider the Fourier transform for continuous signals;

$$X(f)=\int_{-\infty}^{+\infty} x(t)e^{-2\pi jft}\,dt \qquad \text{Equation 15}$$

where

f= frequency $(-\infty< f <+\infty)$

t= time $(-\infty< t <+\infty)$

$j=\sqrt{-1}$

X(f)= frequency domain function

x(t)= time domain function

The X(f) term of the Fourier transform equation represents the frequency domain function of the continuous time domain function x(t). The sampled version of the Fourier Transform, known as the Discrete Fourier Transform (DFT), is shown in the equation below;

$$X(k)=\sum_{n=0}^{n=N-1} D_n e^{-2\pi jnk/N} \qquad \text{Equation 16}$$

where;

D_n= n^{th} data sample

N= number of samples

X(k)= k^{th} frequency component

X(k) of the above equation is a complex quantity representing both the amplitude and phase of the k^{th} frequency component. The amplitude of the k^{th} frequency component is derived from this equation by summing the squares of both the real and imaginary parts of X(k), represented in equation 17 as A_k and B_k respectively.

$$A(F_k)^2 = A_k^2 + B_k^2 \qquad \text{Equation 17}$$

Real Part

$$A_k = D_n \sum_{n=0}^{n=N-1} \cos\left(\frac{2\pi kn}{N}\right)$$

Imaginary Part

$$B_k = D_n \sum_{n=0}^{n=N-1} \sin\left(\frac{2\pi kn}{N}\right)$$

Equations 18

Equations 17 and 18 represent a means whereby the energy contained in the k^{th} frequency bin can be calculated with the time domain data D_n. The Narrow band Noise Subroutine implements equations 17 and 18 by first generating a set of sine and cosine look up tables and loading them into the B[I] and R[I] arrays respectively.

$$B(I) = \sin[2\pi(I-1)/N]$$

Equations 19

$$R(I) = \cos[2\pi(I-1)/N]$$

where I= 1 to N

Once these trigonometric calculations are completed, N data points (recall that the default value of N is 1024) are loaded into the U(I) array and Hanned with the inverted cosine bell curve. Then through the DFT equations 17 and 18, the amplitude at the peak and the amplitude of the noise at 5 bins on each side of the peak is calculated. Multiplying the peak by a factor of 2 and dividing the product by the total noise, yields the SNR ratio (i.e., 2T/Z = F where T = peak amplitude, Z = noise and F = SNR).

Note that the SNR calculation is performed 5 times and then averaged. Due to the random nature of the noise, the 5 time average is necessary to improve the repeatability and accuracy of the SNR measurements. It is interesting to note that the execution of equation 18 requires N complex multiplications and N complex additions, to calculate the energy contained in one bin. Calculating the energy in all N bins across the DC to $F_S/2$ spectrum would require N^2 complex multiplications and N^2 complex additions. (Since the computation time required to perform a complex multiplication is significantly greater then the time required for a complex addition, we need only consider the number of multiplications). This number of required multiplications can become quite large - the default value of N=1024 for example dictates that over 1 million multiplications would be necessary to compute the 0 to $F_S/2$ frequency spectrum using the DFT equation directly!

Reducing the required number of multiplications is accomplished with the Fast Fourier Transform (FFT) Algorithm. The FFT is simply an algorithm that can efficiently compute a series of DFT equations with much fewer multiplications then would be required if the DFT were directly implemented N times. In fact, the required number of multiplications of the FFT for N data points is

$$\text{No of Multiplications} = \frac{N(\log_2 N)}{2} \qquad \text{Equation 20}$$

Thus for the defalt value of N=1024, the FFT would require only 5120 multiplications to perform the frequency spectrum calculations verses the over 1 million required by calculating the DFT directly. Figure 20 illustrates the comparison in number of multiplications required by the DFT and FFT algorithms.

Although the FFT is most efficient for calculating the entire spectrum (ie the energy in each of the N bins that subdivide the 0 to $F_S/2$ spectrum), the DFT is more practical to implement when it is necessary to calculate the energy in only a few bins such as in the case of the Narrow Band Noise Subroutine. Here the energy in only 3 bins is calculated, requiring 3x1024=3072 multiplications - 40% fewer then if the 5120 multiplications needed by the FFT.

The Quest for Spectral Purity

Frequency stability (i.e., low phase noise) and amplitude stability are important requirements of the frequency source used in the A/D evaluation set up - however, so is the requirement of low harmonic distortion. Since many A/D conversion systems boast harmonic performance better than -75 dBFS, (relative to full scale) the signal source must exhibit harmonics lower than this level - a tough requirement even for many of the best frequency synthesizers.

The HP 3325A for example specifies harmonic levels to be less than -60 dBc (referenced to the carrier) over the frequency range of 50 kHz to 200 kHz. Although this specification is quite good for a frequency synthesizer, the harmonics of this signal source would be the limiting factor concerning harmonic evaluation for many Converter systems. One possible solution is to filter the harmonics with an active LPF such as the Krohn-Hite 3202 - but be careful !! Many active filters themselves exhibit HD levels that are comparable to the HD components that they were intended to filter. Careful evaluation on a high quality (i.e., low HD) Spectrum Analyzer should be performed on the signal source and filter to determine the practical lower limits of the HD levels.

Figures 21-26 reveal these potential pitfalls in filtering harmonics. The set up illustrated in Figure 21 is used to obtain a low HD sine wave. Using the HP 4192A as a Frequency Synthesizer, its output is routed through either the Krohn-Hite 3202 Active Filter or the 3 pole passive "PI" filter, to filter harmonics. Although the Krohn-Hite 3202 is a versatile high quality device, it can create HD problems at high signal levels.

Figure 22 reveals the output spectrum of the HP 4192A, which is set to 30 kHz, 1 VRMS (0 dBV), a level that would be consistent with many A/D

Converter evaluation scenarios. Note that the 2nd and 3rd harmonics are at -56 dBV and -54 dBV respectively. Although these distortion levels are commendable for a Frequency Synthesizer, they do present a problem for A/D evaluation. In an attempt to remove these undesired harmonics, the Active Filter is set to a cutoff frequency (-3 dB point) of 30 kHz, thus the theoretical attenuation for this 24 dB/octave filter at 60 kHz and 90 kHz is -24 dB and -38 dB respectively. This would dictate that the components out of the Active Filter should be 30 kHz at -3 dBV, 60 kHz at -80 dBV and 90 kHz at -92 dBV, rendering the 2nd and 3rd harmonics invisible since the dynamic range of the Spectrum Analyzer is set to 0 dBV to -80 dBV.

However, upon examination of figure 23, the 3rd harmonic is "invisible" as expected, but the 2nd harmonic is at -71 dBV well above the expected level of-80 dBV, due to the harmonic distortion introduced by the Active Filter. One way to remedy this problem is to substitute the Active Filter with a passive type filter. The fundamental advantage to this approach is the fact that the active components and their associated harmonic distortion are not present, assuming that the magnetics of the filter operate well below their saturation limits. The results of such a filter is shown in Figure 24, note the absence of both the 2nd and 3rd harmonics. However, one disadvantage to the passive filter approach is the difficulty in adjusting the cutoff frequency.

One way to solve the Active Filter HD problem while maintaining its adjustability is to lower the level presented to the Active Filter and recovering the desired signal level with a post-filter amplifier. Since the 1 VRMS level presented to the filter does cause HD, although it is well below the manufacturer's 3 VRMS maximum input specification, its harmonic performance as well as that of the synthesizer improve significantly at lower signal levels. This is illustrated in the figures 25 and 26. Figure 25 represents the output spectrum of the signal source, note that its harmonics are slightly lower, due to the reduced output level of -20 dBV. As Figure 26 reveals, the HD components out of the filter are "invisible" as expected. Following the Active Filter with a low HD amplifier can regain the desired signal level (0 dBV) while maintaining the low HD.

Recently, generators have been introduced that exhibit ultra low HD and thus require no harmonic filtering - greatly simplifying the test set up. The Bruel and Kjaer 1051A for example guarantees the maximum harmonic and spurious distortion to be less then -96 dBc from 20 Hz to 20 kHz or less than -85 dBc from 0.2 Hz to 200 kHz. The major disadvantage to the 1051A is its high cost - the unit lists for $11,210.00. However, when considering the cost and inconvenience of a separate frequency synthesizer and filter system, the price may be justifiable.

References

1. DDC News, March 1987

2. Burr Brown Application Note AN-113A, "Data Converter Test Methods for Digital Audio Applications", May 1987, p2

3. Ott, Henry, "Ground- A Path For Current Flow", EMC Technology, Jan/March 1983, pp44-46,48

4. Brigham, E.Oram, "The Fast Fourier Transform", Prentice-Hall, pp148-153

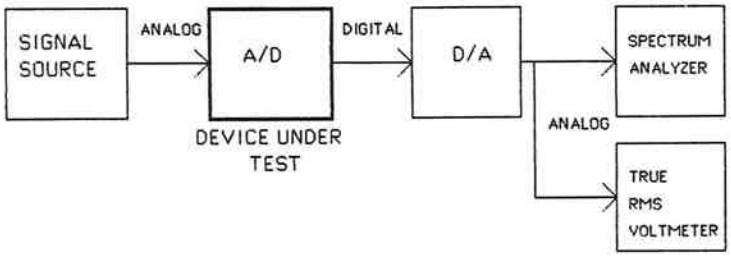


Figure 1. A/D Converter Evaluation using the Reconversion Approach

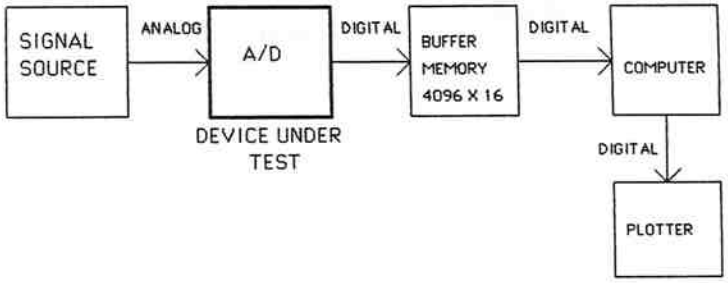


Figure 2. A/D Converter Evaluation using the Digital Dynamic approach

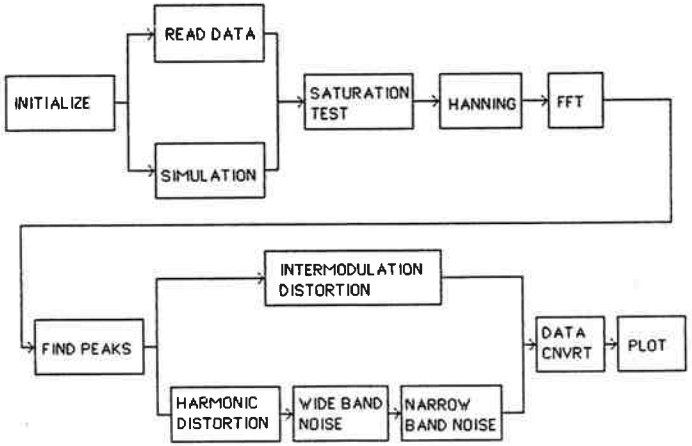


Figure 3. Evaluation Software Block Diagram

Figure 4. Evaluation Software Program Listing

```
0: % "A/D PERFORMANCE IS EVALUATED THROUGH THE USE OF FFT/DFT ANALYSIS"
1: % "WRITTEN BY: James Colotti and Paul Vaccaro"
2: % "EATON/CSD, Farmingdale NY  11735"
3: % "Date of last revision: 87-9-15"
4: "INITIALIZATION":
5: dim Q[2048],B[2048],R[2048],C[7],X[3],Y[3],U[2048],A$[10]
6: 1024}N;% "N=# of samples"
7: 409600}E;% "E=Sampling Rate"
8: rad;flt 11
9: ent "No Samples=1024,Samp Fr=409600 Hz (0=ok,1=change)",A
10: if A=0;gto "START"
11: ent "Enter number of samples as exponent of 2",N
12: 2^N}N
13: ent "Enter sampling rate in Hz",E
14: "START":
15: 0}A
16: ent "Run a simulation or read A/D data? (0=sim,1=A/D)",A
17: if A=1;gto "READ DATA"
18: "SIMULATION":
19: "SIMULATION"}A$
20: 0}r1;0}r2;0}X[1];0}X[2];0}A
21: ent "Enter freq of first component in Hz",r1
22: ent "Enter amp of first component in dB below full scale",X[1]
23: ent "Enter freq of second component in Hz",r2
24: ent "Enter amp of second component in dB below full scale",X[2]
25: dsp "Loading simulation data"
26: 10^(-abs(X[1])/20)*2048}X[1]
27: 10^(-abs(X[2])/20)*2048}X[2]
28: 2*(*r1}r1
29: 2*(*r2}r2
30: for I=1 to N
31: X[1]*sin(I*r1/E)+X[2]*sin(I*r2/E)}Q[I]
32: if Q[I]>2048;2048}Q[I]
33: if Q[I]<-2048;-2048}Q[I]
34: 0}B[I]
35: next I
36: gto "SATURATION TEST"
37: "READ DATA":
38: ent "Enter Converter Part Number",A$
39: wtc 12,35;wtc 12,16;wtc 12,18
40: "CHECK2":rds(12)}A;bit(0,A)}A
41: if A#1;gto "CHECK2"
42: dsp "Reading data"
43: 0}L
44: for I=1 to N
45: rdb(12)}Q[I]
46: 0}B[I]
47: next I
48: "SATURATION TEST":
49: 0}r9
50: for I=1 to N
51: if Q[I]>=2047;1}r9
52: if Q[I]<=-2048;1}r9
53: next I
54: if r9=0;gto "HANNING"
55: beep
56: "SAT":ent "Saturation detected/imminent (0=cont,1=restart)",A
57: if A=0;gto "HANNING"
58: if A=1;gto "START"
59: gto "SAT"
60: "HANNING":
61: dsp "Hanning"
62: for I=1 to N
63: Q[I]*((1-cos(2*(*I/N))/2)}Q[I]
64: next I
65: "FFT":
66: dsp "Computing FFT"
67: E/N}O
68: 0}r6;N-1}r7;0}C[6]
69: for M=1 to r7
70: N}L
71: "GREATER":L/2}L
72: if r6+L>r7;gto "GREATER"
73: r6modL+L}r6
74: if r6<=M;gto "NEXT"
75: Q[M+1]}r8
76: Q[r6+1]}Q[M+1]
77: r8}Q[r6+1]
78: B[M+1]}r10
79: B[r6+1]}B[M+1]
80: r10}B[r6+1]
81: "NEXT":next M
82: 1}L
83: "DIT":if L>=N;gto "CONTINUE"
84: 2*L}S;L}r25
85: rad
86: for M=1 to L
87: (*(1-M)/r25}r26
88: cos(r26)}R
89: sin(r26)}W
90: for I=M to N by S
91: I+L}J
92: R*Q[J]-W*B[J]}r8
93: R*B[J]+W*Q[J]}r10
94: Q[I]-r8}Q[J]
95: B[I]-r10}B[J]
96: Q[I]+r8}Q[I]
97: B[I]+r10}B[I]
98: next I
99: next M
100: S}L;gto "DIT"
101: "CONTINUE":
102: 0}U;0}T;0}S;0}P
103: for I=1 to N/2+1
104: Q[I]}r12;B[I]}r13
105: r12*r12+r13*r13}Q[I]
106: next I
107: "CNT":for I=1 to N/2+1
108: Q[I]/(N*511.75)^2}Q[I];% "Scale data points"
109: Q[I]+C[6]}C[6];% "Get Total Power"
110: next I
111: "FIND PEAKS":
112: 0}C[1];0}C[7];0}r1;0}r7;0}Q
113: for I=4 to N/2+1
114: if Q[I]>=C[1];Q[I]}C[1];I}r1
115: next I
116: for I=r1+3 to N/2+1
117: if Q[I]>=C[1]/2;Q[I]}C[7];I}r7;Q+1}Q
```

```
118: next I
119: for I=4 to r1-3
120: if Q[I]>=C[1]/2;Q[I]}C[7]:I}r7:Q+I}Q
121: next I
122: 10*log(C[7]+1e-70)}C[7]
123: if A$="SIMULATION";gto "DATA CONVERT"
124: if Q=0;gto "HARMONIC DISTORTION"
125: if Q=1;gto "INTERMODULATION DISTORTION"
126: 0}A
127: "FP1":ent "Too many peaks(0=restart,1=continue)",A
128: if A=0;gto "START"
129: if A=1;gto "DATA CONVERT"
130: gto "FP1"
131: "HARMONIC DISTORTION":
132: if 2*r1>N/2+1;gto "HARMB"
133: "HARMA":10*log(Q[2*r1-1]/C[1])}C[2];2*r1-1}r2
134: if 3*r1>N/2+1;gto "HARMC"
135: 10*log(Q[3*r1-2]/C[1])}C[3];3*r1-2}r3
136: gto "HARME"
137: "HARMB":10*log(Q[N+3-2*r1]/C[1])}C[2];N+3-2*r1}r2
138: if 3*r1>N/2+1;gto "HARMD"
139: "HARMC":10*log(Q[N+4-3*r1]/C[1])}C[3];N+4-3*r1}r3
140: gto "HARME"
141: "HARMD":10*log(Q[3*r1-2-N]/C[1])}C[3];3*r1-2-N}r3
142: "HARME":
143: if C[2]<-120;-120}C[2]
144: if C[3]<-120;-120}C[3]
145: "AVE WIDE BAND NOISE":
146: C[6]-Q[1]-Q[2]-Q[3]-Q[4]}C[6];% "Subtract DC"
147: for I=-5 to 5;% "Subtract signal & harmonic BW"
148: C[6]-Q[r1+I]-Q[r2+I]-Q[r3+I]}C[6]
149: next I
150: C[6]/(N/2-36)}C[6]
151: if C[6]<=0;1e-12}C[6]
152: 10*log(C[6])}C[6];% "Average Noise"
153: "NARROW BAND SNR":
154: dsp "Computing sine & cosine tables"
155: 2*()P
156: for I=1 to N
157: sin(P*(I-1)/N)}B[I]
158: cos(P*(I-1)/N)}R[I]
159: next I
160: "Compute DFT":
161: 0}F:0}T:0}Z
162: for V=1 to 5
163: wtc 12,35:wtc 12,16:wtc 12,18
164: "CHECK1":rds(12)}A:bit(0,A)}A
165: if A#1;gto "CHECK1"
166: for I=1 to N
167: rdb(12)}U[I]
168: next I
169: for I=1 to N
170: U[I]*((1-cos(2*(*I/N))/2)^U[I]
171: next I
172: dsp "Data Set ",V
173: for J=1 to 3
174: 0}X[J]:0}Y[J]
175: next J
176: for J=1 to 3
177: 0}A
178: r1-11+5*J}L
179: for I=1 to N
180: A+L}A
181: if A>N;A-N}A
182: X[J]+U[I]*R[A]}X[J]
183: Y[J]+U[I]*B[A]}Y[J]
184: next I
185: next J
186: X[1]^2+Y[1]^2+X[3]^2+Y[3]^2}Z
187: X[2]^2+Y[2]^2}T
188: 2*T/Z+F}F
189: "GOON":next V
190: 10*log(F/V)}U
191: gto "DATA CONVERT"
192: "INTERMODULATION DISTORTION":
193: abs(r7-r1)}r8;% "Delta Freq"
194: % "Find 3rd order IM products"
195: if r7<r1;gto "IMA"
196: r7+r8}r4
197: if r4>N/2+1;N+2-r4}r4
198: abs(r1-r8)}r5
199: gto "IMB"
200: "IMA":
201: abs(r7-r8)}r4
202: r1+r8}r5
203: if r5>N/2+1;N+2-r5}r5
204: "IMB":
205: if Q[r5]>Q[r4];Q[r5]}C[5]
206: if Q[r4]>=Q[r5];Q[r4]}C[5]
207: % "Find 2nd order IM products"
208: abs(r7-r1+1)}r4
209: r7+r1-1}r5
210: if r5>N/2+1;N+2-r5}r5
211: if Q[r5]>Q[r4];Q[r5]}C[4]
212: if Q[r4]>=Q[r5];Q[r4]}C[4]
213: % "Find max IM"
214: if C[5]>C[4];C[5]}C[4]
215: 10*log(C[4])}C[4]
216: "DATA CONVERT":
217: for I=1 to N/2+1
218: 10*log(Q[I]+1e-25)}Q[I]
219: if Q[I]<-120;-120}Q[I]
220: next I
221: 10*log(C[1])}C[1]
222: "PLOT":
223: dsp "Plotting in process"
224: pen# 1
225: fxd 1
226: psc 705
227: scl -E/8000,E/1600,-176,30
228: line
229: csiz 1.5
230: xax -120,E/10000,0,E/2000,1
231: yax 0,10,-120,0.1
232: for I=-120 to 0 by 10
233: plt 0,I,1:plt E/2000,I,2
234: next I
235: for I=0 to E/2000 by E/10000
236: if E/10000<1;plt I/100,0,1:plt I/100,-120,2
237: if E/10000>=1;plt I,0,1:plt I,-120,2
238: next I
239: plt 0,-120,1
240: for I=1 to N/2+1
241: Q*(I-1)/1000}X
242: 2}T
243: if I=1;1}T
244: pen# 2
245: plt X,Q[I],T
246: next I
247: csiz 1.8
248: pen# 3
249: plt -E/7000,-55,1
250: lbl "AMPLITUDE"
251: plt -E/7700,-62,1
252: lbl "(dBFS)"
253: if r9=1;plt E/1900,-55,1:lbl "SATURATION"
254: if r9=1;plt E/1900,-62,1;lbl "DETECTED/"
255: if r9=1;plt E/1900,-69,1:lbl "IMMINENT"
256: plt E/5000,-146,1;lbl "FREQUENCY (kHz)"
257: plt E/8500,15,1
258: if A$="SIMULATION":lbl A$:gto "CSIZ"
259: if Q=0;lbl "HARMONIC/NOISE TEST"
260: if Q=1;lbl "INTERMODULATION TEST"
261: "CSIZ":csiz 1.5
262: plt -E/8000,-156,1
263: lbl " Number of Points=" N
264: plt -E/8000,-161,1
265: lbl " Bin Size=",Q," Hz"
266: plt E/8000,-156,1
267: lbl "Freq of Peak= ",(r1-1)*Q/1000," kHz"
268: plt E/8000,-161,1
269: lbl "Amp of peak= ",C[1]," dBFS"
270: if Q=0;gto "HD PLOT"
271: plt E/2800,-156,1
272: lbl "Freq of smaller peak=",(r7-1)*Q/1000," kHz"
273: plt E/2800,-161,1
274: lbl "Amp of smaller peak=",C[7]," dBFS"
275: if A$="SIMULATION";gto "FQUEST"
276: plt E/8000,-166,1
277: if abs(r8)>3;if Q=1;lbl "Intermod Level=",C[4]-C[1]," dBc"
278: plt E/2800,-166,1
279: lbl "Part No: ",A$
280: gto "FQUEST"
281: "HD PLOT":
282: if A$="SIMULATION";gto "FQUEST"
283: plt E/2800,-156,1
284: lbl "2 nd Harmonic= ",C[2]," dBc"
285: plt E/2800,-161,1
286: lbl "3 rd Harmonic= ",C[3]," dBc"
287: plt -E/8000,-166,1
288: lbl " Wide Band Noise= " C[6]," dBFS"
289: plt E/8000,-166,1
290: lbl "Narrow Band SNR= ",N," dB"
291: plt E/2800,-166,1
292: lbl "Part No: ",A$
293: "FQUEST":pen# 0
294: 0}A
295: ent "Run another test(N=0,Y=1)",A
296: if A=1;gto "START"
297: dsp "Au Revoir"
298: "END":end
16713
```

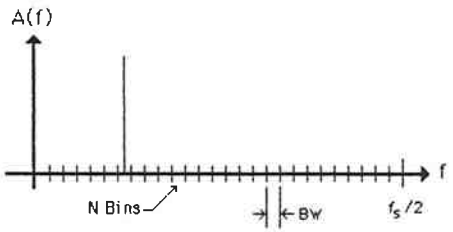


Figure 6. FFT Output consisting of N data points representing the frequency domain of the input.

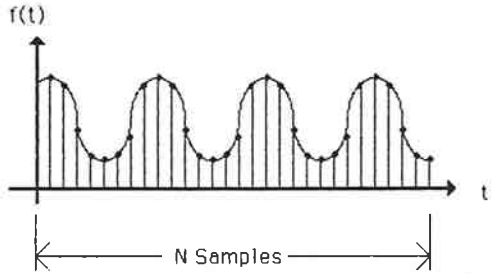


Figure 5. Discontinuity of f(t) in the sampling period

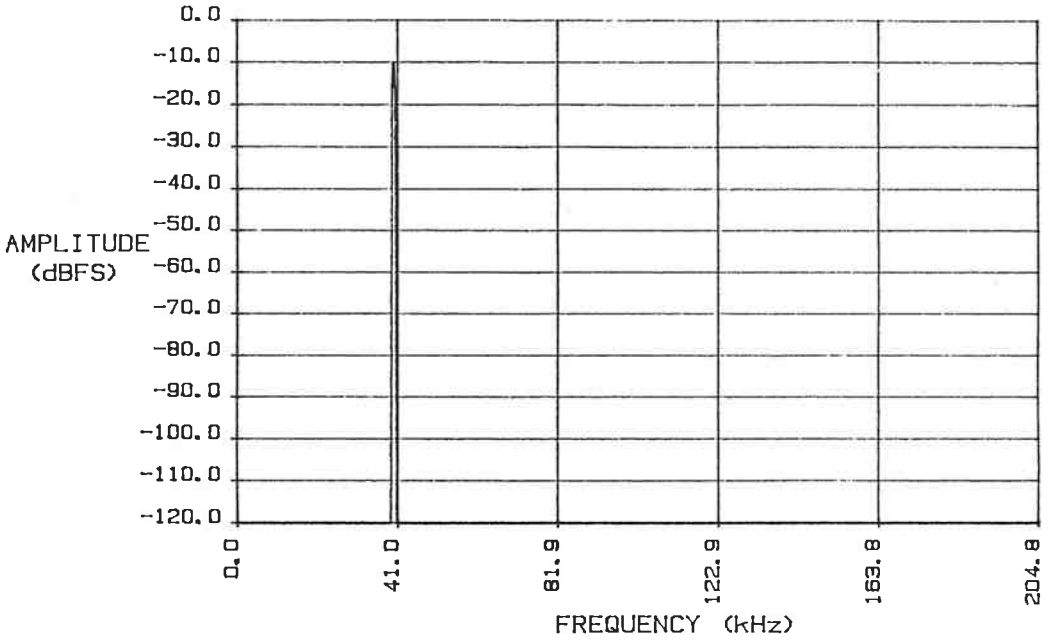


Figure 7. FFT Spectrum of 40.0 kHz Simulated Sine Wave

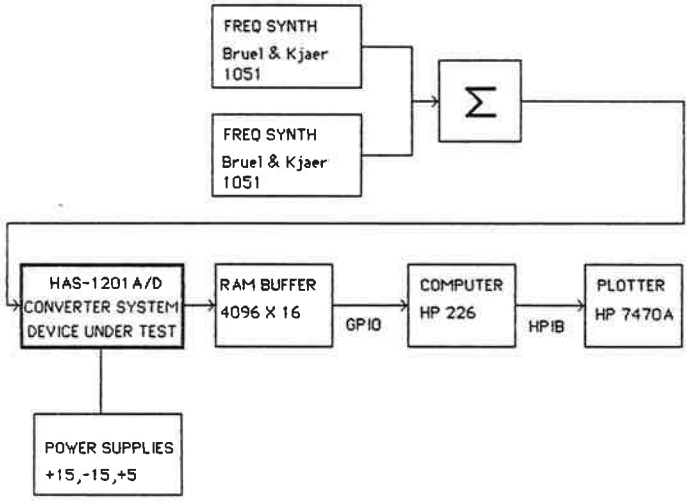


Figure 11. HAS-1201 Evaluation Set Up

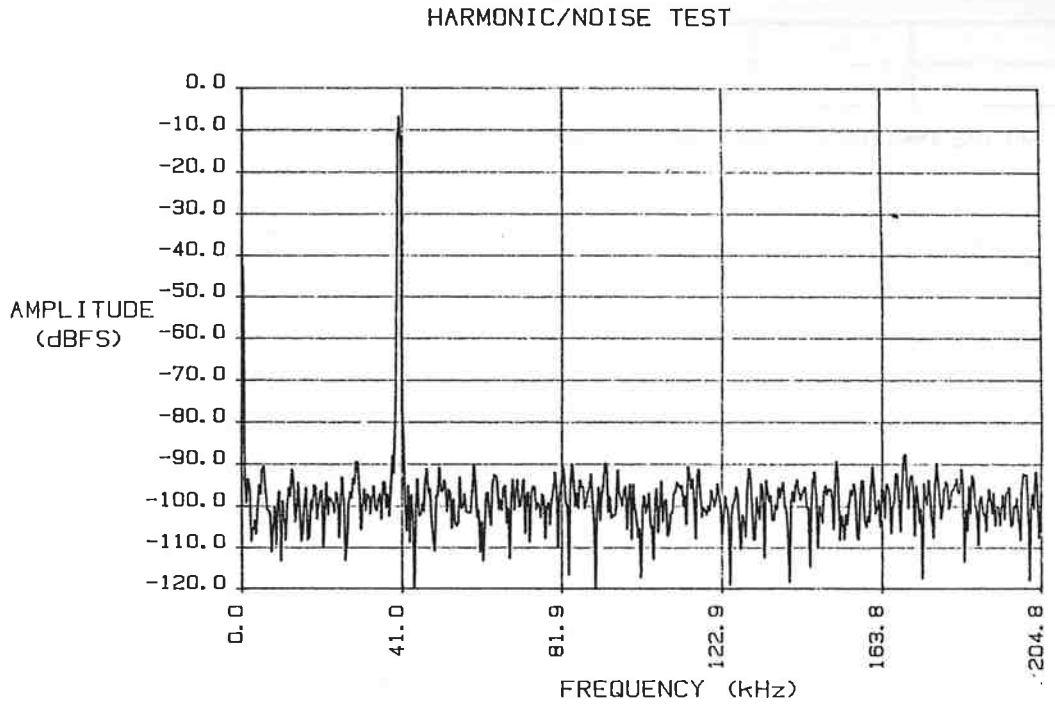


Figure 12. HAS-1201 HD/Noise Test Result Example

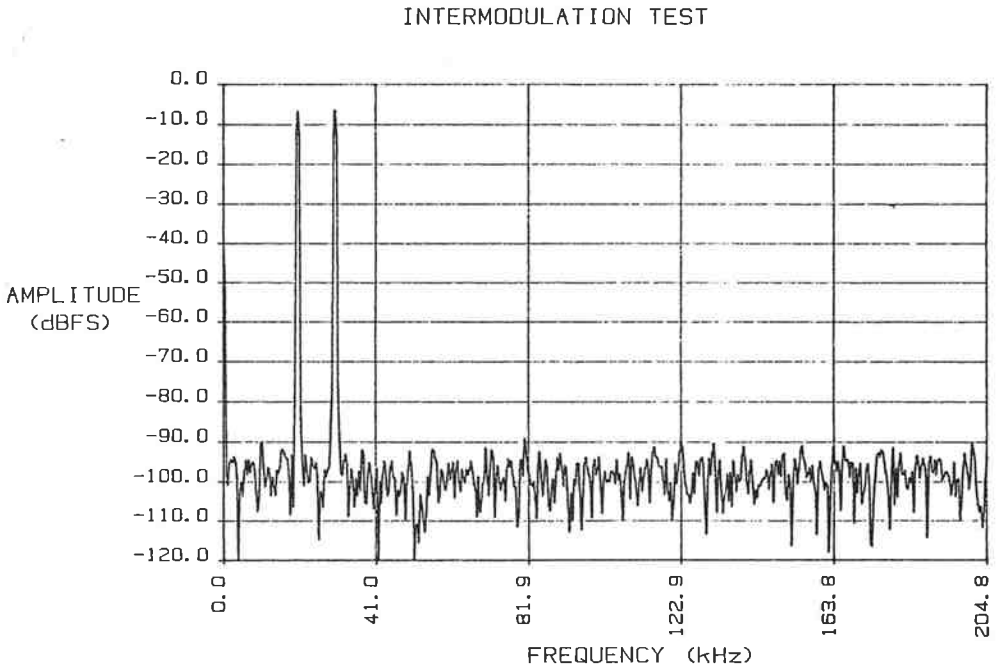


Figure 13. HAS-1201 IMD Test Result Example

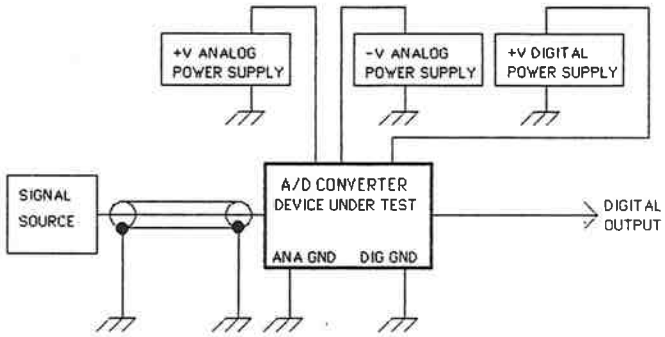


Figure 14. A/D Test Set Up With Potential Grounding Problems

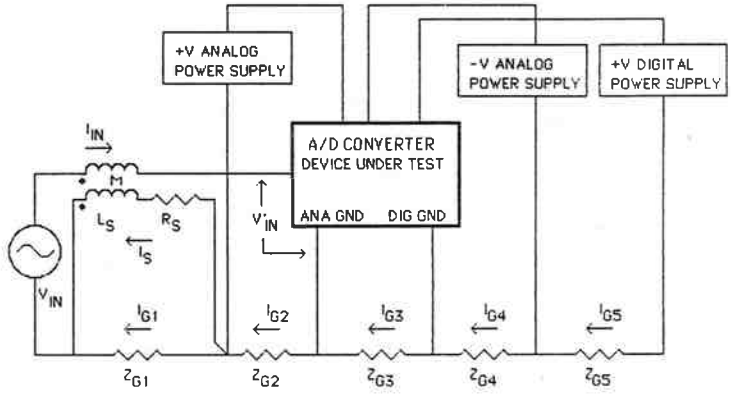


Figure 15. Equivalent Ground Circuit of A/D Test Set Up

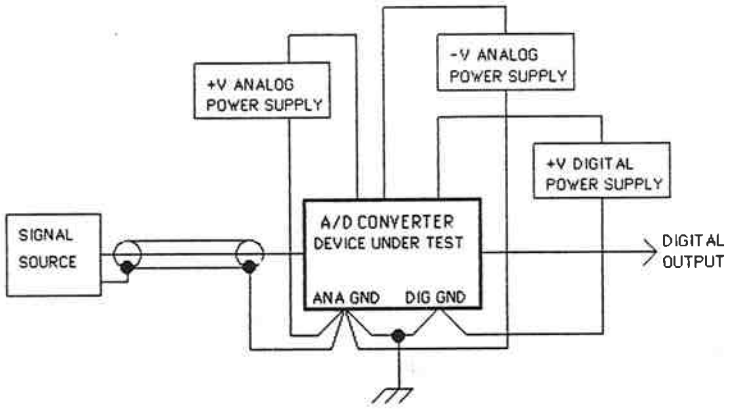


Figure 16. A/D Test Set Up With Improved Ground System

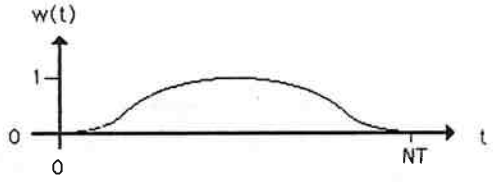


Figure 17. Hanning Window Weighting Function

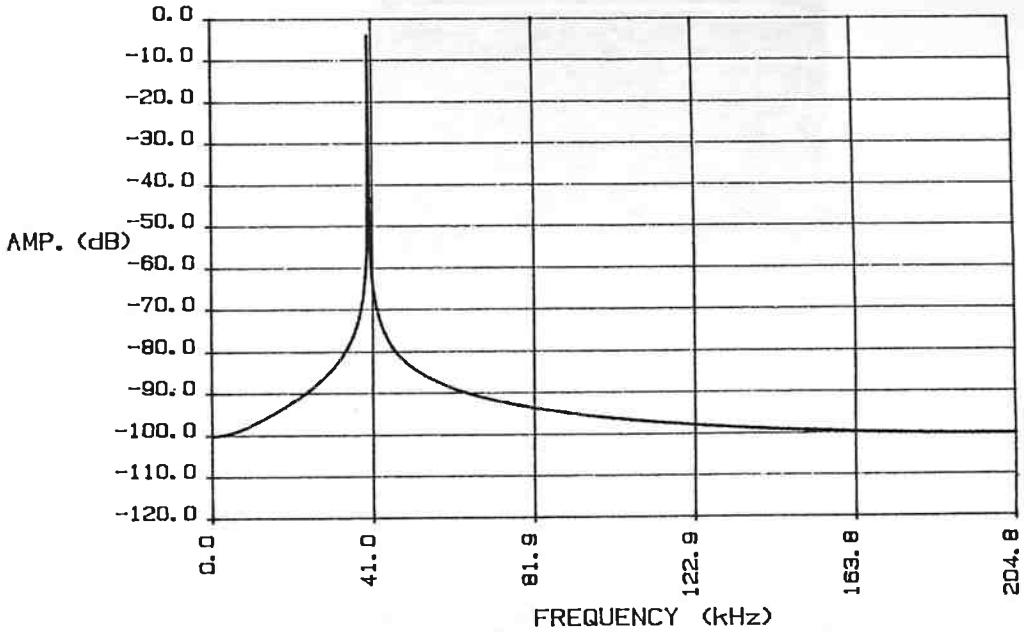


Figure 18. 40.001 kHz Simulated Sine Wave Spectrum Without Hanning

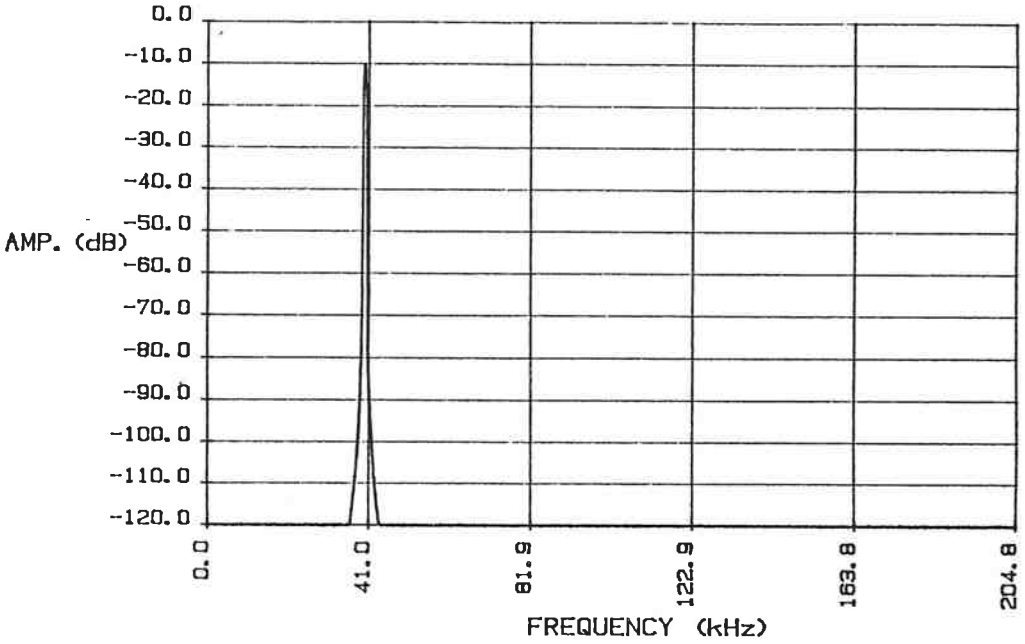


Figure 19. 40.001 kHz Simulated Sine Wave Spectrum With Hanning

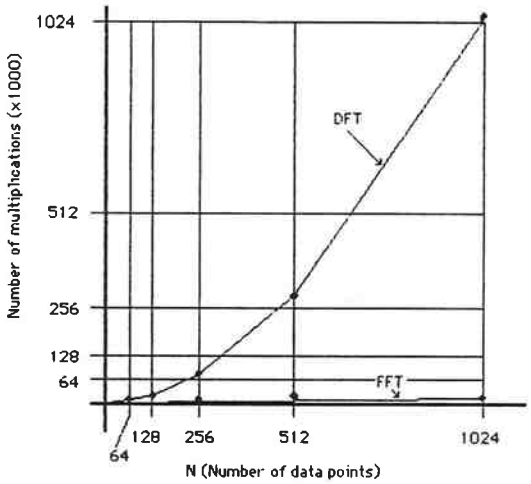


Figure 20. Comparison of Required Number of Multiplications to Perform the DFT and FFT Algorithms

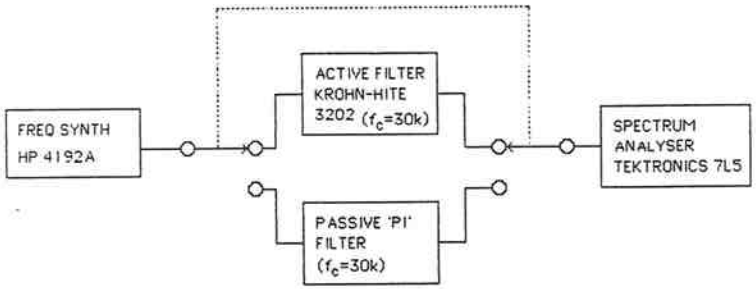


Figure 21. Harmonic Distortion Test Set Up

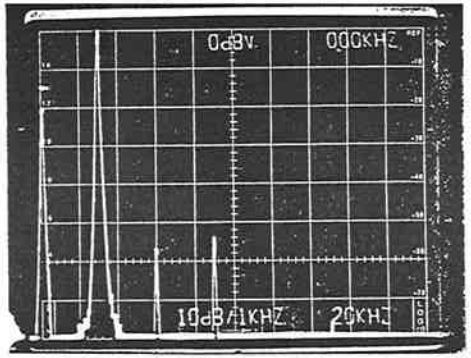


Figure 22. Frequency Spectrum Out Of HP4192A

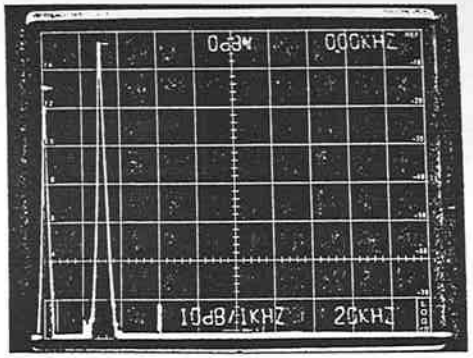


Figure 23. Frequency Spectrum Out Of Active Filter

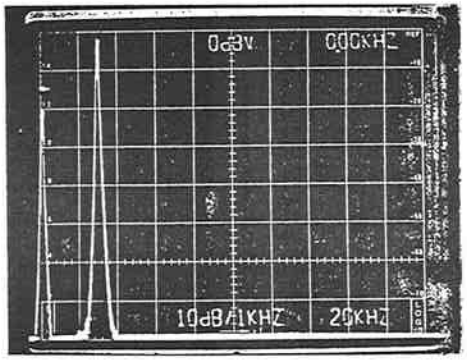


Figure 24. Frequency Spectrum Out Of Passive Filter

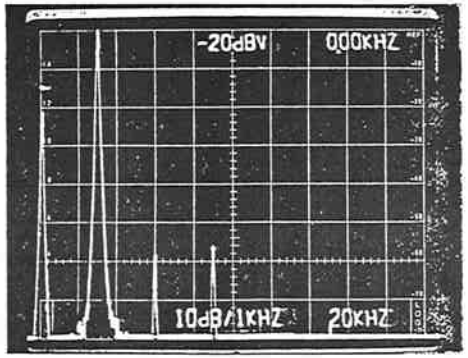


Figure 25. Frequency Spectrum Out Of HP41924 at Lower Level

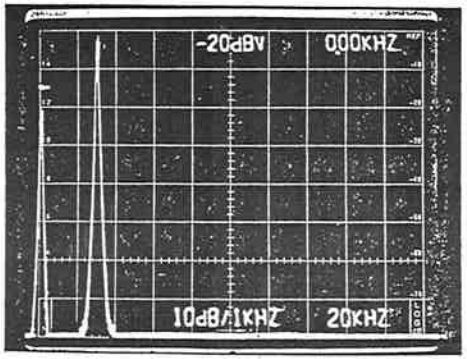


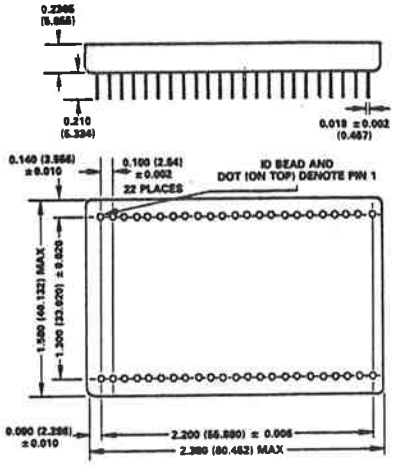
Figure 26. Frequency Spectrum Out Of Active Filter at Lower Level

SPECIFICATIONS (typical @ +25°C with nominal power supplies unless otherwise noted)

Parameter	Units	HAS-1201KM	HAS-1201SM/SMB
RESOLUTION (FS = Full Scale)	Bits	12	*
	% FS	0.025	*
ACCURACY			
Gain	% FS	±3	*
Gain vs. Temperature	ppm/°C	80	*
Linearity @ dc	% FS ± 1/2LSB	0.0125	*
Diff. Nonlinearity vs. Temp.	ppm/°C	10	15
Monotonicity		Guaranteed	*
DYNAMIC CHARACTERISTICS			
In-Band Harmonics[1]			
(dc to 100kHz)	dB below FS (min)	80 (75)	*
(100kHz to 500kHz)	dB below FS	75	*
Conversion Rate	MHz, max	1.05	1.00
Conversion Time[2]	ns, max	950	*
Over Temperature	ns, max	950	1000
Aperture Uncertainty (Jitter)	ps, rms	30	*
Aperture Time (Delay)	ns	25	*
Signal to Noise Ratio (SNR)[3]	dB (min)	68 (65)	*
Transient Response[4]	ns (max)	600 (1000)	*
Overvoltage Recovery[5]	ns	1000	*
Input Bandwidth			
Small Signal, −3dB[6]	MHz	2	*
Large Signal, −3dB[7]	MHz	2	*
Two-Tone Linearity (@ input frequencies)			
(75kHz; 105kHz)	dB below FS	80	*
ANALOG INPUT			
Voltage Ranges	V, p-p FS	5.0/10.0	*
	V, max	±15	*
Impedance (5V/10V Input)	Ω (max)	1000/2000 (±1%)	*
Bipolar Offset[8]			
Initial (5V Input)	mV (max)	±2 (±10)	*
vs. Temperature	FS ppm/°C (max)	50 (200)	*
DIGITAL INPUTS			
Logic Levels, TTL-Compatible	V	"0" = 0 to +0.4	*
	V	"1" = +2.4 to +5	*
Impedance	LS TTL Loads	3	*
Rise and Fall Times	ns, max	10	*
Frequency	MHz, max	1.05	1.00
Encode Command Width[9]			
Min	ns	50	*
Max	ns	Encode Period − 350ns	*
Register Strobe Width			
Min	ns	50	*
Max	ns	Encode Period − 350ns	*
$\overline{\text{Enable}}$ Width			
Min	ns	100	*
DIGITAL OUTPUTS			
Format	Bit 1, $\overline{\text{Bit 1}}$ − $\overline{\text{Bit 12}}$	3-State; NRZ	*
Logic Levels, TTL-Compatible[10]	V	"0" = 0 to +0.5	*
		"1" = +2.4 to +5	*
Drive	TTL Loads	1	*
Time Skew	ns, max	10	*
Delay: Register Strobe to Output Data Validity	ns	30	*
Coding		Complementary Binary (CBIN)	*
		Complementary Offset Binary (COB)	*
		Complementary 2's Complement (C2SC)	*
POWER REQUIREMENTS			
+15V ±5%	mA (max)	55 (70)	*
−15V ±5%	mA (max)	65 (80)	*
+5V ±5%	mA (max)	195 (235)	*
−5.2V ±5%	mA (max)	35 (40)	*
Power Consumption	W (max)	3.0 (3.6)	*
TEMPERATURE RANGE[11]			
Operating	°C	0 to +70	−25 to +85
Storage	°C	−55 to +150	*
THERMAL RESISTANCE[12]			
Junction to Air, θja (Free Air)	°C/W	12	*
Junction to Case, θjc	°C/W	2.5	*

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



HAS-1201 PIN DESIGNATION

PIN	FUNCTION	PIN	FUNCTION
46	+5V	1	+5V
45	−15V	2	GROUND
44	UNIPOLAR POSITIVE	3	ENCODE COMMAND
43	UNIPOLAR NEGATIVE	4	GROUND
42	−5.2V	5	GROUND
41	GROUND	6	DO NOT CONNECT*
40	5V RANGE IN	7	GROUND
39	10V RANGE IN	8	REGISTER STROBE
38	OFFSET	9	+5V
37	DO NOT CONNECT*	10	$\overline{\text{ENABLE}}$
36	GROUND	11	BIT 1 (MSB)
35	−15V	12	$\overline{\text{BIT 1}}$ (MSB)
34	NO CONNECTION	13	$\overline{\text{BIT 2}}$
33	NO CONNECTION	14	$\overline{\text{BIT 3}}$
32	+15V	15	$\overline{\text{BIT 4}}$
31	+15V	16	$\overline{\text{BIT 5}}$
30	GROUND	17	$\overline{\text{BIT 6}}$
29	GROUND	18	$\overline{\text{BIT 7}}$
28	GROUND	19	$\overline{\text{BIT 8}}$
27	GROUND	20	$\overline{\text{BIT 9}}$
26	GROUND	21	$\overline{\text{BIT 10}}$
25	GROUND	22	$\overline{\text{BIT 11}}$
24	GROUND	23	$\overline{\text{BIT 12}}$ (LSB)

NOTE:
PINS 2, 4, 5, 7, 24-30, 36 and 41 NEED TO BE CONNECTED TO THE SAME COMMON GROUND AS CLOSE TO CASE AS POSSIBLE. POWER SUPPLY VOLTAGES NEED TO BE CONNECTED TO ALL DESIGNATED PINS.
*FOR FACTORY USE ONLY.

NOTES

[1] In-Band Harmonics expressed in terms of spurious in-band signals generated at 1 MHz encode rate at analog inputs shown in ( ).
[2] Measured from leading edge of Encode Command to time associated data are valid.
[3] RMS signal to rms noise ratio with 100kHz analog input.
[4] For full-scale step input, 12-bit accuracy attained in specified time.
[5] Recovers to specified performance in specified time after 2 × FS input overvoltage.
[6] With analog input 40dB below FS.
[7] With FS analog input. (Large-signal bandwidth flat within 0.5dB, dc to 500kHz.)
[8] Externally adjustable to zero.
[9] Transition from digital "0" to digital "1" initiates encoding.
[10] Output data are TTL-compatible when analog input is within specified range. Negative over-voltage inputs cause tri-state output to drift to "high" condition and may create erroneous output (see text).
[11] Case Temperature. Models HAS-1201SM/SMB will operate with derated performance over temperature range of −55°C to +100°C; consult factory for details.
[12] Maximum junction temperature is +150°C.

Specifications subject to change without notice.

Table 1. HAS-1201 Specifications

(courtesy of Analog Devices)

PARAMETER	SPECIFICATION
Conversion Rate	409.6 kHz
Noise Floor (400 Hz BW)	-90 dBfs
Harmonic Distortion (14-175 kHz @ -6 dBFS)	-65 dBc
Intermodulation Dist (14-175 kHz @ -6dBFS)	-65 dBc

Table 2. Required A/D Performance of VLF/LF Receiver

PARAMETER	SPECIFICATION
Conversion Rate	409.6 kHz
Noise Floor (400 Hz BW)	-96 dBfs
Harmonic Distortion (14-175 kHz @ -6 dBFS)	-83 dBc
Intermodulation Dist (14-175 kHz @ -6dBFS)	-82 dBc

Table 3. HAS-1201 Measured Performance Summary